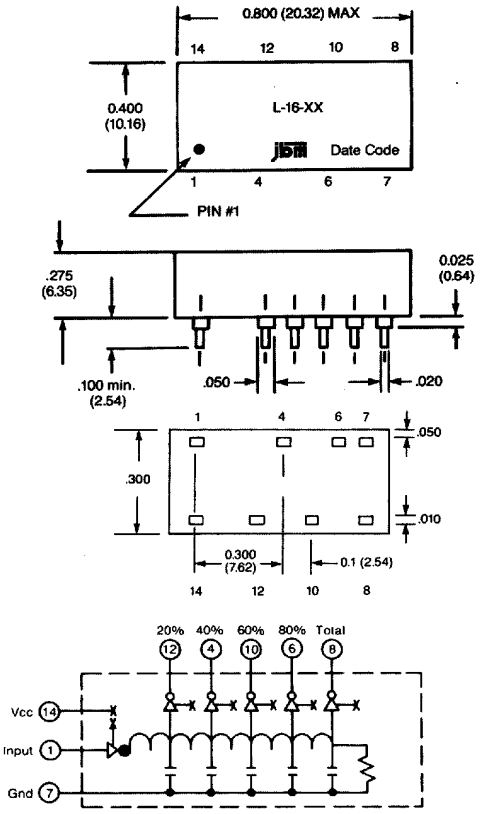
Delay Range 60-500 nsec

STYLE L-16 (14-pin Outline)

High Speed CMOS
5 equally-spaced taps



FEATURES

- CMOS, TTL compatible
- Low power
- Low current
- 14-pin DIP configuration

Input Test Conditions:

Pulse width . . . . . 2 × Td
Input rise time (10/90%) . . . . . 6 ns
Input fall time (90/10%) . . . . . 6 ns
Input voltage 3.2V
V_{CC} . . . . . 5.0V ± .05V

Environment:

Operating temperature . . . . . −40°C to +85°C
Storage temperature . . . . . −55°C to +125°C
Operating supply voltage . . . . . 4.75V to 5.25V

Output characteristics:

Logic "0" . . . . . 0.4V max
Logic "1" . . . . . 3.85V min
Supply Current . . . . . 35mA typ.

	DELAY TIMES IN (ns) NANOSECONDS @ 25° C				
JBM P/N	TAP 1 PIN 12	TAP 2 PIN 4	TAP 3 PIN 10	TAP 4 PIN 6	OUTPUT PIN 8
L-16-50	12 ± 2ns	24 ± 2ns	36 ± 2ns	48 ± 2ns	60 ± 4%
L-16-51	15 ± 2ns	30 ± 2ns	45 ± 3ns	60 ± 3ns	75 ± 4%
L-16-52	20 ± 2ns	40 ± 3ns	60 ± 3ns	80 ± 4%	100 ± 4%
L-16-53	25 ± 3ns	50 ± 3ns	75 ± 3ns	100 ± 4%	125 ± 4%
L-16-54	30 ± 3ns	60 ± 3ns	90 ± 4ns	120 ± 4%	150 ± 4%
L-16-55	35 ± 3ns	70 ± 3ns	105 ± 4%	140 ± 4%	175 ± 4%
L-16-56	40 ± 3ns	80 ± 4%	120 ± 4%	160 ± 4%	200 ± 4%
L-16-57	45 ± 3ns	90 ± 4%	135 ± 4%	180 ± 4%	225 ± 4%
L-16-58	50 ± 3ns	100 ± 4ns	150 ± 4%	200 ± 4%	250 ± 4%
L-16-59	60 ± 3ns	120 ± 4%	180 ± 4%	240 ± 4%	300 ± 4%
L-16-60	70 ± 5%	140 ± 4%	210 ± 4%	280 ± 4%	350 ± 4%
L-16-61	80 ± 5%	160 ± 4%	240 ± 4%	320 ± 4%	400 ± 4%
L-16-62	90 ± 5%	180 ± 4%	270 ± 4%	360 ± 4%	450 ± 4%
L-16-63	100 ± 5%	200 ± 4%	300 ± 4%	400 ± 4%	500 ± 4%

Consult factory for other delays, tolerances and logic families.