**SatCon Electronics**
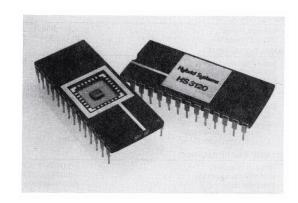
## Double Buffered 12-Bit MDAC

### FEATURES

- Monolithic Construction
- 12 Bit Resolution
- 0.01% Non-Linearity
- jup Compatible
- 4-Quadrant Multiplication
- Latch-up Protected

### DESCRIPTION

The HS 3120 is a precision monolithic 12-bit multiplying DAC with internal two-stage input storage registers for easy interfacing with microprocessor busses. It is packaged in a 28-pin DIP to give high I/O design flexibility.
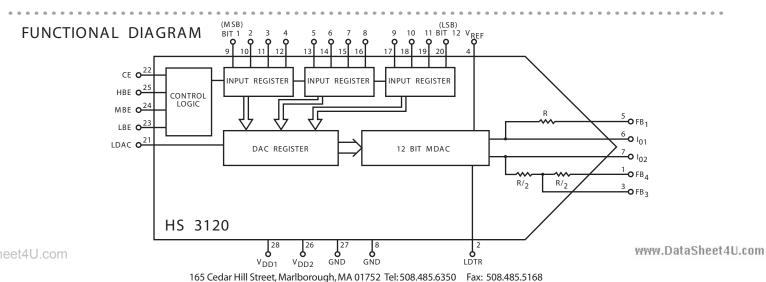
DOUBLE BUFFERED - The input registers are sectioned into 3 segments of 4 bits each, all individually addressable. The DAC-register, following the input registers, is a parallel 12-bit register for holding the DAC data while the input registers are updated. Only the data held in the DAC register determines the analog output value of the converter.

MICRO PROCESSOR COMPATIBLE — The HS 3120 has been designed for great flexibility in connecting to bus-oriented systems. The 12 data inputs are organized into 3 independent addressable 4-bit input registers such that the HS 3120 can be connected to either a 4, 8 or 16-bit data bus. The control logic of the HS 3120 includes chip enable and latch enable inputs for flexible memory mapping. All

controls are level-triggered to allow static or dynamic operation.

VERSATILE OUTPUTS - A total of 5 output lines are provided by the HS 3120 to allow unipolar and bipolar output connection with a minimum of external components. The feedback resistor is internal. The resistor ladder network termination is externally available, thus eliminating an external resistor for the 1 LSB offset in bipolar mode.

MONOLITHIC CMOS CONSTRUCTION - The HS 3120 is a one-chip CMOS circuit with a resistor ladder network designed for 0.01% linearity without laser trimming. Small chip size and high manufacturing yields result in greatly reduced cost.

## FUNCTIONAL DIAGRAM



HS 3120

## SPECIFICATIONS

(Typical @ 25ºC, nominal power supply, $V_{REF}$=+10V, unipolar unless otherwise noted).

| MODEL | HS3120-2 | HS 3120-0 |
|---|---|---|
| TYPE | MULTIPLYING, DOUBLE BUFFERED INPUTS | |
| **DIGITAL INPUT** | | |
| Resolution | 12-Bits | |
| 2-Quad. Unipolar Coding | Binary[1], Comp. Binary[1] | |
| 4-Quad. Bipolar Coding | Offset Binary | |
| Logic Compatibility[2] | CMOS, TTL | |
| Input Current | ±1 µA (max) | |
| Data Set-up Time[3] | 250nS (min) | |
| Strobe Width[3] | 250nS (min) | |
| Data Hold Time[3] | OnS (min) | |
| **REFERENCE INPUT** | | |
| Voltage Range | ±25V (max) | |
| Input Impedance | 8k ±50% | |
| **ANALOG OUTPUT** | | |
| Scale Factor | 125µA/VRef ±50% | |
| Scale Factor Accuracy[4] | ±0.4% | |
| Output Leakage[5] | | |
| @25ºC | <10nA (max) | |
| @125ºC | <200nA (max) | |
| Output Capacitance | | |
| $C_{OUT}$ 1, all inputs high | 80pF | |
| $C_{OUT}$ 1, all inputs low | 40pF | |
| $C_{OUT}$ 2, all inputs high | 40pF | |
| $C_{OUT}$ 2, all inputs low | 80pF | |
| **STATIC PERFORMANCE** | | |
| Integral Linearity | ±0.015% F.S.R. (max) | ±0.05% F.S.R. (max) |
| Differential Linearity | ±0.024% F.S.R. (max) | ±0.097% F.S.R. (max) |
| Monotonicity | Guaranteed to 12 bits | Guaranteed to 10 bits |
| Monotonicity Temp. Range | | |
| C-Models | 0ºC to +70ºC | |
| B-Models | −55ºC to +125ºC | |
| **DYNAMIC PERFORMANCE** | | |
| Digital Small Signal Settling | 1.0µsec | |
| Full Scale Transition Settling | | |
| to 0.01% (strobed) | 2.0µsec | |
| Reference Feedthrough Error (VRef=20Vpp) | | |
| @1kHz | <1mV | |
| @10kHz | 2mV | |
| Delay to output | | |
| from Bits input | 100nS[6] | |
| from LDAC | 200nS[6] | |
| from CE | 120nS[6] | |
| **STABILITY (Over Specified Temp. Range)** | | |
| Scale Factor[4] | 2 ppm F.S.R./ºC (max) | |
| Integral Linearity | 0.2 ppm F.S.R./ºC (max) | |
| Differential Linearity | 0.2 ppm F.S.R./ºC (max) | |
| Monotonicity Temp. Range | | |
| C-Option | 0ºC to +70ºC | |
| B-Option | −55ºC to +125ºC | |
| **POWER SUPPLY (VDD)** | | |
| Operating Voltage (specifications guaranteed) | +15V ±5% | |
| Maximum Voltage Range | +5V to 16V | |
| Current | 2.5mA (max) | |
| Rejection Ratio | 0.002% /% (max) | |
| **TEMPERATURE RANGE** | | |
| Operating C-Option | 0ºC to +70ºC | |
| Operating B-Option | 55ºC to +125ºC | |
| Storage | −65ºC to +150ºC | |
| **MECHANICAL** | | |
| Case Style | 28-pin double DIP | |
| C-Option | ceramic | |
| B-Option | ceramic | |

NOTES:
* Same as HS 3120-2
1. The input coding is complementary binary if $I_{O2}$ is used.
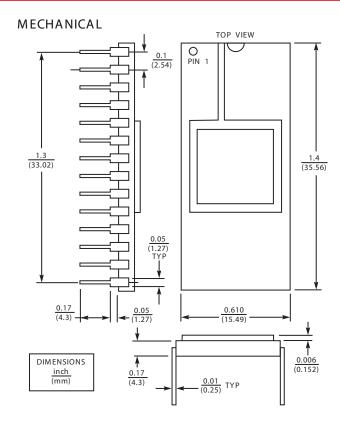2. Digital input voltage must not exceed supply voltage or go below −0.5V.
   "0" <0.8V, 2.4V < "1" $V_{DD}$
3. All strobes are level triggered. See TIMING DIAGRAM.
4. Using the internal feedback resistor and an external opamp.
5. The output leakage current will create an offset voltage at the external opamps output. It doubles
   every 10ºC temperature increase.
6. Delay times are twice the amount shown at TA =+125ºC

## PIN ASSIGNMENTS

| PIN | FUNCTION |
|---|---|
| 1 | $FB_4$, Feedback Bipolar Operation |
| 2 | LDTR, Ladder Termination |
| 3 | $FB_3$, Feedback Bipolar Operation |
| 4 | $V_{REF}$ Reference Voltage Input |
| 5 | $FB_1$, Feedback, Unipolar/Bipolar |
| 6 | $I_{01}$, Current out into virtual ground |
| 7 | $I_{02}$, Current out-complement of $I_{01}$ |
| 8 | $V_{SS}$, Ground, Analog and DAC Register |
| 9 | Bit 1, MSB |
| 10 | Bit 2 |
| 11 | Bit 3 |
| 12 | Bit 4 |
| 13 | Bit 5 |
| 14 | Bit 6 |
| 15 | Bit 7 |
| 16 | Bit 8 |
| 17 | Bit 9 |
| 18 | Bit 10 |
| 19 | Bit 11 |
| 20 | Bit 12 |
| 21 | LDAC, Transfers data from input to DAC register |
| 22 | CE, Chip Enable, active low |
| 23 | LBE, Bit 12 to Bit 9 Enable |
| 24 | MBE, Bit 8 to Bit 5 Enable |
| 25 | HBE, Bit 4 to Bit 1 Enable |
| 26 | $V_{DD2}$, Supply Analog and DAC Register |
| 27 | $V_{SS1}$, Ground input latches |
| 28 | $V_{DD1}$, Supply input latches |

NOTE: Pins 8 and 27 and pins 26 and 28 must be connected externally.

## MECHANICAL



TOP VIEW

PIN 1

0.1 (2.54)

1.3 (33.02)

1.4 (35.56)

0.05 (1.27) TYP

0.17 (4.3)

0.05 (1.27)

0.610 (15.49)

0.006 (0.152)

0.17 (4.3)

0.01 (0.25) TYP

DIMENSIONS inch (mm)

### CONNECTIONS

| | |
|---|---|
| Unipolar Operation: | Connect $I_{01}$ and $FB_1$ Tie $I_{02}$, (Pin 7). $FB_3$, (Pin 3), $FB_4$, (Pin 1) all to Ground (Pin 8) |
| Bipolar Operation: | Connect $I_{01}$, $I_{02}$, $FB_1$, $FB_3$, $FB_4$ Tie LDTR to $I_{02}$ |
| Grounding: | Connect all GRD to system analog ground and tie this to digital ground. |
| NOTE: | All unused input must be grounded |

## Consult factory for application information.

### ORDERING INFORMATION

| MODEL | DESCRIPTION |
|---|---|
| HS 312000 | Double Buffered 12-Bit MDAC. Commercial |
| HS 3120C-2 | Double Buffered 12-Bit MDAC. Commercial |
| HS 3120B-0 | Double Buffered 12-Bit MDAC. MIL-STD-883C |
| HS 3120B-2 | Double Buffered 12-Bit MDAC. MIL-STD-883C |

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