FLASH MODULE

AVAILABLE AS MILITARY SPECIFICATIONS

•SMD 5962-94612
•MIL-STD-883

FEATURES

- SMD 5962-94612 Pending
- Fast Access Times: 70, 90, 120 and 150ns
- Operation with single 5 volt supply
- User configurable as 512Kx32, 1Mx16, or 2Mx8
- Eight Equal Sectors of 64K Bytes for each 512Kx8
- Compatible with JEDEC EEPROM command set
- Any Combination of Sectors can be Erased
- Supports Full Chip Erase
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built in decoupling caps for low noise operation
- Suspend Erase/Resume Function
- Individual Byte Read/ Write Control
- 10,000 Program/Erase Cycles
- Packaging
  - 68 lead CQFP
  - 66 pin PGA

GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8F512K32 is a 16 Megabit CMOS FLASH Module organized as 512Kx32 bits. The AS8F512K32 achieves high speed access (70 to 150 ns), low power consumption and high reliability by employing advanced CMOS memory technology.

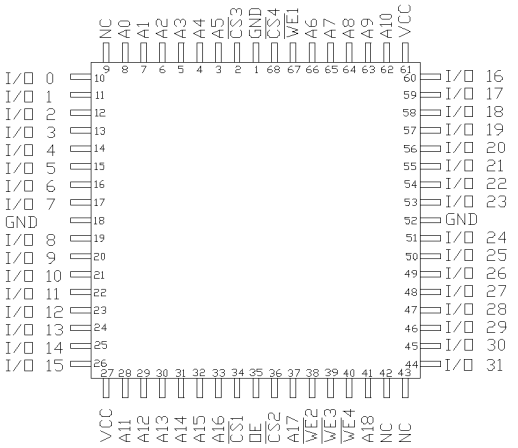
An on-chip state machine controls the program and erase functions. The embedded byte-program and sector/ chip erase functions are fully automatic. Data-protection of any sector combination is accomplished using a hardware sector-protection feature.

The *Erase/Resume function* allows the sector erase operation to read data from, or program to a non-erasing sector, then resume the erase operation.

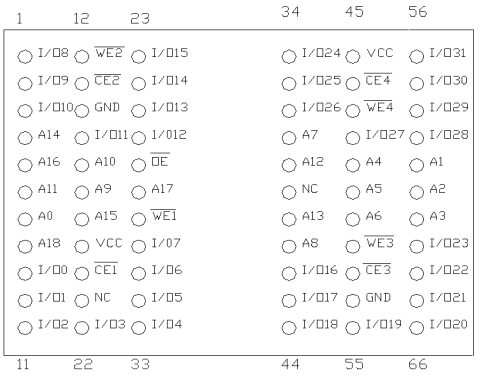
Device operations are selected by using standard commands into the command register using standard microprocessor write timings. The command register acts as an input to an internal state machine that interprets the commands, controls the erase and programming operations, outputs the status of the device, and outputs data stored in the device. On initial power-up operation, the device defaults to the read mode.

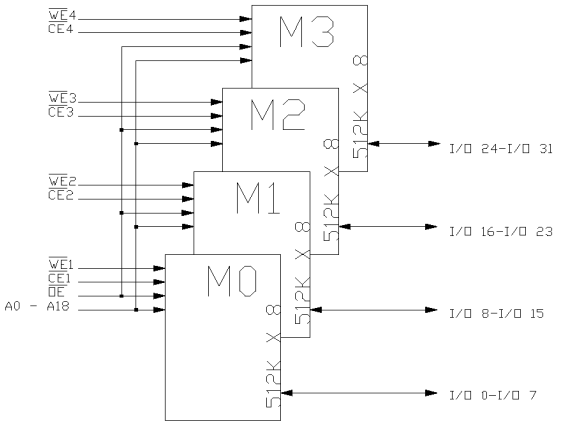
PIN ASSIGNMENT (Top View)

68 Lead CQFP



66 Lead PGA





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OPERATIONS

Read Mode

A low-level logic signal is applied to $\overline{CE}$ and $\overline{OE}$ pins to read the output of the AS8F512K32. The $\overline{CE}$ is power control and is used for device selection.

The delay from stable address to valid output data is the address access time (t_{AVQA}). The delay from $\overline{CE}$ equals logic low and stable addresses to valid output data is the chip-enable access time (t_{ELQV}). The output-enable access time (t_{GLQV}) is the delay from $\overline{OE}$ =low logic to valid output data, when $\overline{CE}$ =low logic and addresses are stable for at least t_{AVQA}-t_{GLQV}.

Standby Mode

I_{CC} supply current is reduced by applying a logic-high on the $\overline{CE}$ to enter the standby mode. In the standby mode, the outputs are placed in the high impedance state.

If the device is deselected during erasure or programming, the device continues to draw active current until the operation is complete.

Output Disable

$\overline{OE}$= V_{IL} or $\overline{CE}$=V_{IH}, output from the device is disabled and the output pins (DQ0 - DQ7) are placed in the high-impedance state.

Erasure and Programming

Erasure and programming of the AS8F512K32 are accomplished by writing a sequence of commands using standard microprocessor write timings. The commands are written to a command register and input to the command state machine. The command state machine interprets the command entered and initiates program, erase, suspend, and resume operations as instructed. The command state machine acts as the interface between the write-state machine and external chip operations. The write-state machine controls all voltage generation, pulse generation, preconditioning and verification of the contents of the memory. Program and block/chip-erase functions are fully automatic. Once the end of a program or erase operation has been reached, the device internally resets to the read mode. If V_{CC} drops below the low-voltage-detect level (VLKO), any operation in progress is aborted and the device resets to the read mode. If a byte-program or chip-erase operation is in progress, additional program/erase operations are ignored until the operation completes.

Command Definitions

Operating modes are selected by writing particular address and data sequences into the command register ***Command Sequence Table*** . The device will reset to read mode if an incorrect address and data value or writing them in the incorrect sequence transpires. The command register does not fill an addressable memory location. The register is used to store the command sequence, along with the address and data needed by the memory array. Commands are written by setting $\overline{CE}$=V_{IL} and $\overline{OE}$= V_{IH} and bring $\overline{WE}$ from logic-high to logic-low. Addresses are latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. Holding $\overline{WE}$ =V_{IL} and toggling $\overline{CE}$ can be used as an alternative.

Read/Reset Command

The read/reset mode is activated by writing either of the two read/reset command register. The device remains in this mode until one of the other valid command sequences is input into the command register. Memory data can be read with standard microprocessor read-cycle timing in the read mode.

On power up, the device defaults to the read/reset mode. A read/reset command sequence if not required and memory data is available.

Algorithm-Selection Command

The algorithm-selection command allows access to binary code that matches the device with the proper programming -and erase-command operations. After writing the three bus cycle command sequence, the first byte of the algorithm-selection code (01) can be read from address XX00. The second byte of the code (A4) can be read from address XX01. This mode remains in effect until another valid command sequence is written to the device.

Byte-Program Command

Byte-programming is a four-bus-cycle-command sequence. The first three bus cycles put the device into the program-setup state. The fourth bus cycle loads the address location and the data to be programmed into the device. The addresses are latched on the falling edge of $\overline{WE}$ and the data is latched on the rising edge of $\overline{WE}$ in the fourth cycle. The raising edge of $\overline{WE}$ starts the byte-program operation. The embedded byte-programming function automatically provides needed voltage and timing to program and verify the cell margin. Any further commands written to the device during the program operation are ignored.

Programming can be preformed at any address

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location in any order. When erased, all bits are in a logic state 1. Logic 0s are programmed into the device. Attempting to program logic 1 into a bit that has been previously programmed to logic 0 causes the internal pulse counter to exceed the pulse-count limit. This sets the exceed-timing-limit indicator (DQ5) to a logic high state. Only an erase operation can change bits from logic 0 to logic 1.

The status of the device during the automatic programming operation can be monitored for the completion using the data-polling feature or the toggle-bit feature . See the "operation status" for the full description.

Chip Erase Command

Chip-erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the chip erase command. This command sequence is required to ensure that the memory contents are not erased accidentally. The raising edge of $\overline{WE}$ starts the chip erase operation. Any further commands written to the device during the chip erase operation is ignored.

The embedded chip erase function automatically provides voltage and timings needed to program and verify all the memory cells prior to electrical erase. It then erases and verifies the cell margin automatically. The user is not required to program the memory cells prior to erase. The status of the device during the automatic chip erase operation can be monitored for completion using the data-polling feature. See the "operation status" section for a full description.

Sector-Erase Command

Sector erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the sector erase command and the sector address location to be erased. Any address location within the desired sector can be used. The addresses are latched on the falling edge of $\overline{WE}$ in the sixth bus cycle. After a delay of 100-µs from the rising edge of $\overline{WE}$, the sector erase operation begins in the selected source.

Sectors can be selected to be erased concurrently during the sector-erase command sequence. For each additional sector selected for erase, another bus cycle is issued. The bus cycle loads the next sector-address location and the sector-erase command. The time between the end of the previous bus cycle and the start of the next bus cycle must be less than 100 µs-other wise, the new sector location is not loaded. A time delay of 100 µs from the raising edge of the last $\overline{WE}$ starts the sector erase operation. If there is a falling edge of $\overline{WE}$ within the 100 µs time delay, the timer is reset.

One to eight sector address locations can be loaded in any order. The state of the delay timer can be monitored using the sector-erase-delay indicator (DQ3). If DQ3 is logic low, the time delay has not expired. See the "operation status" for the full description.

Any commands other than erase-suspend (B0) or sector erase (30) written to the device during the sector erase operation causes the device to exit the sector erase mode. The contents of the sector(s) selected for erase is not valid. To complete the sector-erase operation, reissue the sector erase command.

The embedded sector erase function automatically provides voltage and timings needed to program and verify all the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. The user is not required to program the memory cells prior to erase. The status of the device during the automatic sector erase operation can be monitored for completion using the data-polling feature or the toggle bit feature. See the "operation status" section for a full description.

Erase-Suspend Command

Sector-erase operations may be interrupted by the erase-suspend command (B0) , in order to read data from an unaltered sectors of the device. Erase-suspend is a one-bus-cycle command. The addresses can be V_{IL} or V_{IH} and the erase-suspend command (B0) is latched on the rising edge of $\overline{WE}$. Once the sector-erase operation is in progress, the erase-suspend command request the internal write-state-machine to halt operation at predetermined break points. The erase-suspend command is valid only during the sector-erase operation and is valid only during the byte-programming and chip-erase operations. The sector-erase delay timer expires immediately if the erase-suspend command is issued while the delay is active.

After erase-suspend is issued, the device takes between 0.1µs and 15 µs to suspend the operation. The

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toggle bit must be monitored to determine when the suspend has been executed. When the toggle bit stops toggling, data can be read from sectors that are not selected for erase. See the "operation status" section for a full definition. Reading from a sector marked for erase can result in invalid data.

Once the sector-erase operation is suspended, further writes of the erase-suspend command are ignored. Any command other than erase-suspend (B0) or erase-resume (30H) written to the device during the erase-suspend mode causes the device to exit the suspend mode. To complete the sector-erase operation, reissue the sector-erase command sequence.

Erase-Resume Command

The erase-resume command (30H) restarts a suspended sector erase operation from where it was halted to completion. Erase-resume is a one-bus-cycle command. The addresses can be VIH or VIL and the erase-resume command (30H) is latched on the rising edge of $\overline{WE}$. When an erase-suspend/ erase-resume command combination is written, the internal pulse counter (exceed timing limit) is reset. The erase-resume command is valid only in the erase-suspend state. After the erase-resume command is executed, the device returns to the valid sector-erase state and further writes of the erase-resume commands are ignored. After the device has resumed the sector-erase operation, another erase-resume command can be issued to the device.

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OPERATION STATUS

Status Bit Definition

During operation of the automatic embedded program and erase functions, the status of the device can be determined by reading the data state of designated outputs. The data-polling bit (DQ7) and toggle-bit (DQ6) require multiple successive reads to observe a change in the state of the designated output. Operation Status Flags Table defines the values of the Flag status.

Operation Status Flags[1] Table

Device Operations[2]	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Byte-programming in progress	D\	T	0	X	0	X	X	X
Byte-programming exceed time limit	D\	T	1	X	0	X	X	X
Byte-programming complete	D	D	D	D	D	D	D	D
Sector/chip erase in progress	0	T	0	X	1	X	X	X
Sector/chip erase exceed time limit	0	T	1	X	1	X	X	X
Sector/chip erase complete	1	1	1	1	1	1	1	1

NOTES:
1. T= toggle, D=data, X=data undefined
2. DQ4, DQ2, DQ1, DQ0 are reserved for future use.

Data-Polling DQ7

The data-polling status outputs the complement of the data latched into the DQ7 data register while the write-state machine is engaged in a program or erase operation. Data bit DQ7 changing from complement to true indicates the end of an operation. Data-polling is available only during the byte-programming, chip-erase, sector-erase, and sector-erase timing delay. Data-polling is valid after the rising edge of $\overline{WE}$ in the last bus cycle of the command sequence loaded into the command register.

During a byte-program operation, reading DQ7 outputs the complement of the DQ7 data to be programmed at the selected address location. Upon completion, reading DQ7 outputs the true DQ7 data loaded into the program data register. During the erase operations, reading DQ7 outputs a 0. Upon completion, reading DQ7 outputs a 1. Also, data polling must be performed at a new sector address that is within a sector being erased; otherwise the status is not valid. When using data-polling, the address should remain stable throughout the operation.

During a data-polling read, while $\overline{WE}$ is low, data bit DQ7 can change asynchronously. Depending on the read timing, the system can read valid data on DQ7, while other DQ pins are still invalid. A subsequent read of the device is valid.

Data-Polling DQ6

The function of toggle-bit status, is to output data on DQ6 that toggles between 1 and 0 while the write-state machine is engaged in a program or erase operation. When toggle-bit DQ6 stops toggling after two consecutive reads to the same address, the operation is complete. The toggle-bit is only available during the byte-programming, chip-erase, and sector-erase timing delay. Toggle-bit data is valid after the raising edge of $\overline{WE}$ in the last bus cycle of the command sequence loaded into the command register. Depending on the read timing, DQ6 can stop toggling while other DQ pins are still invalid. A subsequent read of the device is valid.

Exceed Time Limit DQ5

The program and erase operations use an internal pulse counter to limit the number of pulses applied. If the pulse count limit is exceeded, DQ5 is set to a 1 data state. This indicates that the program or erase operation has failed. DQ7 will not change from complemented data to true data and DQ6 will not stop toggling when read. To continue operation, the device must be reset.

This condition occurs when attempting to program a logic 1 state into a bit that has been programmed previously to a logic 0. Only an erase operation can change bits from 0 to 1. After reset, the device is functional and can be erased and reprogrammed.

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Sector-Load- Timer DQ3

DQ3 is the sector-load timer status bit it determines if the time to load additional sector addresses has expired. DQ3 remains a logic low for 80 µs after completion of a sector-erase sequence. This indicates another sector-erase command sequence can be issued. If DQ3 is at logic high, it indicates that the delay has expired and attempts to issue additional sector-erase commands are ignored.

The data polling bit and toggle bit are valid during the 100 µs time delay and can be used to determine if a valid sector erase command has been issued. To ensure additional sector erase commands have been accepted, the status of DQ3 should be read before and after each additional sector-erase command. If DQ3 is at a logic low on both reads, then the additional sector-erase was accepted.

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DATA PROTECTION

Hardware-Sector Protection Feature

This feature disables both programming and erase operations on any combination of one to eight sectors. Commands to program or erase a protected sector do not change the data contained in the sector. The data-polling and toggle bits operate for 2µs to 100µs and then return to valid data. This feature is enabled using high-voltage V_{ID} (11.5V to 12V) on address pin A9 and control pin $\overline{OE}$ and V_{IL} on control pin $\overline{CE}$.

The device is delivered with all sector unprotected . Sector-unprotected mode is available to unprotect protected sectors.

Sector Protect Operation

The sector protect mode is activated when $\overline{WE}$=V_{IH}, $\overline{CE}$=V_{IL}, and address pin A9 and control pin $\overline{OE}$ are forced to V_{ID}. The sector-select address pins A18, A17, and A16 are used to select the sector to be protected. Address pins A0-A15 and I/O pins DQ0- DQ7 must be stable and can be V_{IL} or V_{IH}. Once the addresses are stable, $\overline{WE}$ is pulsed low for 100 µs. The operation begins on the falling edge of $\overline{WE}$ and terminates on the raising edge of $\overline{WE}$.

Sector Protect Verify

Verification of sector protection is activated when $\overline{WE}$=V_{IH}, $\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IL}, and address pin A9 is V_{ID}. Address pins A0 and A6 are set to V_{IL}, and A1 is set to V_{IH}. The sector address pins A18, A17, and A16 select the sector to be verified. The other addresses can be V_{IH} or V_{IL}. If the sector selected if protected, the DQs output O1. If the sector selected is unprotected the DQs output is 00.

Sector protection can also be verified using the algorithm-selection command. After issuing the three bus-cycle command sequence, the sector protection status can be read on DQ0. Set address pins A0 = V_{IL}, A1 = V_{IH}, and A6 = V_{IL}. Sector address pins A18, A17, and A16 select the sector to be verified. The remaining addresses are set to V_{IL}. If the sector selected is protected. DQ0 outputs a 1 state, and if the sector selected is unprotected DQ0 outputs a 0 state. This mode remains in effect until another valid sequence is written to the device.

Sector Unprotect

Prior to sector unprotected, all sectors should be protected using the sector unprotect mode. The sector unprotect is activated when $\overline{WE}$=V_{IH}, and control pin $\overline{CE}$, $\overline{OE}$, and address pin A9 are forced to V_{ID}. Address pins A6, A12, and A16 are set to V_{IH}. The sector select address pins A18, A17, and A16 can be V_{IL} or V_{IH}. All eight sectors are unprotected in parallel. Once the inputs are stable, $\overline{WE}$ is pulsed low for 10ms. The unprotect operation begins on the falling edge of $\overline{WE}$ and terminates on the raising edge of $\overline{WE}$.

Sector Unprotect Verify

Verification of the sector unprotected is activated when $\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, and address pin A9 = V_{ID}. Select the sector to be verified. Address A1 and A6 are set to V_{IH} and A0 to V_{IL}. The other addresses can be V_{IL} or V_{IH}. If the sector selected is protected, the DQs output a 01, if sector selected is unprotected the DQs output a 00. Sector unprotect can also be read using the algorithm selection command.

Low VCC Write Lock Out

During power-up and power-down , are locked out for V_{CC} less than VLKO If V_{CC}<VLKO, the command inputs is disabled and the device is reset to the read mode. On power-up, if $\overline{CE}$=V_{IL}, $\overline{WE}$= V_{IL}, and $\overline{OE}$=V_{IH}, the device does not accept commands on the raising edge of WE. The device automatically powers up in the read mode.

Glitiching

Pulses of less than 5ns (typical) on $\overline{WE}$, $\overline{OE}$, and $\overline{CE}$ will not issue a write cycle.

Power Supply Consideration

Each device should have as a maximum of 0.1 µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Printed circuit traces to V_{CC} should have be appropriate to handle the current demand and minimize inductance.

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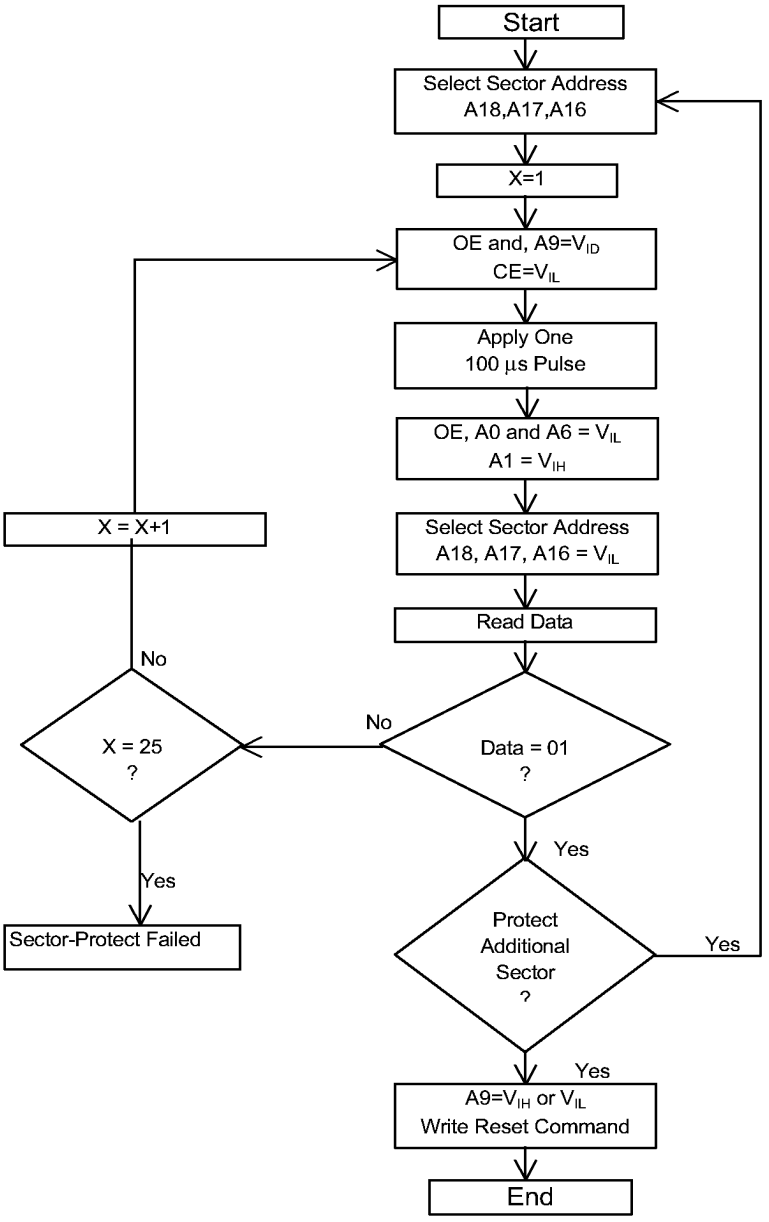

Flow Chart 1. Sector Protect Algorithm

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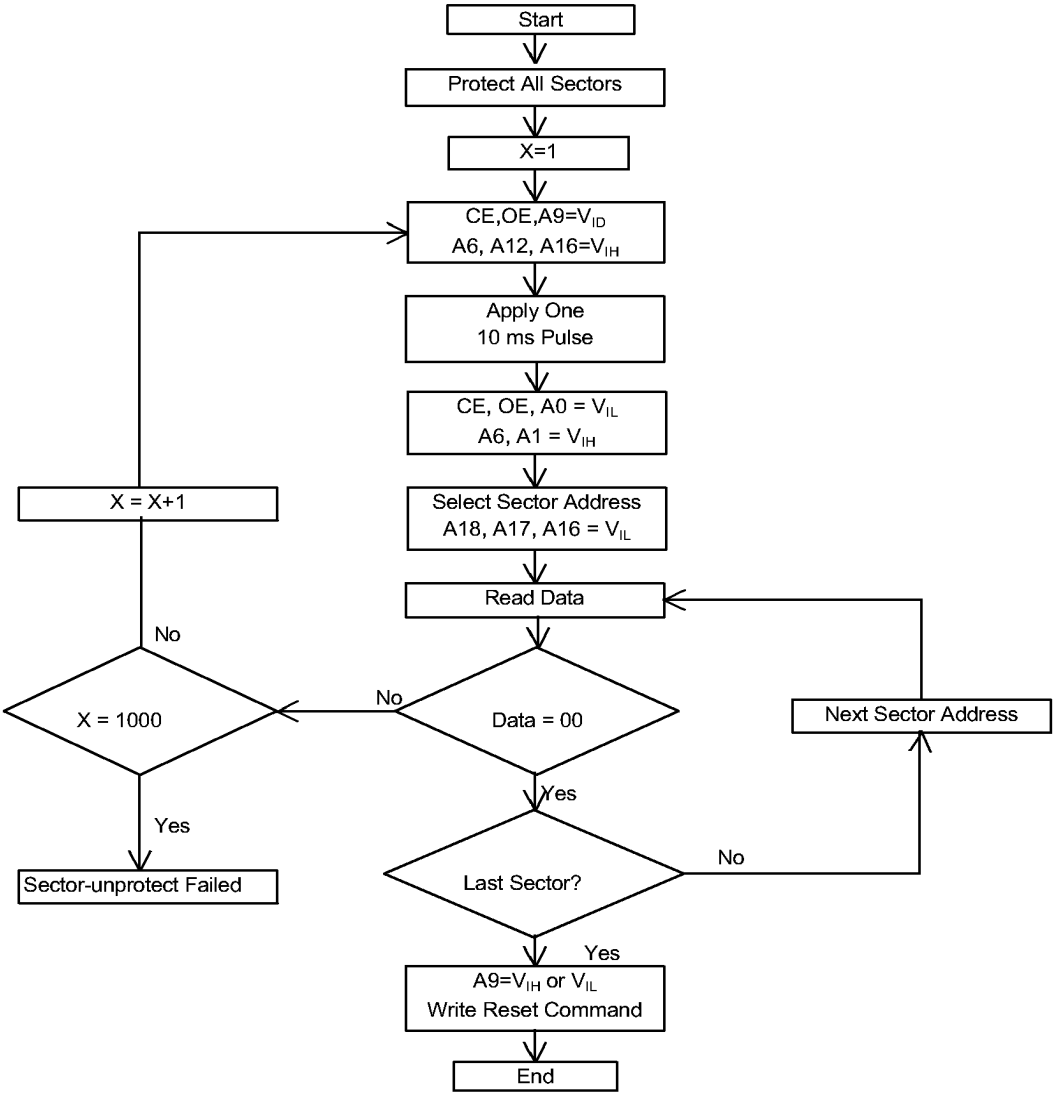

Flow Chart 2. Sector Unprotect Algorithm

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc (Note 1) .....-2.0V to +7.0V
A9 (Note 2)…..…… -2.0V to +12.5V
All Other Pins (Note 1).....…….....-2.0V to +7.0V
Operating Temperature, T_A (Ambient).....55°C to +125°C
Storage Temperature .....-65°C to +150°C
Power Dissipation…….....…...1.5W
Short Circuit Output Current (Note 3)….....200mA
Lead Temperature (soldering 10 seconds).....+300°C
Junction Temperature.....+165°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied, Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During Voltage transitions, inputs may overshoot Vss to -2.0V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins is Vcc +0.5V. During Voltage transitions, inputs may overshoot Vcc to +2.0V for periods of up to 20 ns. See Figure 2.

2. Minium DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 pins may overshoot Vss to -2.0V for periods of up to 20 nS. See Figure 1. Maximum DC input voltage on A9 is +12.5V inputs which may overshoot to +13.5V for periods of up to 20 ns. See Figure 2.

3. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.

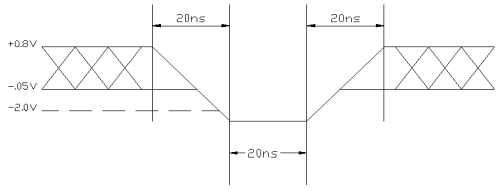

Figure 1.
Maximum Negative Overshoot Waveform

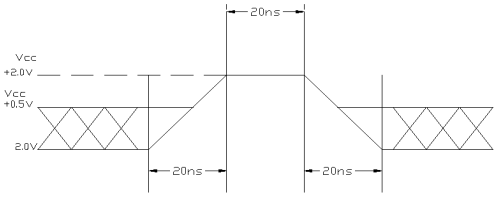

Figure 2 .
Maximum Positive Overshoot Waveform

Capacitance Table
V_{IN} = 0V, f = 1MHz, TA = 25°C

Symbol	Parameter	Maximum	Units
C_{ADD}	A0 - A18 Capacitance	50	pF
C_{OE}	OE\ Capacitance	50	pF
C_{WE} ,C_{CE}	WE\ and Chip Enable Capacitance	20	pF
C_{IO}	I/O0 - I/O 31 Capacitance	20	pF

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User Bus Operations								
Operation	**CS\ 1-4**	**OE**	**WE\ 1-4**	**A0**	**A1**	**A6**	**A9**	**I/O**
Read	L	L	H	X	X	X	X	Data Out
Output Disable	L	H	H	X	X	X	X	HIGH Z
Standby and Write Inhibit	H	X	X	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	Data In
Sector Protect	L	VID	L	X	X	X	VID	X
Verify Sector Protect	L	L	H	L	H	L	VID	Data Out
Sector Unprotect	See Chart 1	See Chart 1	L	L	H	H	See Chart 1	Data Out
Verify Sector Unprotect	L	L	H	L	H	H	VID	Data Out
Erase Operations	L	H	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1	See Note 1

Legend:
L = V_{IL}, H = V_{IH}, X = Don't Care, V_{ID} = 12V, See DC Charateristics for voltage levels

Note
1. See Chip/Sector Erase Operation Timings and Alternate CE\ Controlled Write Operation Timings.

Sector Address Table				
SECTOR	A18	A17	A16	ADDRESS RANGE
SA0	0	0	0	00000-0FFFF
SA1	0	0	1	10000-1FFFF
SA2	0	1	0	20000-2FFFF
SA3	0	1	1	30000-3FFFF
SA4	1	0	0	40000-4FFFF
SA5	1	0	1	50000-5FFFF
SA6	1	1	0	60000-6FFFF
SA7	1	1	1	70000-7FFFF

Pin Description	
Pin	Function
A0-A18	Address Inputs
I/O 0-31	Data Input/Outputs
CE\ 1-4	Chip Enable
WE\ 1-4	Write Enable
OE\	Output Enable
V_{SS}	Device Ground
V_{CC}	Device Internal Power Supply (5.0 V+/- 10%)

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Command Denfinitions Table

Command Sequence	Cycles	Bus Cycles											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXX	F0										
Read	4	5555	AA	2AAA	55	5555	F0	RA	RD				
Algorithm Selection	4	5555	AA	2AAA	55	5555	90	RA	RD				
Program	4	5555	AA	2AAA	55	5555	A0	PA	PD				
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA	30
Sector Erase Supend		XXXX	B0	Erase-supend vaild during sector-erase operation									
Sector Erase Resume		XXXX	30	Erase-resume vaild only after erase supend									

Legend:
RA = Address of the location to be read
PA = Address of the location to be programed
SA = Address of the sector to erased
Addresses A18, A17, A16 select 1 of 8 sectors
RD = Data to be read at selected address location
PD = Data to be programmed at selected address location
*Address pin A18, A17, A16, A15 = V_{IL} or V_{IH} for al bus cycle addresses except for program address (PA), sector address(SA), and read address (RA).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

Symbol	Parameter Description	Test Description	Min	Max	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}		±10.0	µA
I_{ID}	A9 Input Load Current (Note 3)	A9 = 12.5 V		200	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC}=V_{CC} Max		±10.0	µA
I_{CC1}	V_{cc} Active Current	CE\ = V_{IL}, OE\= V_{IH}, V_{CC} = V_{CC} Max, f = 5MHz		190	mA
I_{CC2}	V_{cc} Active Current (Note 1,2)	CE\ = V_{IL}, OE\= V_{IH}, V_{CC} = V_{CC} Max, f = 5MHz		240	mA
I_{CC3}	V_{cc} Standby Current	V_{CC} = V_{CC} Max, CE\ =V_{IH}, f = 5MHz		6.5	mA
V_{IL}	Input Low Voltage		-.05	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{ID}	Voltage for Sector Protected	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	A9 Output Low Voltage	I_{OL} = 12mA, V_{CC} = V_{CC} Min		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -2.5mA, V_{CC} = V_{CC} Min	0.85 x V_{CC}		V
V_{OH2}		I_{OH} = -100µA, V_{CC} = V_{CC} Min	V_{CC}-0.4		V
V_{LKO}	Low V_{cc} Lock-out Voltage		3.2	4.2	V

Notes:
1. Icc active while Embedded Program or Embedded Erase Algorithm is in progress.
2. Not 100% tested.
3. Applies to 32 bit operations.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

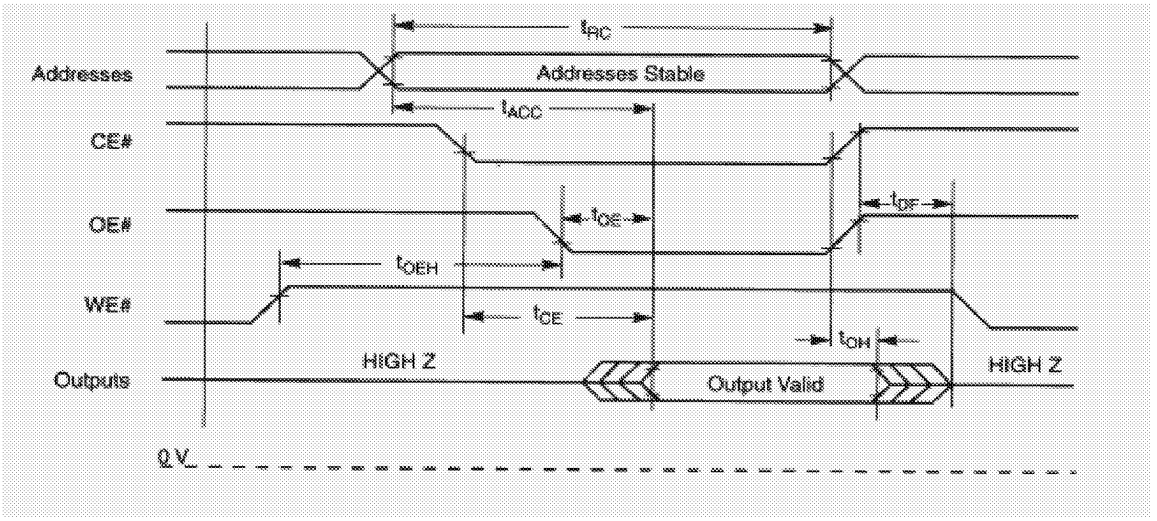
(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

AC Read Characteristics

Parameter Symbol		Parameter Description		Test Setup		Speed Options				Units
JEDEC	Std.					-70	-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)		CE\ =V_{IL}, OE\ = V_{IL}	Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE\ =V_{IL}, OE\ = V_{IL}	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid			Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Delay			Max	35	35	50	55	ns
	t_{OEH}	Output Enable Hold Time (Note 3)	Read		Min	0				ns
			Toggle and Data\ Polling		Min	10				ns
t_{EHQZ}	t_{HZ}	Chip Enable High to Output High Z (Note 2, 3)			Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 2, 3)				20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE\ or OE\, Whichever Occurs First			Min	0	0	0	0	ns

Notes:

1. See Test Specification for test conditions.
2. Output driver disable time.
3. Guaranteed but not Tested.



Read Operation Timings

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

Erase and Program WE\ Controlled

Parameter Symbol		Parameter Description		Speed Options				Units
JEDEC	Std.			-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	50	50	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recover time Before Write (OE\ high to WE\ low)	Min	0				ns
t_{ELWL}	t_{CS}	CE\ Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE\ Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Min	16				us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Max	30				sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation	Max	120				sec
t_{VCHEL}		V_{CC} Setup Time	Min	50				us
		Chip Program Time	Max	50				sec

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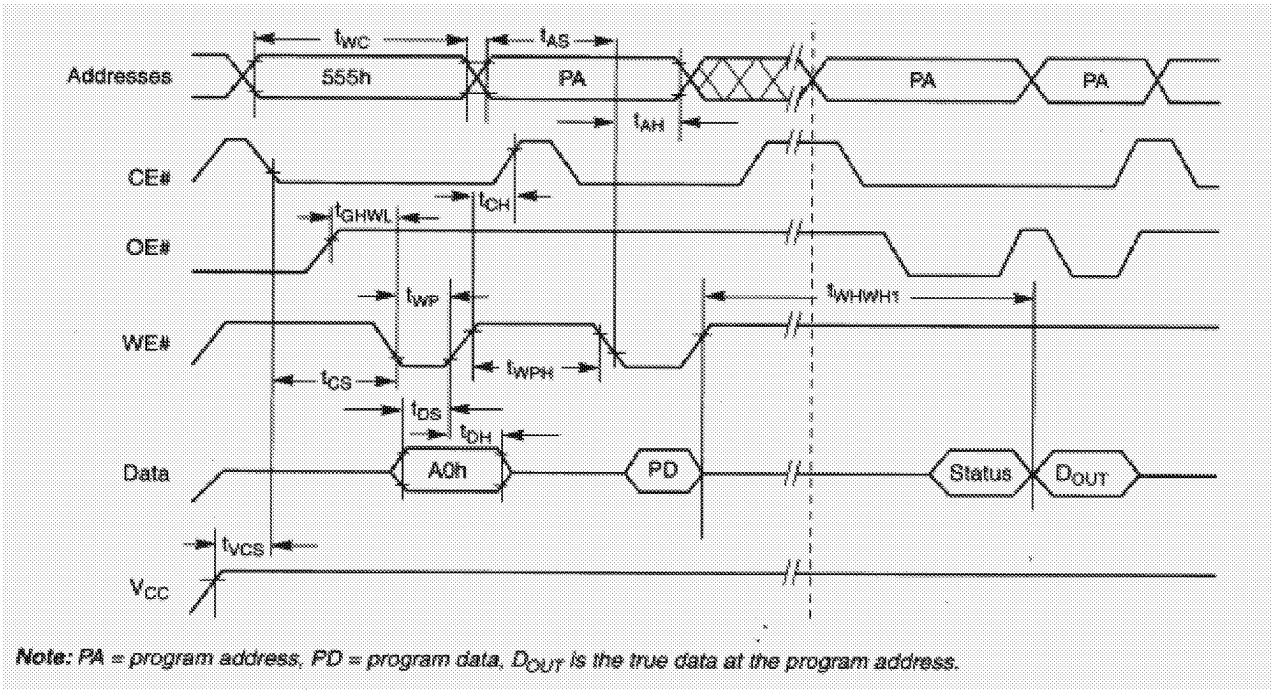
Program Operation Timings



***Note:** PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

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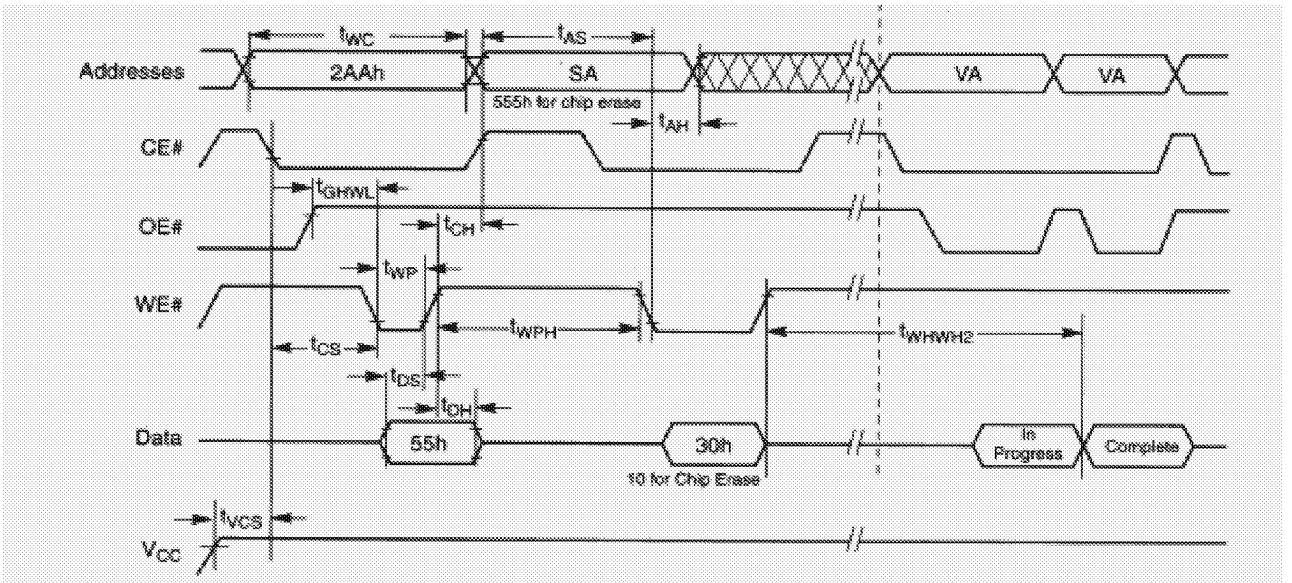
Chip/Sector Erase Operation Timings



Note:
SA = Sector Address. VA = Valid Address for reading status data.

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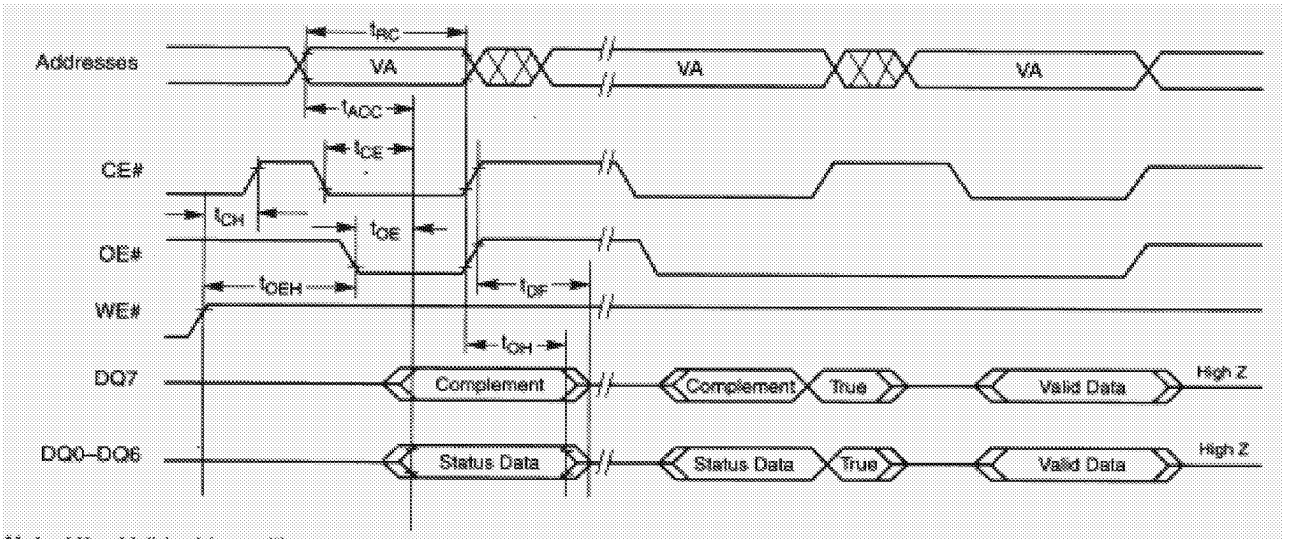
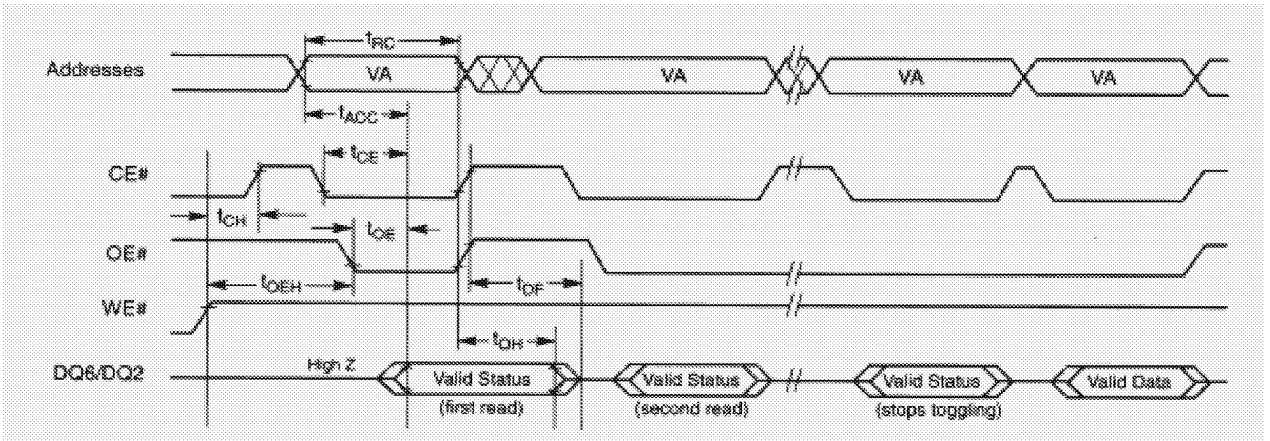
Data Polling Timings (During Embedded Algorithms)



Note: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle .

Toggle Bit Timings (During Embedded Algorithms)



Note:
VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C < TA < 125°C; V_{CC} = 5V +/- 10%)

Erase and Program CE\ Controlled

Alternate CE\Controlled Writes

Parameter Symbol		Parameter Description		Speed Options				Units
JEDEC	Std.			-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	40	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recover time Before Write	Min	0				ns
t_{WLEL}	t_{WS}	Setup Time, WE\	Min	0				ns
t_{EHWH}	t_{WH}	Hold Time, WE\	Min	0				
t_{ELEH}	t_{CP}	Pulse Duration CE\ Low	Min	40	45	50	50	ns
t_{EHEL}	t_{CPH}	Pulse Duration CE\ High	Min	20				ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Min	16				us
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation	Max	30				sec
		Chip Erase	Max	120				sec
		Chip Programming	Max	50				sec

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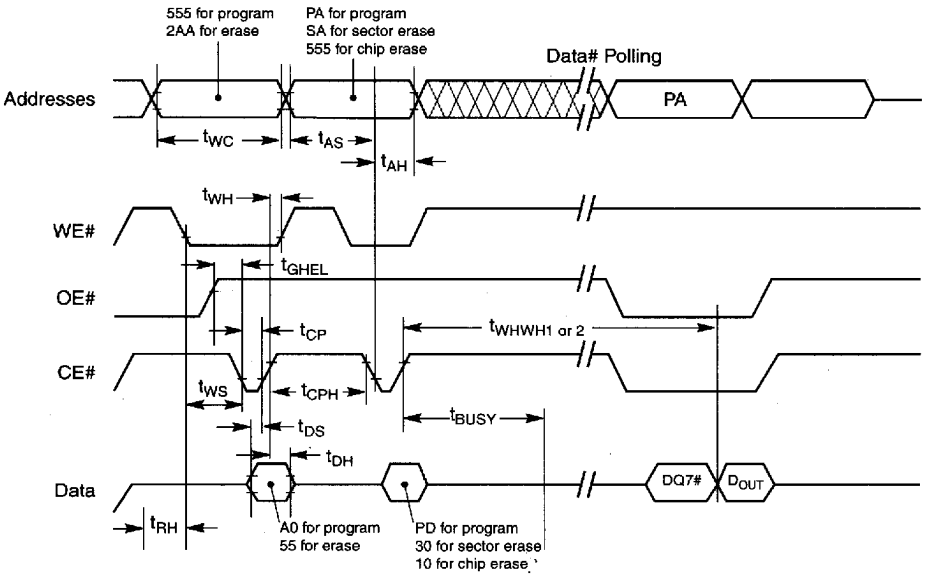
Alternate $\overline{CE}$ Controlled Write Operation Timings



Notes:

1. *PA = Program Address, PD = Program Data, SA = Sector Address, DQ7# = Complement of Data Input, D_{OUT} = Array Data.*
2. *Figure indicates the last two bus cycles of the command sequence.*

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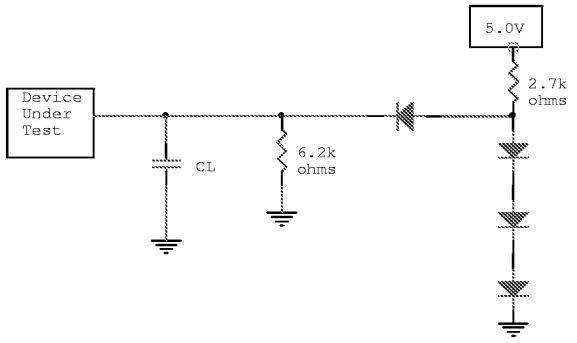
Test Conditions

Test Setup



Test Specifications

Test Conditions	-55	All Others	Unit
Output Load Cacacitance,CL	30	100	pF
Input Raise and Fall Time	5	20	ns
Input Pulse Levels	0.0 - 3.0	0.45 - 2.4	V
Input timing measurement reference levels	1.5	0.8	V
Output timing measurement reference levels	1.5	2.0	V

Note:
1. Diodes are IN3064 or equivalant

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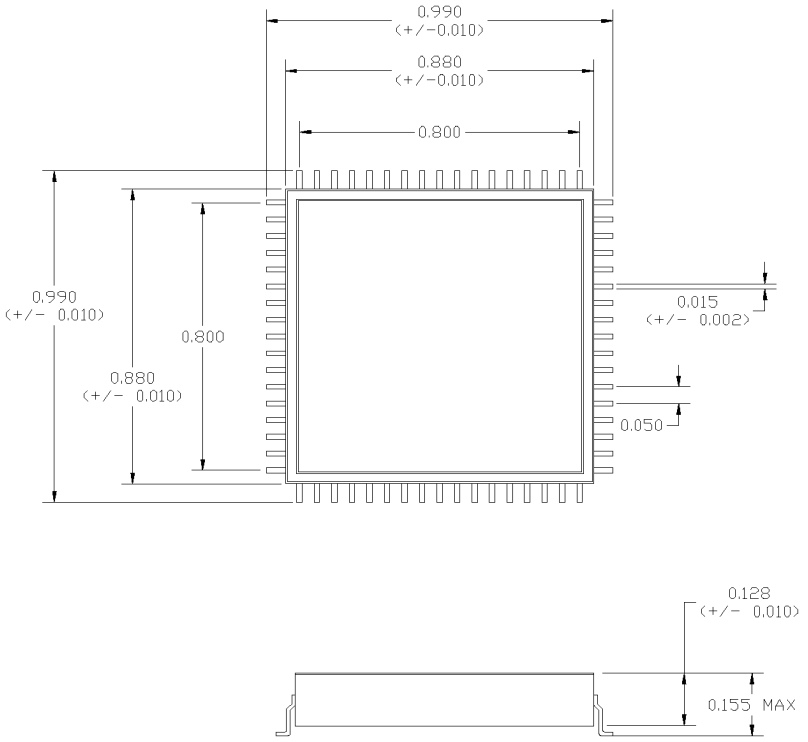
MECHANICAL DEFINITION

for the AS8F512K32 Ceramic Quad Flat Pack



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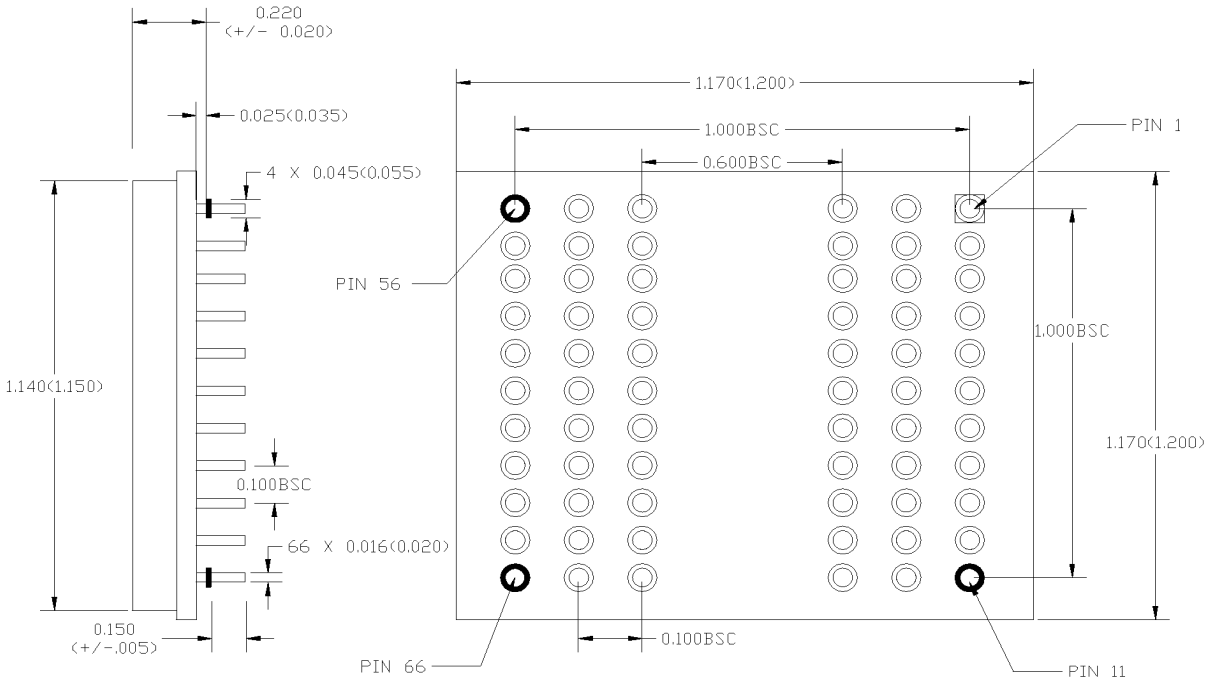
MECHANICAL DEFINITIONS

for the AS8F512K32 Pin Grid Array Package



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