REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added case outline Z to figure 1. Made changes to paragraph 1.2.2., 1.4., and table I. Corrected dimensions on case outline X. Made changes to figure 2. Rewrote entire document.	93-08-19	K. Cottongim

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A								
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

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DRAWING APPROVAL DATE
92-03-18

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, MIL-STD-1553 AND MIL-STD-1760, BC/RTU/MT, MULTIPLEXED TERMINAL, HYBRID

SIZE	CAGE CODE	5962-91734
A	67268	

SHEET 1 OF 25

DESC FORM 193
JUL 91

5962-E389-93

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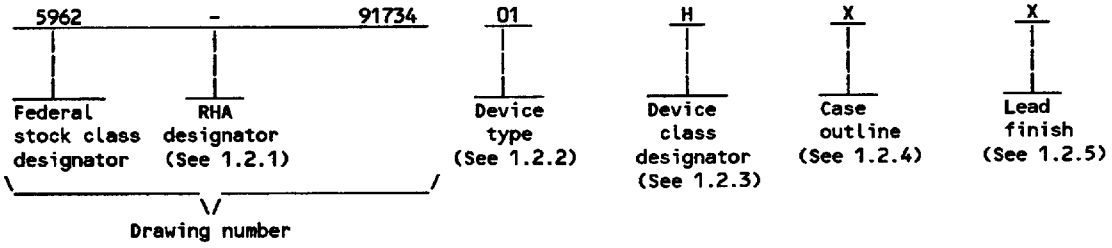
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-H-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-H-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	See 6.7	MIL-STD-1553, BC/RTU/MT, transceiver multiplexed terminal
02	See 6.7	MIL-STD-1553, BC/RTU/MT, transceiver multiplexed terminal
03	See 6.7	MIL-STD-1553, BC/RTU/MT, transceiver multiplexed terminal
04	See 6.7	MIL-STD-1760, BC/RTU/MT, transceiver multiplexed terminal

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
H or K	Certification and qualification to MIL-H-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	78	Dual-in-line
Y	See figure 1	82	Flat package
Z	See figure 1	78	Flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-H-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (V_{CC}):	
Devices types 01-04	-0.5 V dc to +7.0 V dc
Negative supply voltage range (V_{EE})	
Devices types 01, 02, and 04	+0.3 V dc to -18 V dc
Logic supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Power dissipation (P_D): 1/ 2/ 3/	
Device types 01 and 04	2.23 W
Device type 02	2.16 W
Device type 03	0.32 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}): 2/	
Device types 01, 02, and 04	6.13°C/W
Device type 03	112°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC}):	
Device types 01, 02, and 04	+4.5 V dc to +5.5 V dc
Device type 03	+4.75 V dc to +5.5 V dc
Logic supply voltage range (V_{DD}):	
Device types 01, 02, and 04	+4.5 V dc to +5.5 V dc
Device type 03	+4.75 V dc to +5.5 V dc
Negative supply voltage range (V_{EE}):	
Device types 01 and 04	-14.25 V dc to -15.75 V dc
Device type 02	-11.40 V dc to -12.60 V dc
Minimum logic high input voltage (V_{IH})	2.2 V dc
Maximum logic low input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Operating frequency (F_{OP})	16.0 MHz

1/ Applies up to T_C = +125°C.
2/ Hottest die.
3/ Assumes 100 percent transmitter duty cycle on one channel and 0 percent duty cycle on the other channel.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, and handbook. Unless otherwise specified, the following specifications, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-H-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-H-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-H-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Pin functions. The pin functions shall be as specified in table III.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-H-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.

3.6 Manufacturer eligibility. In addition to the general requirements of MIL-H-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DESC-EC) upon request.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups 1/	Device type	Limits		Unit
					Min	Max	
Logic supply current, idle 2/	I_{DD}	V_{DD} = 5.5 V, V_{CC} = 5.5 V, for all device types. V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02. f_{IN} = 16 MHz.	1,2,3	All	5.0	80	mA
Positive supply current, idle 3/	I_{CC1}			01,02,04	5.0	90	
				03	5.0	80	
Negative supply current, idle 4/	I_{EE1}			01,02,04	-5.0	-80	
Positive supply current, channel A = 25 percent duty cycle, channel B = idle 3/	I_{CC2}			01,02,04	5.0	90	
				03	5.0	230	
Positive supply current, channel B = 25 percent duty cycle, channel A = idle 3/	I_{CC3}			01,02,04	5.0	90	
				03	5.0	230	
Negative supply current, channel A = 25 percent duty cycle, channel B = idle 4/	I_{EE2}			01,04	-25	-130	
				02	-25	-135	
Negative supply current, channel B = 25 percent duty cycle, channel A = idle 4/	I_{EE3}			01,04	-25	-130	
				02	-25	-135	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups 1/	Device type	Limits		Unit
						Min	Max	
High level output voltage 5/	V_{OH1}	V_{DD} = 4.5 V, V_{CC} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, for all device types. V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02. 6/	I_{OH1} = -400 µA	1,2,3	All	2.4		V
High level output voltage 7/	V_{OH2}		I_{OH2} = -3.4 mA			3.7		
High level output voltage 8/	V_{OH3}		I_{OH3} = -6.8 mA			3.7		
Low level output voltage 8/	V_{OL1}		I_{OL1} = +6.8 mA				0.4	
Low level output voltage 9/	V_{OL2}		I_{OL2} = +2.0 mA				0.4	
Low level output voltage 10/	V_{OL3}		I_{OL3} = +4.0 mA				0.4	
Low level output voltage 7/	V_{OL4}		I_{OL4} = +3.4 mA				0.4	
High level input current 11/	I_{IH1}	V_{DD} = 5.5 V, V_{CC} = 5.5 V, V_{IN} = 2.7 V, for all device types. V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02.		1,2,3	All	-20	-155	µA
High level input current 12/	I_{IH2}					-50	-200	
High level input current 13/	I_{IH3}					-10	+10	
High level input current 14/	I_{IH4}					-10	-165	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups 1/	Device type	Limits		Unit
					Min	Max	
Low level input current 11/	I_{IL1}	V_{DD} = 5.5 V, V_{CC} = 5.5 V, V_{IN} = 0.4 V for all device types. V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02.	1,2,3	All	-20	-155	µA
Low level input current 12/	I_{IL2}				-100	-400	
Low level input current 13/	I_{IL3}				-10	+10	
Low level input current 14/	I_{IL4}				-10	-165	
Transmitter/Receiver differential input resistance 15/ 16/ 17/	R_{IN}	75 kHz to 1.0 MHz	4,5,6	01,02,04	11		kΩ
				03	2		
Transmitter/Receiver differential input capacitance 15/ 16/ 17/	C_{IN}	DC to 1.0 MHz		All		10	pF
Receiver input threshold voltage	V_{TH}	Transformer coupled		All	650	860	mVpp
Receiver differential input voltage 15/ 16/	V_{IN}	DC to 1.0 MHz		01,02,04		40	Vpp
				03		11.5	
Transmitter differential output voltage	V_O	Transformer coupled, measured across the stub.		01,02,03	18	27	Vpp
				04	20	27	
Transmitter output rise and fall time	t_r, t_f			All	100	300	ns
Output offset voltage	V_{OS}			All	-250	+250	mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups 1/	Device type	Limits		Unit
					Min	Max	
Transmitter overshoot	V_{OVRSHT}	Transformer coupled, measured across the stub.	4,5,6	All	-900	+900	mV
Functional tests		V_{DD} = 4.5 V, V_{CC} = 4.5 V, 6/ V_{IL} = 0.4 V, V_{IH} = 2.7 V, for all device types V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02. See 4.3.1b.	7,8	All			pass/ fail
$\overline{IOEN}$ low pulse width (memory read) 18/	t_{pw1}	V_{DD} = 4.5 V, V_{CC} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, I_{OH1} = -400 µA, I_{OH2} = -3.4 mA, I_{OH3} = -6.8 mA, I_{OL1} = 6.8 mA, I_{OL2} = 2.0 mA, I_{OL3} = 4.0 mA, I_{OL4} = 3.4 mA for all device types. V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02. 6/ 19/	9,10,11	All	100	200	ns
$\overline{READYD}$ low pulse width (memory read) 18/	t_{pw2}				25	75	
$\overline{MEMOE}$ low pulse width (memory read) 18/	t_{pw3}				100	200	
$\overline{MEMWR}$ low pulse width (memory write) 20/	t_{pw4}				25	75	
$\overline{MEMENA\text{-}OUT}$ low pulse width (memory read) 18/	t_{pw5}				100	200	
$\overline{MEMENA\text{-}OUT}$ low pulse 20/ width (memory write)	t_{pw6}				100	200	
$\overline{BSCTRCV}$ low pulse width 21/	t_{pw7}				3	5	µs
$\overline{INT}$ low pulse width 22/	t_{pw8}				450	550	ns
$\overline{CMD\_STR}$ low pulse width (receive command) 23/	t_{pw9}				75	175	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups 1/	Device type	Limits		Unit
					Min	Max	
$\overline{\text{CMD\_STR}}$ low pulse width (transmit command) 24/	t_{pw10}	V_{DD} = 4.5 V, V_{CC} = 4.5 V, V_{IH} = 2.7 V, V_{IL} = 0.4 V, I_{OH1} = -400 µA, I_{OH2} = -3.4 mA, I_{OH3} = -6.8 mA, I_{OL1} = 6.8 mA, I_{OL2} = 2.0 mA, I_{OL3} = 4.0 mA, I_{OL4} = 3.4 mA for all device types. V_{EE} = -15 V for device types 01 and 04, and -12 V for device type 02. 6/ 19/	9,10,11	All	75	175	ns
$\overline{\text{RX\_DTA\_STR}}$ low pulse width 23/	t_{pw11}				75	175	
$\overline{\text{TX\_DTA\_STR}}$ low pulse (memory read) 18/	t_{pw12}				450	550	
$\overline{\text{INCMD}}$ low pulse width (receive word) 23/	t_{pw13}				47.5	52.5	µs
$\overline{\text{INCMD}}$ low pulse width (transmit word) 24/	t_{pw14}				48.7	53.7	

1/ All group A subgroup testing of the same temperature may be performed concurrently.

2/ Measured at the following pins:
Case X:
Device types 01-04: Pin 14.
Case Y:
Device types 01-04: Pin 28.
Case Z:
Device types 01-04: Pin 27.

3/ Measured at the following pins:
Case X:
Device types 01-04: Pins 58 and 77.
Case Y:
Device types 01-04: Pins 37 and 46.
Case Z:
Device types 01-04: Pins 36 and 43.

4/ Measured at the following pins:
Case X:
Device types 01, 02, and 04: Pins 18 and 39.
Case Y:
Device types 01, 02, and 04: Pins 36 and 45.
Case Z:
Device types 01-04: Pins 35 and 42.

5/ Measured at the following pins:
Case X:
Device types 01-04: Pins 12, 13, 16, 52, 53, 55, and 70.
Case Y:
Device types 01-04: Pins 24-27, 31, 32, and 60.
Case Z:
Device types 01-04: Pins 23-26, 30, 31, and 57.

TABLE I. Electrical performance characteristics - Continued.

6/ For device type 03, V_{CC} = 4.75 V, V_{DD} = 4.75 V.

7/ Measured at the following pins:
Case X:
Device types 01-04: Pins 30, 31, 68, 72, 73, and 75.
Case Y:
Device types 01-04: Pins 50, 54, 56, 61, 63, and 64.
Case Z:
Device types 01-04: Pins 47, 51, 53, 58, 60, and 61.

8/ Measured at the following pins:
Case X:
Device types 01-04: Pins 1-8, 22-29, 41-48, and 60-67.
Case Y:
Device types 01-04: Pins 2-17 and 65-80.
Case Z:
Device types 01-04: Pins 1-16 and 62-77.

9/ Measured at the following pins:
Case X:
Device types 01-04: Pins 12, 13, 16, 55, and 70.
Case Y:
Device types 01-04: Pins 24, 26, 31, 32, and 60.
Case Z:
Device types 01-04: Pins 23, 25, 30, 31, and 57.

10/ Measured at the following pins:
Case X:
Device types 01-04: Pins 52 and 53.
Case Y:
Device types 01-04: Pins 27 and 25.
Case Z:
Device types 01-04: Pins 24 and 26.

11/ Measured at the following pins:
Case X:
Device types 01-04: Pins 1-8, 15, 22-29, 30, 33-37, 41-48, 57, 60-67, 71, 74, and 76.
Case Y:
Device types 01-04: Pins 2-17, 30, 35, 48, 49, 51-53, 55, 57, 58, 63, and 65-80.
Case Z:
Device types 01-04: Pins 1-16, 29, 34, 44-46, 48, 50, 52, 54, 55, 60, and 62-77.

12/ Measured at the following pins:
Case X:
Device types 01-04: Pins 9-11 and 49-51.
Case Y:
Device types 01-04: Pins 18-23.
Case Z:
Device types 01-04: Pins 17-22.

13/ Measured at the following pins:
Case X:
Device types 01-04: Pins 17, 54, and 56.
Case Y:
Device types 01-04: Pins 29, 33, and 34.
Case Z:
Device types 01-04: Pins 28, 32, and 33.

TABLE I. Electrical performance characteristics - Continued.

14/ Measured at the following pins:
Case X:
Device types 01-04: Pins 32 and 69.
Case Y:
Device types 01-04: Pins 59 and 62.
Case Z:
Pins 56 and 59.

15/ Measured at the following pins:
Case X:
Device types 01-04: Pins 20, 40, 59, and 78.
Case Y:
Device types 01-04: Pins 39, 40, 43, and 44.
Case Z:
Device types 01-04: Pins 39-41.

16/ Parameter shall be tested as part of the initial characterization of this device and after design and process changes. Parameter shall be guaranteed to limits specified in table I for all lots not specifically tested.

17/ The test limits assume a 2 V rms balanced, differential, sinusoidal input. The applicable frequency range is 75 kHz to 1 MHz. The limits are applicable for both unpowered and powered conditions.

18/ Test limits based on the following test conditions:
- TRANSPARENT/BUFFERED_L input set to logic "1".
- SELECT_L input set to logic "0".
- MEM/REG_L input set to logic "1".
- RD/WR_L input set to logic "1".
- 250 ns active low pulse into STRBD_L.

19/ All timing parameters are measured at the 50 percent level of the waveform.

20/ Test limits based on the following test conditions:
- TRANSPARENT/BUFFERED-L input set to logic "1".
- SELECT_L input set to logic "0".
- MEM/REG_L input set to logic "1".
- RD/WR_L input set to logic "0".
- 250 ns active low pulse into STRBD_L.

21/ Test limits based on the following test conditions:
- DUT active in RT mode.
- BRO_ENA input set to logic "1".
-1553 command 1F R 01 01 is sent to DUT.

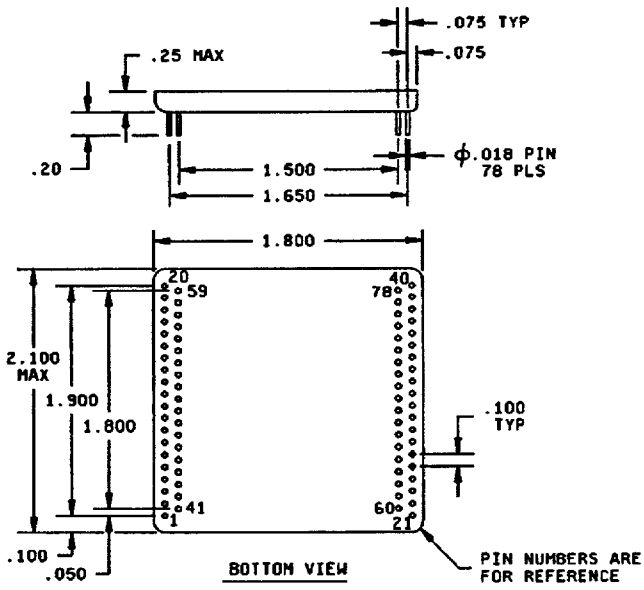
22/ Test limits based on the following test conditions:
- DUT active in RT mode.
- Interrupt mask register is programmed with a hex value of 0080 (interrupt on rt address parity error).
- The following sequence is input on the rt address inputs:
  1. rt address = 01 (rt address parity bit = 0).
  2. rt address = 00 (rt address parity bit = 0).
  3. rt address = 01 (rt address parity bit = 0).
  Note: interrupt pulse will occur in response to step 2.

23/ Test limits based on the following test conditions:
- DUT active in RT mode.
- rt address = 01 (rt address parity = 0).
- 1553 Command 01 R 01 01 is sent to DUT.

24/ Test limits based on the following test conditions:
- DUT active in RT mode.
- rt address = 01 (rt address parity = 0).
-1553 Command 01 T 01 01 is sent to DUT.

Device types 01 through 04

Case X



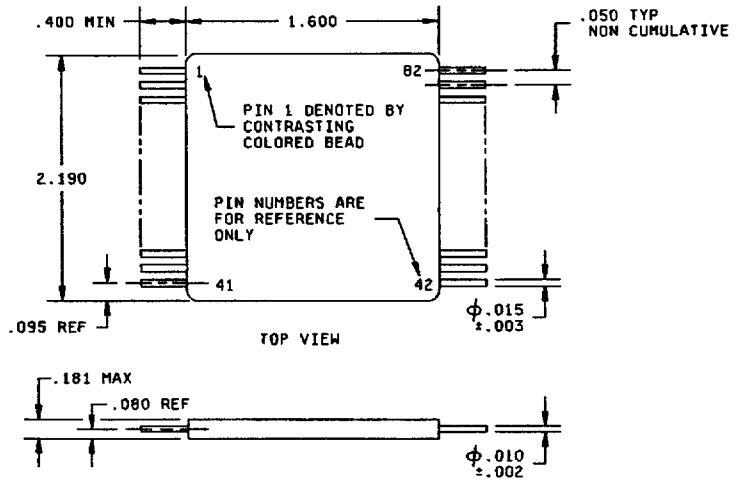
Inches	mm
.018	0.45
.050	1.27
.056	1.42
.075	1.91
.100	2.54
.25	6.4
1.500	38.10
1.650	41.91
1.800	45.72
1.900	48.26
2.100	53.34

NOTES:
1. Dimensions are in inches
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outlines.

Device types 01 through 04

Case Y



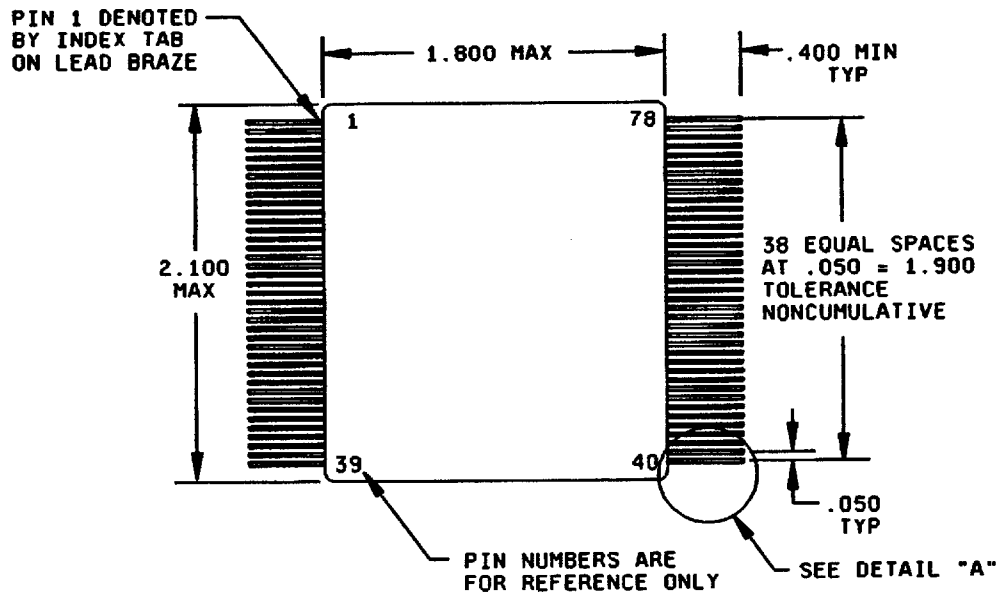
Inches	mm
.002	0.05
.003	0.08
.010	0.25
.015	0.38
.050	1.27
.080	2.03
.095	2.41
.181	4.60
.400	10.16
1.600	40.64
2.190	55.63

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

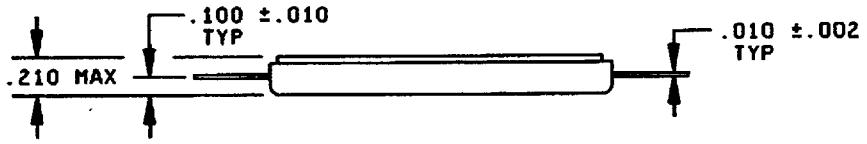
FIGURE 1. Case outlines - Continued.

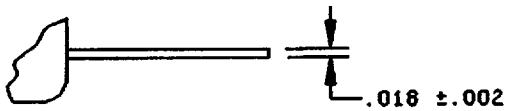
Device types 01 through 04

Case Z



Inches	mm
.002	0.05
.010	0.25
.018	0.46
.050	1.27
.100	2.54
.210	5.33
.400	10.16
1.800	45.72
1.900	48.26
2.100	53.34





DETAIL "A"

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outlines - Continued.

Device types	All		Device types	All	
Case outline	X	Y	Case outline	X	Y
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	D00	No connection	22	A01	RTAD4
2	D02	D00	23	A03	RTADP
3	D04	D01	24	A05	$\overline{\text{MSG\_ERROR}}$
4	D06	D02	25	A07	$\overline{\text{RX\_DTA\_STR}}$
5	D08	D03	26	A09	$\overline{\text{CMD\_STR}}$
6	D10	D04	27	A11	$\overline{\text{TX\_DTA\_STR}}$
7	D12	D05	28	A13	V_{DD}
8	D14	D06	29	A15	BRO_ENA
9	RTAD1	D07	30	$\overline{\text{MEMOE}}$/ADDR_LAT	TAG_CLK
10	RTAD0	D08	31	$\overline{\text{MEMENA-OUT}}$	RTFAIL
11	RTAD4	D09	32	CLOCK IN	$\overline{\text{BCSTRCV}}$
12	$\overline{\text{MSG\_ERROR}}$	D10	33	MEM/$\overline{\text{REG}}$	RTFLAG
13	$\overline{\text{CMD\_STR}}$	D11	34	$\overline{\text{STRBD}}$	ILLENA
14	V_{DD}	D12	35	TRANSP/$\overline{\text{BUFFERED}}$	TX_INH_B
15	TAG_CLK	D13	36	RD/$\overline{\text{WR}}$	V_{EE} (CH B) (see note)
16	$\overline{\text{BCSTRCV}}$	D14	37	$\overline{\text{SSFLAG}}$	V_{CC} (CH B)
17	ILLENA	D15	38	GNDA	GNDB
18	V_{EE} (CH B) (see note)	RTAD1	39	V_{EE} (CH A) (see note)	$\overline{\text{TX/RX-B}}$
19	GNDB	RTAD3	40	TX/RX-A	TX/RX-B
20	TX/RX-B	RTAD0	41	D01	No connection
21	LOGIC GND	RTAD2	42	D03	No connection

FIGURE 2. Terminal connections.

Device types	All		Device types	All	
Case outline	X	Y	Case outline	X	Y
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
43	D05	TX/RX-A	63	A06	MEMOE/ADDR_LAT
44	D07	$\overline{\text{TX/RX-A}}$	64	A08	$\overline{\text{MEMWR}}$
45	D09	V_{EE} (CH A) (see note)	65	A10	A15
46	D11	V_{CC} (CH A)	66	A12	A14
47	D13	GNDA	67	A14	A13
48	D15	TX_INH_A	68	$\overline{\text{MEMWR}}$	A12
49	RTAD3	$\overline{\text{SSFLAG}}$	69	$\overline{\text{MEMENA-IN}}$	A11
50	RTAD2	$\overline{\text{READYD}}$	70	$\overline{\text{INCMD}}$	A10
51	RTADP	RD/$\overline{\text{WR}}$	71	$\overline{\text{MSTRCLR}}$	A09
52	$\overline{\text{RX_DTA_STR}}$	$\overline{\text{SELECT}}$	72	$\overline{\text{INT}}$	A08
53	$\overline{\text{TX_DTA_STR}}$	TRANS/$\overline{\text{BUFFERED}}$	73	$\overline{\text{IOEN}}$	A07
54	BRO_ENA	$\overline{\text{IOEN}}$	74	$\overline{\text{SELECT}}$	A06
55	$\overline{\text{RTFAIL}}$	$\overline{\text{STRBD}}$	75	$\overline{\text{READYD}}$	A05
56	$\overline{\text{RTFLAG}}$	$\overline{\text{INT}}$	76	TX_INH_A	A04
57	TX_INH_B	MEM/$\overline{\text{REG}}$	77	V_{CC} (CH A)	A03
58	V_{CC} (CH B)	$\overline{\text{MSTRCLR}}$	78	$\overline{\text{TX/RX-A}}$	A02
59	$\overline{\text{TX/RX-B}}$	CLOCK IN	79	---	A01
60	A00	$\overline{\text{INCMD}}$	80	---	A00
61	A02	$\overline{\text{MEMENA-OUT}}$	81	---	LOGIC GND
62	A04	$\overline{\text{MEMENA-IN}}$	82	---	No connection

NOTE: For device type 03, no connection.

FIGURE 2. Terminal connections - Continued.

Device type	01 through 04				
Case outline	Z				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D00	27	V_{DD}	53	$\overline{INT}$
2	D01	28	SA/MC-3	54	MEM/$\overline{REG}$
3	D02	29	SA/MC-1	55	$\overline{MSTRCLR}$
4	D03	30	$\overline{THIS-RT}$	56	CLOCK-IN
5	D04	31	$\overline{BCSTRCV}$	57	$\overline{INCMD}$
6	D05	32	$\overline{RTPARERR}$	58	$\overline{MEMENA-OUT}$
7	D06	33	LMC	59	$\overline{MEMENA-IN}$
8	D07	34	T/$\overline{R}$	60	$\overline{MEMOE}$
9	D08	35	V_{EE} (CH B)	61	$\overline{MEMWR}$
10	D09	36	V_{CC} (CH B)	62	A15
11	D10	37	GNDB	63	A14
12	D11	38	$\overline{TX/RX-B}$	64	A13
13	D12	39	TX/RX-B	65	A12
14	D13	40	TX/RX-A	66	A11
15	D14	41	$\overline{TX/RX-A}$	67	A10
16	D15	42	V_{EE} (CH A)	68	A09
17	RTAD1	43	V_{CC} (CH A)	69	A08
18	RTAD3	44	GNDA	70	A07
19	RTAD0	45	$\overline{TAGEN}$	71	A06
20	RTAD2	46	$\overline{EXTLD}$	72	A05
21	RTAD4	47	$\overline{READYD}$	73	A04
22	RTADP	48	RD/$\overline{WR}$	74	A03
23	$\overline{ILLCMD}$	49	$\overline{SELECT}$	75	A02
24	SA/MC-2	50	$\overline{EXTEN}$	76	A01
25	SA/MC-0	51	$\overline{IOEN}$	77	A00
26	SA/MC-4	52	$\overline{STRBD}$	78	GND

FIGURE 2. Terminal connections - Continued.

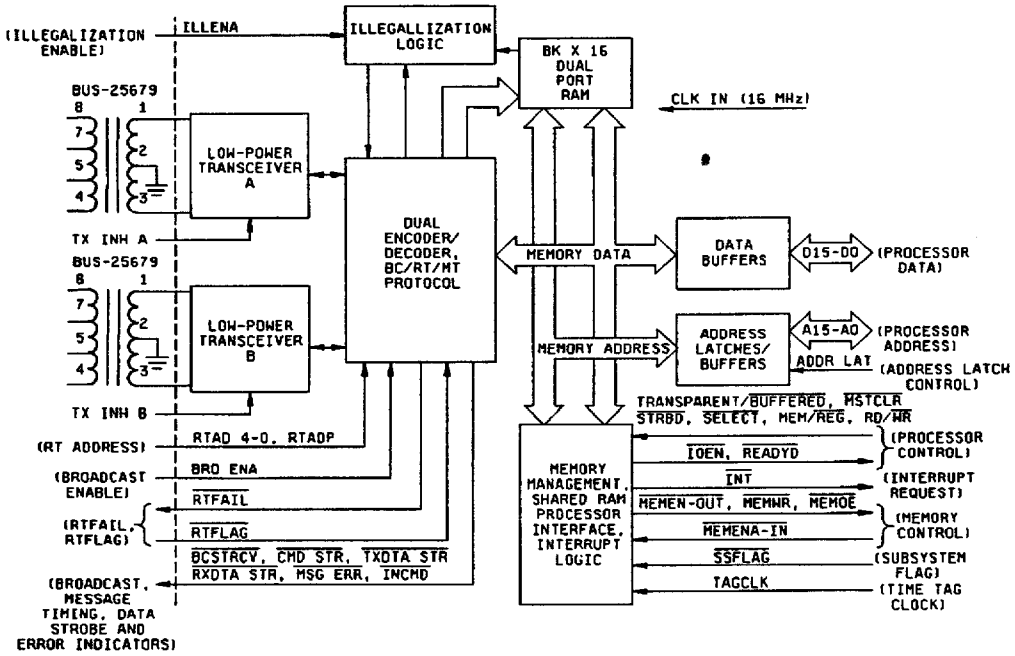


FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91734
		REVISION LEVEL A	SHEET 18

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3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DESC-ECT shall affirm that the manufacturer's product meets the requirements of MIL-H-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-H-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-H-38534.

4.2 Screening. Screening shall be in accordance with MIL-H-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-H-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-H-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendors test tape and shall be maintained and available from the approved source of supply.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-H-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-H-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DESC-EC or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-H-38534.

TABLE II. Electrical test requirements.

MIL-H-38534 test requirements	Subgroups (in accordance with MIL-H-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6, 7,8,9,10,11
Final electrical test parameters	1*,2,3,4,5,6, 7,8,9,10,11
Group A test requirements	1,2,3,4,5,6, 7,8,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6, 7,8,9,10,11
MIL-STD-883, Group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

*PDA applies to subgroup 1
**When applicable to this standardized military drawing, the subgroups shall be defined.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-H-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-H-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5374.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DESC-EC and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	I/O	Description
D00	I/O	Data bus bit 0 (LSB).
D02	I/O	Data bus bit 2.
D04	I/O	Data bus bit 4.
D06	I/O	Data bus bit 6.
D08	I/O	Data bus bit 8.
D10	I/O	Data bus bit 10.
D12	I/O	Data bus bit 12.
D14	I/O	Data bus bit 14.
RTAD1	I	Remote terminal address bit 1.
RTAD0	I	Remote terminal address bit 0 (LSB).
RTAD4	I	Remote terminal address bit 4 (MSB).
$\overline{\text{MSG\_ERROR}}$	O	In BC or RT modes, will be low following a word or format error and remain low until the start of the next message.
$\overline{\text{CMD\_STR}}$	O	In RT/transparent mode, this output will pulse low for nominally 125 ns when a received Command Word is on D15-D0.
V_{DD}	I	+5 V supply input for digital logic section.
TAG_CLK	I	External Time Tag Clock Input, for BC/RT modes.
$\overline{\text{BCSTRSV}}$	O	Broadcast received. Indicates current command is a 1553 broadcast command.
ILLENA	O	Illegalization Enable. If logic 1, designates shared RAM addresses 0300-03FF to be dedicated for command illegalization in RT mode. If logic 0, illegalization is disabled.
V_{EE} (CH B)	I	Input power supply connection for the B channel transceiver. -15 V for device type 01, -12 V for device type 02. For device type 03 no connection (NC).
GNDB	-	Ground B. Power supply return connection for the B channel transceiver.
TX/RX-B	I/O	Transmit/receive transceiver-B. Input/output to the coupling transformer that connects to the B channel of the 1553 bus.
LOGIC GND	-	Logic ground. Power supply return for the digital logic section.
A01	I/O	Address bit 1.
A03	I/O	Address bit 3.
A05	I/O	Address bit 5.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
A07	I/O	Address bit 7.
A09	I/O	Address bit 9.
A11	I/O	Address bit 11.
A13	I/O	Address bit 13.
A15	I/O	Address bit 15.
$\overline{\text{MEMOE}}$/ADDR_LAT	O/I	Memory Output Enable/Address Latch. In transparent mode, used to enable data outputs for external RAM. In buffered mode, input used to configure the internal address buffers.
$\overline{\text{MEMENA-OUT}}$	O	Memory enable out. Logic 0 output enables external RAM. Used with MEMOE to read data or with MEMWR to write data into external RAM.
CLOCK IN	I	Clock input. 16 MHz TTL clock.
MEM/$\overline{\text{REG}}$	I	Memory/register. Input from CPU to select memory or register data transfer.
$\overline{\text{STRBD}}$	I	Strobe data. Used in conjunction with $\overline{\text{SELECT}}$ to initiate a data transfer cycle to/from CPU.
TRANSP/$\overline{\text{BUFFERED}}$	I	Used to select between the transparent and buffered modes for the host processor interface.
D11	I/O	Data bus bit 11.
D13	I/O	Data bus bit 13.
D15	I/O	Data bus bit 15 (MSB).
RTAD3	I	Remote terminal address bit 3.
RTAD2	I	Remote terminal address bit 2.
RTADP	I	Remote terminal address parity input.
$\overline{\text{RX\_DTA\_STR}}$	O	In RT/transparent mode, this output will pulse low for nominally 125 ns when a received Data Word is on D15-D0.
$\overline{\text{TX\_DTA\_STR}}$	O	In RT/transparent mode, this output will pulse low for nominally 500 ns when a Data Word to be transmitted on the 1553 bus is required to be on D15-D0.
BRO_ENA	I	Broadcast Enable. If logic 1, device will recognize RT Address 31 as the broadcast address. If logic 0, RT Address 31 may be used as a discrete RT Address.
$\overline{\text{RTFAIL}}$	O	In RT mode, is updated following every valid, nonbroadcast message.
$\overline{\text{RTFLAG}}$	I	Active low input used to control RT FLAG bit in RT Status Word.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
TX_INH_B	I	The 1553 transmitter may be inhibited by asserting the respective TX_INH input(s) high.
RD/$\overline{WR}$	I	Read/write. Input from the CPU which defines the data bus transfer as a read or write operation.
$\overline{SSFLAG}$	I	If this input is asserted low, the Subsystem Flag bit will be set in the device's RT Status Word.
GNDA	-	Ground A. Power supply return connection for the A channel transceiver.
V_{EE} (CH A)	I	Input power supply connection for the A channel transceiver. -15 V for device type 01, -12 V for device type 02. For device type 03 no connection (NC).
TX/RX-A	I/O	Transmit receive transceiver-A. Input/output to the coupling transformer that connects to the A channel of the 1553 bus.
D01	I/O	I/O data bus bit 1.
D03	I/O	Data bus bit 3.
D05	I/O	Data bus bit 5.
D07	I/O	Data bus bit 7.
D09	I/O	Data bus bit 9.
V_{CC} (CH B)	I	+5 V power supply connection for the B channel transceiver.
$\overline{TX/RX-B}$	I/O	Transmit/receive transceiver-B. Inverted I/O to coupling transformer that connects to channel B of the 1553 bus.
A00	I/O	Address bit 0 (LSB).
A02	I/O	Address bit 2.
A04	I/O	Address bit 4.
A06	I/O	Address bit 6.
A08	I/O	Address bit 8.
A10	I/O	Address bit 10.
A12	I/O	Address bit 12.
A14	I/O	Address bit 14.
$\overline{MEMWR}$	O	Memory write. Output pulse to write data into memory.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{MEMENA-IN}}$	I	Memory enable in. Enables internal RAM only; connect directly to MEMENA-OUT.
$\overline{\text{INCMD}}$	O	In command. Indicates BC to RTU currently in message transfer sequence.
$\overline{\text{MSTRCLR}}$	I	Master clear. Power-on reset from CPU.
$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
$\overline{\text{IEON}}$	O	Input/output enable. Output to enable external buffers/latches connecting the hybrid to the address/data bus.
$\overline{\text{SELECT}}$	I	Select. Input from the CPU. When active selects device for operation.
$\overline{\text{READYD}}$	O	Ready data. When active indicates data has been received from, or is available to, the CPU.
TX_INH_A	I	The 1553 Channel A transmitter may be inhibited by asserting the respective TX_INH input(s) high.
V_{CC} (CH A)	I	+5 V input power supply connection for the channel A transceiver.
$\overline{\text{TX/RX-A}}$	I/O	Transmit/receive transceiver-A. Inverted I/O to the coupling transformer that connects to channel A of the 1553 bus.