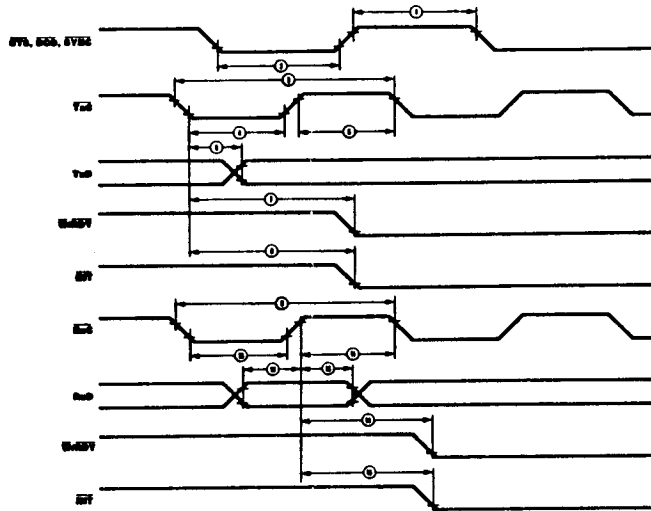
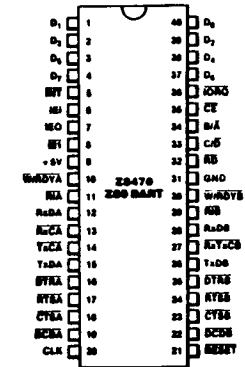


Z08470 Customer  
Procurement Spec (CPS)



**GENERAL DESCRIPTION**

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.



40-Pin Dual-In-Line Package (DIP),  
Pin Assignments

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are tested, except those which are  
characterized or guaranteed by  
design.

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(MARCOM) DC2847

DOCUMENT CONTROL  
MASTER

**DC CHARACTERISTICS**

Symbol	Parameter	Min	Max	Unit	Test Condition
V <sub>IL</sub> C	Clock Input Low Voltage	-0.3 <sup>a</sup>	+0.45 <sup>a</sup>	V	
V <sub>IH</sub> C	Clock Input High Voltage	V <sub>CC</sub> - 0.6 <sup>a</sup>	+5.5 <sup>a</sup>	V	
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>a</sup>	+0.8 <sup>a</sup>	V	
V <sub>IH</sub>	Input High Voltage	+2.0 <sup>a</sup>	+5.5 <sup>a</sup>	V	
V <sub>OL</sub>	Output Low Voltage		+0.4 <sup>a</sup>	V	I <sub>OL</sub> = 2.0 mA
V <sub>OH</sub>	Output High Voltage	+2.4 <sup>a</sup>		V	I <sub>OH</sub> = -250 μA
I <sub>IL</sub>	Input/3-State Output Leakage Current	-10 <sup>b</sup>	+10 <sup>b</sup>	μA	0.4 < V <sub>IN</sub> < 2.4V
I <sub>IPB</sub>	R <sub>I</sub> Pin Leakage Current	-40 <sup>b</sup>	+10 <sup>b</sup>	μA	0.4 < V <sub>IN</sub> < 2.4V
I <sub>CC</sub>	Power Supply Current		100 <sup>b</sup>	mA	

V<sub>L</sub> = 0°C to 70°C; V<sub>CC</sub> = -0.5 V<sub>CC</sub>

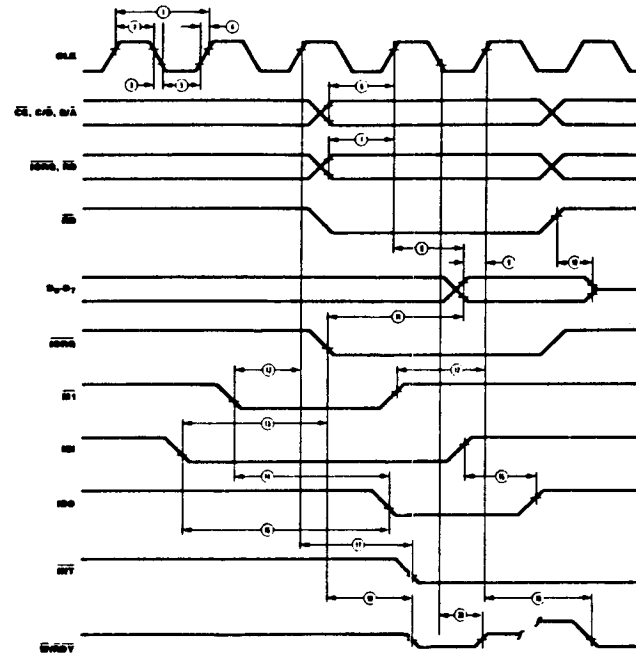
- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization

**AC CHARACTERISTICS\***

Number	Symbol	Parameter	Z80-4 DART		Z80-6 DART	
			Min	Max	Min	Max
1	T <sub>c</sub> C	Clock Cycle Time	250 <sup>a</sup>	4000 <sup>a</sup>	165 <sup>a</sup>	4000 <sup>a</sup>
2	T <sub>w</sub> Ch	Clock Width (High)	105 <sup>a</sup>	2000 <sup>a</sup>	70 <sup>a</sup>	2000 <sup>a</sup>
3	T <sub>f</sub> C	Clock Fall Time		30 <sup>a</sup>		15 <sup>a</sup>
4	T <sub>r</sub> C	Clock Rise Time		30 <sup>a</sup>		15 <sup>a</sup>
5	T <sub>w</sub> Cl	Clock Width (Low)	105 <sup>a</sup>	2000 <sup>a</sup>	70 <sup>a</sup>	2000 <sup>a</sup>
6	T <sub>s</sub> AD(C)	CE, C/Σ, B/A to Clock ↑ Setup Time	145 <sup>b</sup>		80 <sup>b</sup>	
7	T <sub>s</sub> CS(C)	IORC, RD to Clock ↑ Setup Time	115 <sup>b</sup>		80 <sup>b</sup>	
8	T <sub>d</sub> C(DO)	Clock ↑ to Data Out Delay		220 <sup>b</sup>		150 <sup>b</sup>
9	T <sub>d</sub> C(C)	Data In to Clock ↑ Setup (Write or M1 Cycle)	50 <sup>b</sup>		30 <sup>b</sup>	
10	T <sub>d</sub> RD(DOz)	RD ↑ to Data Out Float Delay		110 <sup>c</sup>		90 <sup>c</sup>
11	T <sub>d</sub> RO(DO)	IORC ↓ to Data Out Delay (NTACK Cycle)		180 <sup>c</sup>		100 <sup>c</sup>
12	T <sub>s</sub> M1(C)	M1 to Clock ↑ Setup Time	90 <sup>b</sup>		75 <sup>b</sup>	
13	T <sub>s</sub> IE(EO)	IE1 to IORC ↓ Setup Time (NTACK Cycle)	140 <sup>c</sup>		120 <sup>c</sup>	
14	T <sub>d</sub> M1(EO)	M1 ↓ to IE0 ↓ Delay (interrupt before M1)		180 <sup>c</sup>		180 <sup>c</sup>
15	T <sub>d</sub> IE(EOz)	IE1 ↑ to IE0 ↓ Delay (after ED decode)		100 <sup>c</sup>		70 <sup>c</sup>
16	T <sub>d</sub> IE(EO)	IE1 ↓ to IE0 ↓ Delay		100 <sup>b</sup>		70 <sup>b</sup>
17	T <sub>d</sub> C(NT)	Clock ↑ to INT ↓ Delay		200 <sup>b</sup>		150 <sup>b</sup>
18	T <sub>d</sub> OR(WRRW)	IORC ↓ or CE ↓ to W/RDY ↓ Delay (Wait Mode)		210 <sup>c</sup>		175 <sup>c</sup>
19	T <sub>d</sub> C(WRR)	Clock ↑ to W/RDY ↓ Delay (Ready Mode)		120 <sup>b</sup>		100 <sup>c</sup>
20	T <sub>d</sub> C(WRRz)	Clock ↓ to W/RDY Float Delay (Wait Mode)		130 <sup>c</sup>		110 <sup>c</sup>

\*Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization



**AC CHARACTERISTICS (Continued)**

Number	Symbol	Parameter	Z80-4 DART		Z80-6 DART		Notes*
			Min	Max	Min	Max	
1	T <sub>w</sub> Ph	Pulse Width (High)	200 <sup>c</sup>		200 <sup>c</sup>		2
2	T <sub>w</sub> Pl	Pulse Width (Low)	200 <sup>c</sup>		200 <sup>c</sup>		2
3	T <sub>c</sub> T <sub>c</sub>	ΣC Cycle Time	400 <sup>c</sup>	∞ <sup>c</sup>	330 <sup>c</sup>	∞ <sup>c</sup>	2
4	T <sub>w</sub> T <sub>c</sub> l	ΣC Width (Low)	180 <sup>c</sup>	∞ <sup>c</sup>	100 <sup>c</sup>	∞ <sup>c</sup>	2
5	T <sub>w</sub> T <sub>c</sub> h	ΣC Width (High)	180 <sup>c</sup>	∞ <sup>c</sup>	100 <sup>c</sup>	∞ <sup>c</sup>	2
6	T <sub>d</sub> T <sub>c</sub> (RD)	ΣC ↓ to RD Delay		300 <sup>b</sup>		220 <sup>b</sup>	2
7	T <sub>d</sub> T <sub>c</sub> C(WRR)	ΣC ↓ to W/RDY ↓ Delay (Ready Mode)	5 <sup>c</sup>	9 <sup>c</sup>	5 <sup>c</sup>	9 <sup>c</sup>	1
8	T <sub>d</sub> T <sub>c</sub> C(INT)	ΣC ↓ to INT ↓ Delay	5 <sup>c</sup>	9 <sup>c</sup>	5 <sup>c</sup>	9 <sup>c</sup>	1
9	T <sub>c</sub> R <sub>x</sub> C	R <sub>x</sub> C Cycle Time	400 <sup>c</sup>	∞ <sup>c</sup>	330 <sup>c</sup>	∞ <sup>c</sup>	2
10	T <sub>w</sub> R <sub>x</sub> Cl	R <sub>x</sub> C Width (Low)	180 <sup>c</sup>	∞ <sup>c</sup>	100 <sup>c</sup>	∞ <sup>c</sup>	2
11	T <sub>w</sub> R <sub>x</sub> Ch	R <sub>x</sub> C Width (High)	180 <sup>c</sup>	∞ <sup>c</sup>	100 <sup>c</sup>	∞ <sup>c</sup>	2
12	T <sub>s</sub> R <sub>x</sub> D(R <sub>x</sub> C)	R <sub>x</sub> D to R <sub>x</sub> C ↑ Setup Time (x1 Mode)	0 <sup>c</sup>		0 <sup>c</sup>		2
13	T <sub>h</sub> R <sub>x</sub> D(R <sub>x</sub> C)	R <sub>x</sub> D Hold Time (x1 Mode)	140 <sup>c</sup>		100 <sup>c</sup>		2
14	T <sub>d</sub> R <sub>x</sub> C(WRR)	R <sub>x</sub> C ↑ to W/RDY ↓ Delay (Ready Mode)	10 <sup>c</sup>	13 <sup>c</sup>	10 <sup>c</sup>	13 <sup>c</sup>	1
15	T <sub>d</sub> R <sub>x</sub> C(INT)	R <sub>x</sub> C ↑ to INT ↓ Delay	10 <sup>c</sup>	13 <sup>c</sup>	10 <sup>c</sup>	13 <sup>c</sup>	1

\* In all modes, the System Clock rate must be at least five times the maximum data rate. RESET must be active a minimum of one complete clock cycle.

1 Units equal to System Clock Periods.

2 Units in nanoseconds (ns).

- a Tested
- b Guaranteed by Design
- c Guaranteed by Characterization