

Description

The μ PD43254B is a 65,536-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μ PD43254B a high-speed device that requires very low power and no clock or refreshing.

The μ PD43254B is available in standard 24-pin plastic DIP and SOJ packaging.

Features

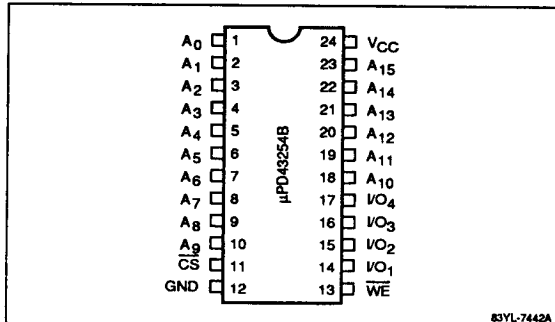
- 65,536-word x 4-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
 - 140 mA max (active)
 - 2 mA max (standby)
- Standard 24-pin plastic DIP and SOJ packaging

Ordering Information

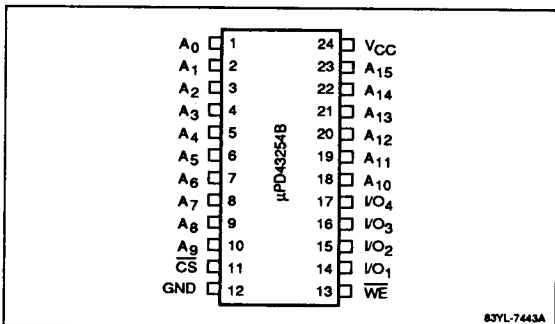
Part Number	Access Time (max)	Package
μ PD43254BCR-15	15 ns	24-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μ PD43254BLA-15	15 ns	24-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configurations

24-Pin Plastic DIP



24-Pin Plastic SOJ



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Pin Identification

Symbol	Function
A ₀ - A ₁₅	Address inputs
I/O ₁ - I/O ₄	Data inputs and outputs
CS	Chip select
WE	Write enable
GND	Ground
V _{CC}	+ 5-volt power supply

Supply voltage, V_{CC}	- 0.5 to + 7.0 V
Input and output voltages, V_{IN} (Note 1)	- 0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to + 70°C
Storage temperature, T_{STG}	- 55 to + 125°C
Power dissipation, P_D	1.0 W

Parameter	Symbol	Min	Max	Unit
Input capacitance	C _{IN}		6	pF
Output capacitance	C _{DOUT}		8	pF

[illegible]

DC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	-2		2	μA	$V_{IN} = 0 \text{ V to } V_{CC}$
Output leakage current	I_{LO}	-2		2	μA	$V_{OUT} = 0 \text{ V to } V_{CC}$; $\overline{CS} = V_{IH}$
Standby supply current	I_{SB}			30	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$; $V_{IN} \leq 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0 \text{ mA}$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0 \text{ mA}$

AC Characteristics

$T_A = 0 \text{ to } +70^\circ\text{C}$; $V_{CC} = +5.0 \text{ V} \pm 10\%$

Parameter	Symbol	μPD43254B-15		μPD43254B-20		μPD43254B-25		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Read Operation									
Operating supply current	I _{CC}		140		120		120	mA	$\overline{CS} = V_{IL}; I_{DOUT} = 0 \text{ mA}$
Read cycle time	t _{RC}	15		20		25		ns	(Note 2)
Address access time	t _{AA}		15		20		25	ns	
Chip select access time	t _{ACS}		15		20		25	ns	
Output hold from address change	t _{OH}	3		3		3		ns	
Chip selection to output in low-Z	t _{CLZ}	3		3		3		ns	(Note 3)
Chip deselection to output in high-Z	t _{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Write Operation									
Write cycle time	t _{WC}	15		20		25		ns	(Note 2)
Chip select to end of write	t _{CW}	13		15		20		ns	
Address valid to end of write	t _{AW}	13		15		20		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	12		14		18		ns	
Write recovery time	t _{WR}	0		0		0		ns	
Data valid to end of write	t _{DW}	10		12		14		ns	
Data hold time	t _{DH}	0		0		0		ns	
Write enable to output in high-Z	t _{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Output active from end of write	t _{OW}	0		0		0		ns	(Note 3)

Notes:

- (1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.
- (2) All read cycle timings are referenced from the last valid address to the first transitioning address.

- (3) Transition is measured at $\pm 200 \text{ mV}$ from steady-state voltage with the load shown in figure 2.
- (4) Transition is measured at $V_{OL} + 200 \text{ mV}$ and $V_{OH} - 200 \text{ mV}$ with the load shown in figure 2.

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Figure 1. Output Load

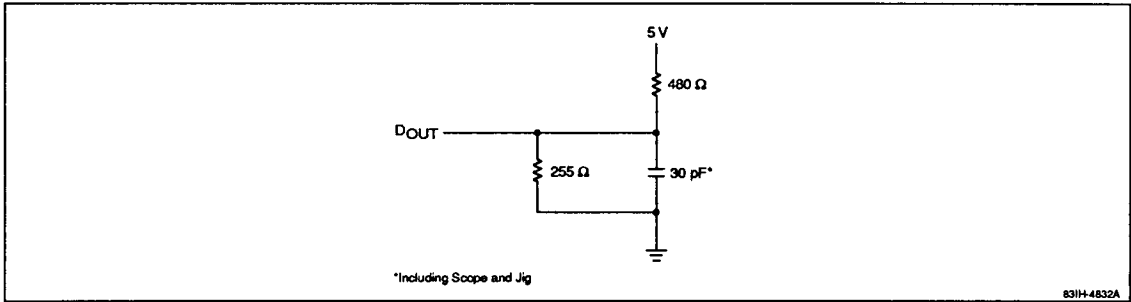
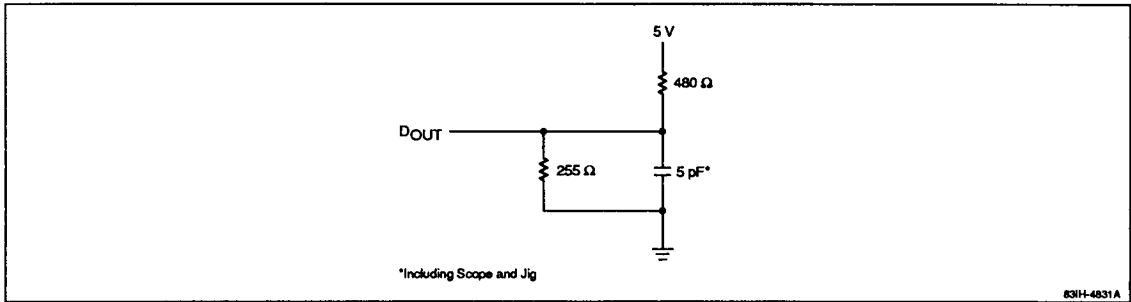
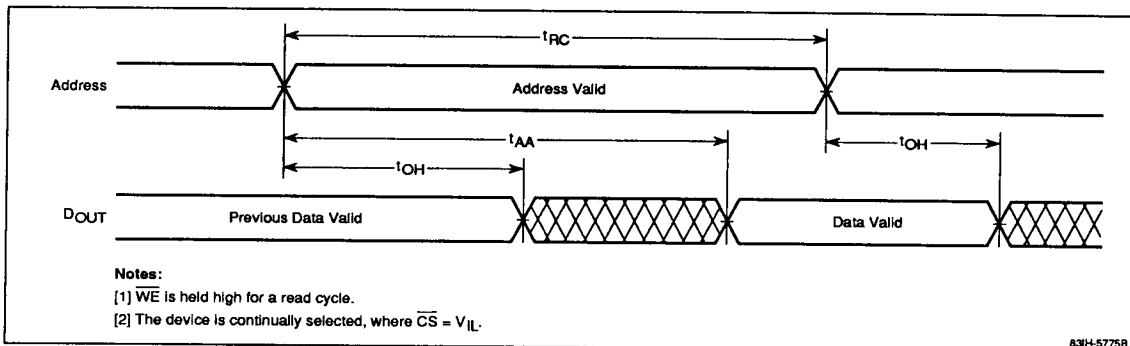


Figure 2. Output Load for t_{CHZ} , t_{CLZ} , t_{WHZ} , and t_{OW}

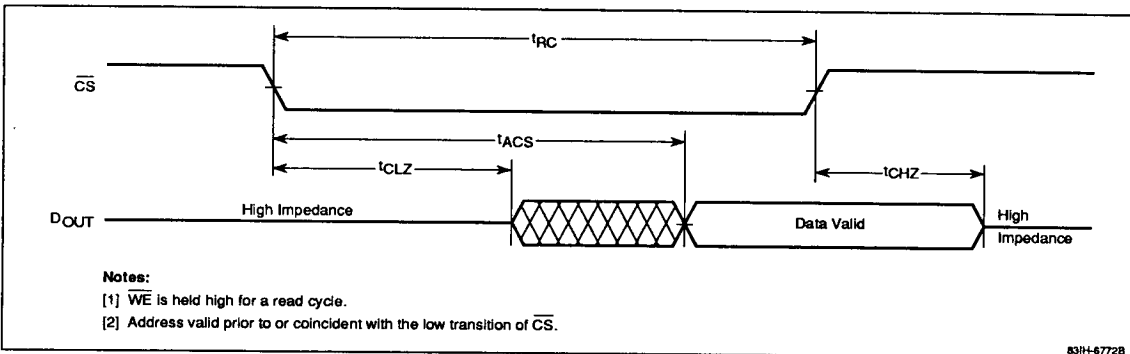


Timing Waveforms

Address Access Cycle

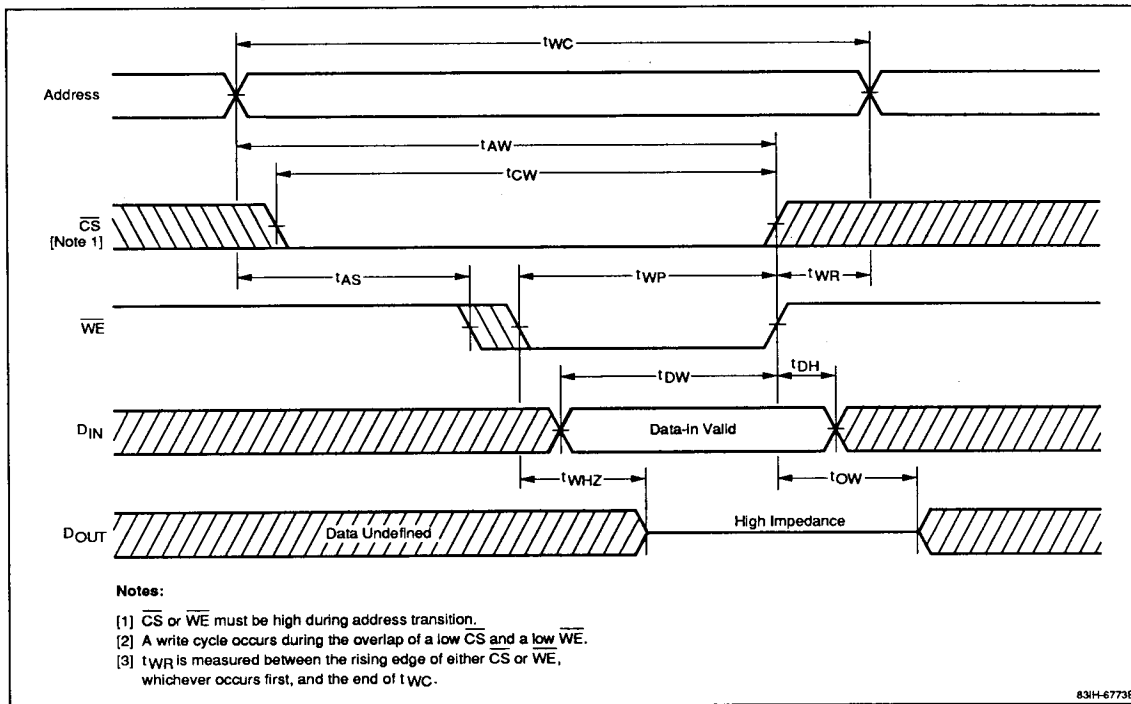


Chip Select Access Cycle



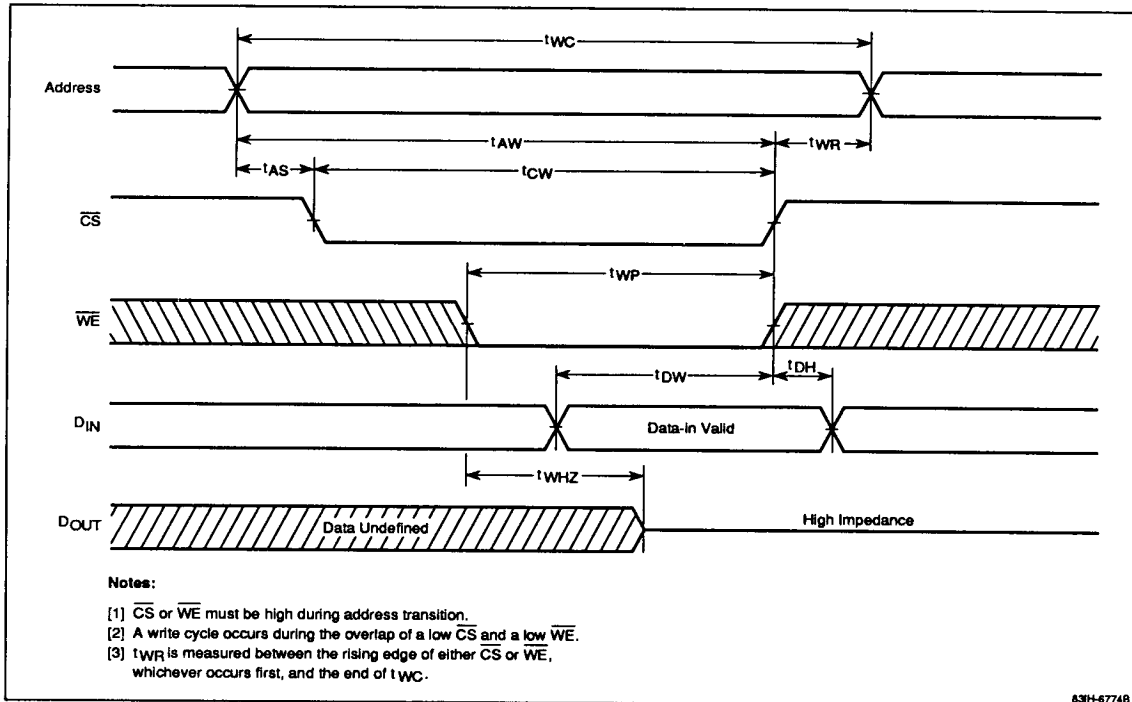
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Timing Waveforms (cont)

 $\overline{WE}$ -Controlled Write Cycle

Timing Waveforms (cont)

$\overline{CS}$ -Controlled Write Cycle



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