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MIXED TECHNOLOGY PUMA

PUMA 2US2500

Issue 4.0 : October 1995

Description

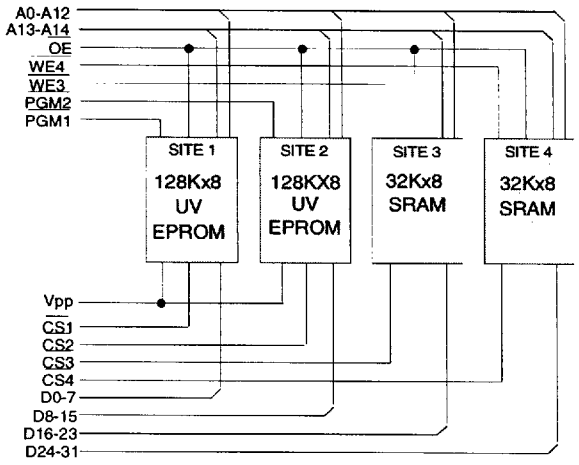
The PUMA 2US2500 is a Mixed Technology Puma 2 Module comprising of 2 x 128K8 UVEPROM's and 2 x 32K8 SRAMS. The device is user configurable as 8 and 16 bit wide. The UVEPROM is available in speeds ranging from 100 to 250ns and has Fast Page Programming of 14 sec (typ). The SRAM has speeds ranging from 85 to 150ns and has a completely static operation. Both devices have inputs and outputs which are TTL compatible.
May be screened in accordance with MIL-STD-883.

2,097,152 bit UVEPROM and 524,288 bit SRAM

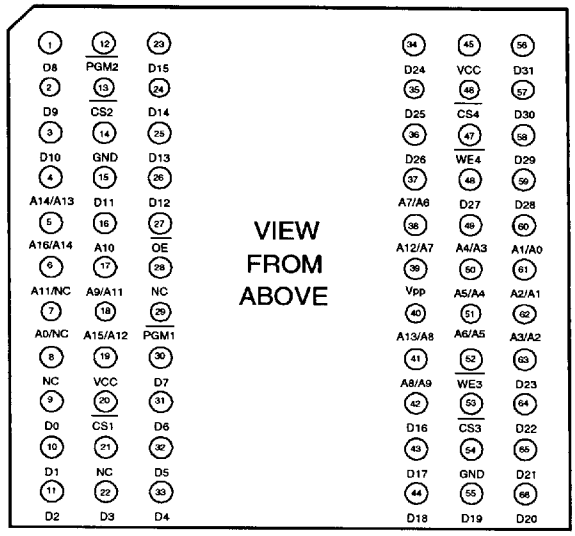
Features

- Output user configurable as 8 / 16 bit wide.
- Average Power UVEPROM 315 / 585 mW (max).
  SRAM 425 / 805 mW (max).
- Standby Power 410 µW (typical) - CMOS levels.
- On-board decoupling capacitors.
- All Inputs and Outputs TTL Compatible.
- *EPROM Data* Access times of 100 to 250 ns.
  Fast Page Programming of 14 sec (typ).
  Programming Voltage of 12.5V±0.3V
- *SRAM Data* Access times of 85 to 150 ns.
  Completely Static Operation

Block Diagram



Pin Definition



Note: Some pins in the above table have been allocated two functions. Where this is the case, the functions specified refer to the EPROM pinout and SRAM pinout respectively; for example, pin 41, allocated A8/A9, connects to A8 on the EPROMs, and to A9 on the SRAMs.

Pin Functions

A0~A16	Address Inputs	**D0~D31**	Data Input/Output
CS1~4	Chip Selects	**OE**	Output Enable
WE3~4	Write Enables	**PGM1~2**	Programming Enables
V_{PP}	Programming Voltage	**V_{CC}**	Power (+5V)
GND	Ground		

DC OPERATING CONDITIONS

The operation of the UV EPROMs is obviously different from the operation of the SRAMs. For this reason the technical data which follows is separated into an EPROM section (pages 3 to 10) and a SRAM section (pages 11 to 15), with both 8 and 16 bit modes covered for both types of memory. Note that the DC Characteristics in both sections are for the ***entire*** module, irrespective of whether they are in the EPROM part or the SRAM part.

Absolute Maximum Ratings (1)

Temperature Under Bias	T_{OPR}	-55 to +125 °C
Storage Temperature	T_{STG}	-65 to +150 °C
Voltage on Any Pin with respect to GND(2)	V_{IN}	-0.6 to +7.0 V
Voltage on V_{PP} pin with respect to GND(3)	V_{PT}	-2.0 to +14.0 V

Notes (1) Stresses above those listed may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_{IN} and V_{PT} minimum may be -1.0V for pulse width - 50ns.

Recommended Operating Conditions

			min	*typ*	*max*	
Supply Voltage		V_{CC}	4.75	5.0	6.25	V
Programming Voltage	Read	V_{PPR}	4.75	5.0	5.25	V
	Program	V_{PPW}	12.2	12.5	12.8	V
Input High Voltage	TTL	V_{IH}	2.2	-	V_{CC}+1.0	V
	CMOS	V_{IHC}	0.7 V_{CC}	-	V_{CC}+1.0	V
Input Low Voltage	TTL	V_{IL}	-0.3	-	0.8	V
	CMOS	V_{ILC}	-0.3	-	0.3	V
Operating Temperature		T_A	0	-	70	°C
		T_{AI}	-40	-	85	°C (-**I** suffix)
		T_{AM}	-55	-	125	°C (-**M**, **MB** suffix)

Capacitance (T_A=25°C, f=1MHz) These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	A1~10, A12~16, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	54	pF
	A0, A11	C_{IN2}	V_{IN}=0V	-	40	pF
	$\overline{CS1~2}$, $\overline{PGM1~2}$	C_{IN3}	V_{IN}=0V	-	40	pF
	$\overline{CS3~4}$, $\overline{WE3~4}$	C_{IN4}	V_{IN}=0V	-	34	pF
Output Capacitance	D0~ D15	C_{OUT1}	V_{OUT}=0V	-	25	pF
	D16~D31	C_{OUT2}	V_{OUT}=0V	-	15	pF

UV EPROM DATA SECTION

DC Electrical Characteristics

Read (T_A = -55°C to +125°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter		Symbol	Test Condition	min	typ(2)	max	Unit
I/P Leakage Current	A0~A16, $\overline{OE}$	I_{LI1}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}, V_{PP} = V_{PPL}	-	-	±8	µA
	$\overline{PGM1\sim2}$, $\overline{CS1\sim2}$	I_{LI2}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±4	µA
Output Leakage Current	D0~D15	I_{LO1}	V_{CC} = V_{CC} max, V_{OUT} = 0V or V_{CC}	-	-	±2	µA
V_{PP} Leakage Current		I_{PPS}	V_{PP} - V_{CC}	-	2	40	µA
V_{CC} Operating Current	16bit	I_{CC16}	$\overline{CS}$(6) = V_{IL}, I_{OUT} = 0mA, Inputs Static.	-	-	66	mA
V_{CC} Average Read Current	16bit	I_{CCO16}	$\overline{CS}$(6) = V_{IL}, I_{OUT} = 0mA, f = 5MHz	-	-	106	mA
	8bit	I_{CCO8}	As above	-	-	57	mA
V_{CC} Average Read Current	16bit	I_{CCA16}	$\overline{CS}$(6) = V_{IL}, I_{OUT} = 0mA, f = 10MHz	-	-	146	mA
	8bit	I_{CCA8}	As above	-	-	77	mA
Standby Supply Current	TTL	I_{SB1}	$\overline{CS}$(6) = V_{IH}	-	-	8	mA
	CMOS	I_{SB2}	$\overline{CS}$(6) = V_{IHC}, $V_{ILC} \geq V_{IN} \geq V_{IHC}$	-	-	4	mA
V_{PP} Voltage During Read		V_{PPL}	Programming is inhibited if V_{PP} = V_{PPL}	4.75	-	5.25	V
Output Low Voltage	D0-D15	V_{OL1}	I_{OL} = 2.1mA.	-	-	0.45	V
Output High Voltage	TTL loading	V_{OH1}	I_{OH} = -1.0mA. (D0~D15)	2.4	-	-	V
	CMOS loading	V_{OH2}	I_{OH} = -100µA. (D0~D15)	V_{CC}-0.7	-	-	V

Program (T_A = 25°C ± 5°C, V_{CC} = 6.0V ± 0.25, V_{PP} = 12.5V ± 0.3V) (7)

Parameter		Symbol	Test Condition	min	typ(2)	max	Unit
I/P Leakage Current	A0~A16, $\overline{OE}$	I_{LI1}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}, V_{PP} = V_{PPL}	-	-	±8	µA
	$\overline{PGM1\sim2}$, $\overline{CS1\sim2}$	I_{LI2}	V_{CC} = V_{CC} max, V_{IN} = 0V or V_{CC}	-	-	±4	µA
Output Leakage Current	D0~D15	I_{LO}	V_{CC} = V_{CC} max, V_{OUT} = 0V or V_{CC}	-	-	±2	µA
V_{CC} Program Current	16bit	I_{CCP16}	$\overline{CS}$(1) = $\overline{PGM}$(1) = V_{IL}, Program in progress	-	-	66	mA
	8bit	I_{CCP8}	As above	-	-	37	mA
V_{PP} Byte Program Current	16bit	I_{PPB16}	V_{PP} = V_{PPH}, Byte Program in progress	-	-	80	mA
	8bit	I_{PPB8}	As above	-	-	40	mA
V_{PP} Page Program Current	16bit	I_{PPP16}	V_{PP} = V_{PPH}, Page Program in progress	-	-	100	mA
	8bit	I_{PPP8}	As above	-	-	50	mA
V_{CC} Voltage During Program		V_{CCP}		5.75	6.0	6.25	V
V_{PP} Voltage During Program		V_{PPH}		12.2	12.5	12.8	V
Output Low Voltage	D0~D15	V_{OLV}	I_{OL} = 2.1mA, Verify in progress	-	-	0.45	V
Output High Voltage	D0~D15	V_{OHV}	I_{OH} = -400µA, Verify in progress	2.4	-	-	V

Notes (1) UV EPROM devices are controlled by input lines $\overline{CS1}$, $\overline{CS2}$, $\overline{PGM1}$, $\overline{PGM2}$ and $\overline{OE}$.

(2) Typical figures are measured at 25°C and nominal V_{CC}

(3) Maximum program current is the sum of I_{CC} and I_{PP}.

(4) **CAUTION**: the PUMA2US2500 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.

(5) During the above operations, $\overline{CS3\sim4}$ and $\overline{WE3\sim4}$ must be held at a logic high level.

(6) $\overline{CS}$ above are accessed through $\overline{CS1\sim2}$. These inputs must be operated simultaneoulsy for 16 bit operation and singly for 8 bit mode.

(7) Information stated for design purposes only.

Operating Modes

This table shows the logic inputs required to control the operating modes of each EPROM on the PUMA2US2500.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	*Outputs*
Read	0	0	1	5V	5V	Data Out
Output Disable	0	1	1	5V	5V	High Z
Standby	1	X	X	5V	5V	High Z
Program	0	1	0	12.5V	6V	Data In
Program Verify	0	0	1	12.5V	6V	Data Out
Page Data Latch	1	0	1	12.5V	6V	Data In
Page Program	1	1	0	12.5V	6V	High Z
Program Inhibit	0	0	0	12.5V	6V	High Z
	0	1	1	12.5V	6V	
	1	0	0	12.5V	6V	
	1	1	1	12.5V	6V	

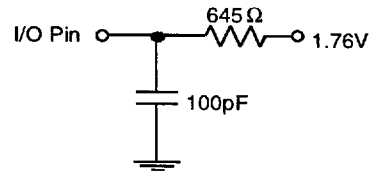
$1 = V_{IH}$
$0 = V_{IL}$
X = Don't Care

Note: $\overline{CS}$ is accessed through $\overline{CS1}$ and $\overline{CS2}$ while $\overline{CS3}$ and $\overline{CS4}$ are both held high. Also, where TTL or CMOS levels are applied they are used on all Chip Selects at the same time i.e. if $\overline{CS1,2} = V_{IL}$ then $\overline{CS3,4} = V_{IH}$

AC Test Conditions

* Input pulse levels: 0V to 3.0V.
* Input and Output timing reference levels: 1.5V
* Input rise and fall times: - 10ns.
* Output load : see diagram
* Module is tested in 8 bit mode.

Output Load



AC Characteristics

Read

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Address to Output Delay	t_{ACC}	-	100	-	120	-	150	ns
Chip Select to Output Delay	t_{CS}	-	100	-	120	-	150	ns
Output Enable to Output Delay	t_{OE}	-	60	-	60	-	70	ns
$\overline{OE}$ or $\overline{CS}$ High to Output Float(1)	t_{DF}	0	50	0	50	0	60	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$	t_{OH}	0	-	0	-	0	-	ns

Parameter	Symbol	-17 min	-17 max	-20 min	-20 max	-25 min	-25 max	Unit
Address to Output Delay	t_{ACC}	-	170	-	200	-	250	ns
Chip Select to Output Delay	t_{CS}	-	170	-	200	-	250	ns
Output Enable to Output Delay	t_{OE}	-	70	-	80	-	100	ns
$\overline{OE}$ or $\overline{CS}$ High to Output Float(1)	t_{DF}	0	60	0	60	0	60	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$	t_{OH}	0	-	0	-	0	-	ns

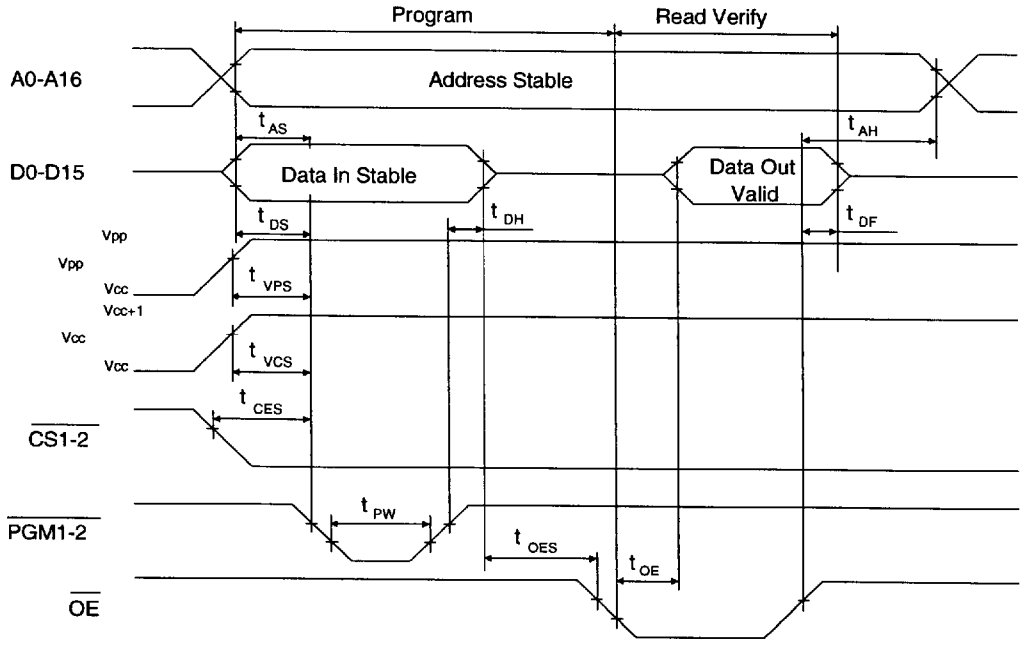
Notes: (1) t_{DFZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.

Write

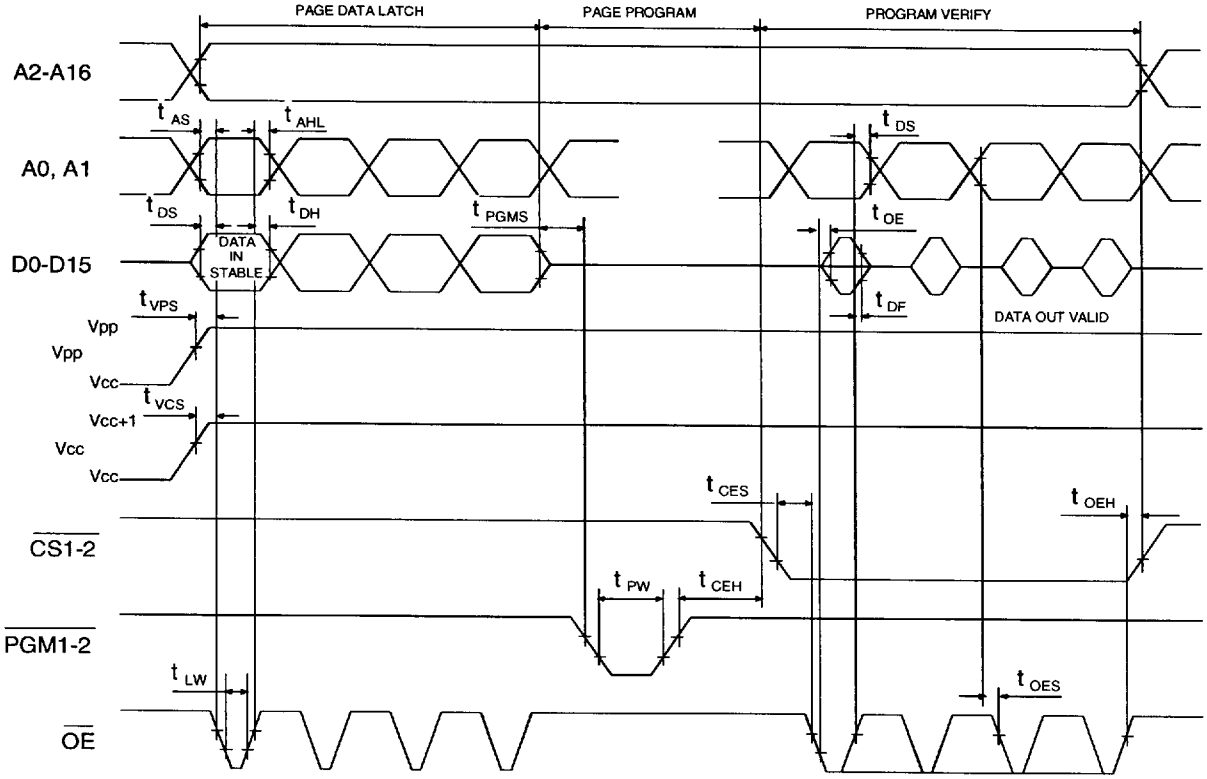
Parameter	Symbol	min	typ	max	Unit
Address Setup Time	t_{AS}	2	-	-	µs
Output Enable Setup Time	t_{OES}	2	-	-	µs
Output Enable Hold Time	t_{OEH}	2	-	-	µs
Data Setup Time	t_{DS}	2	-	-	µs
Address Hold Time	t_{AH}	0	-	-	µs
	t_{AHL}	2	-	-	µs
Data Hold Time	t_{DH}	2	-	-	µs
Output Enable High to Output Float Delay(1)	t_{DF}	0	-	130	ns
V_{PP} Setup Time	t_{VPS}	2	-	-	µs
V_{CC} Setup Time	t_{VCS}	2	-	-	µs
Program Initial Program Pulse Width(2)	t_{PW}	0.19	0.2	0.21	ms
Program Overprogram Pulse Width(3)	t_{OPW}	0.19	-	5.25	ms
Data Valid from Output Enable	t_{OE}	0	-	150	ns
Program Setup Time	t_{PGMS}	2	-	-	µs
Chip Select Setup Time	t_{CES}	2	-	-	µs
Chip Select Hold Time	t_{CSH}	2	-	-	µs
Output Enable Pulse Width during Data Latch	t_{LW}	1	-	-	µs

Notes (1) Defines the time at which the output achieves the open circuit condition and is no longer driven.
(2) The value of this pulse is 0.2 ms ± 5%.
(3) Length of this pulse may vary as a function of the iteration counter value n.

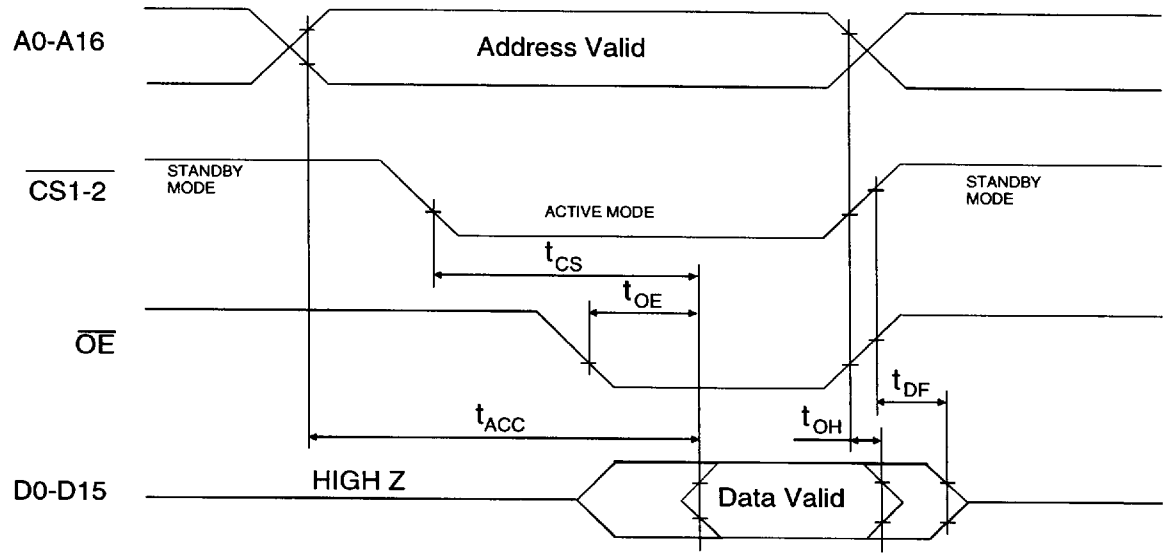
Single Byte Programming



Page Mode Programming



Read Cycle Timing Waveform



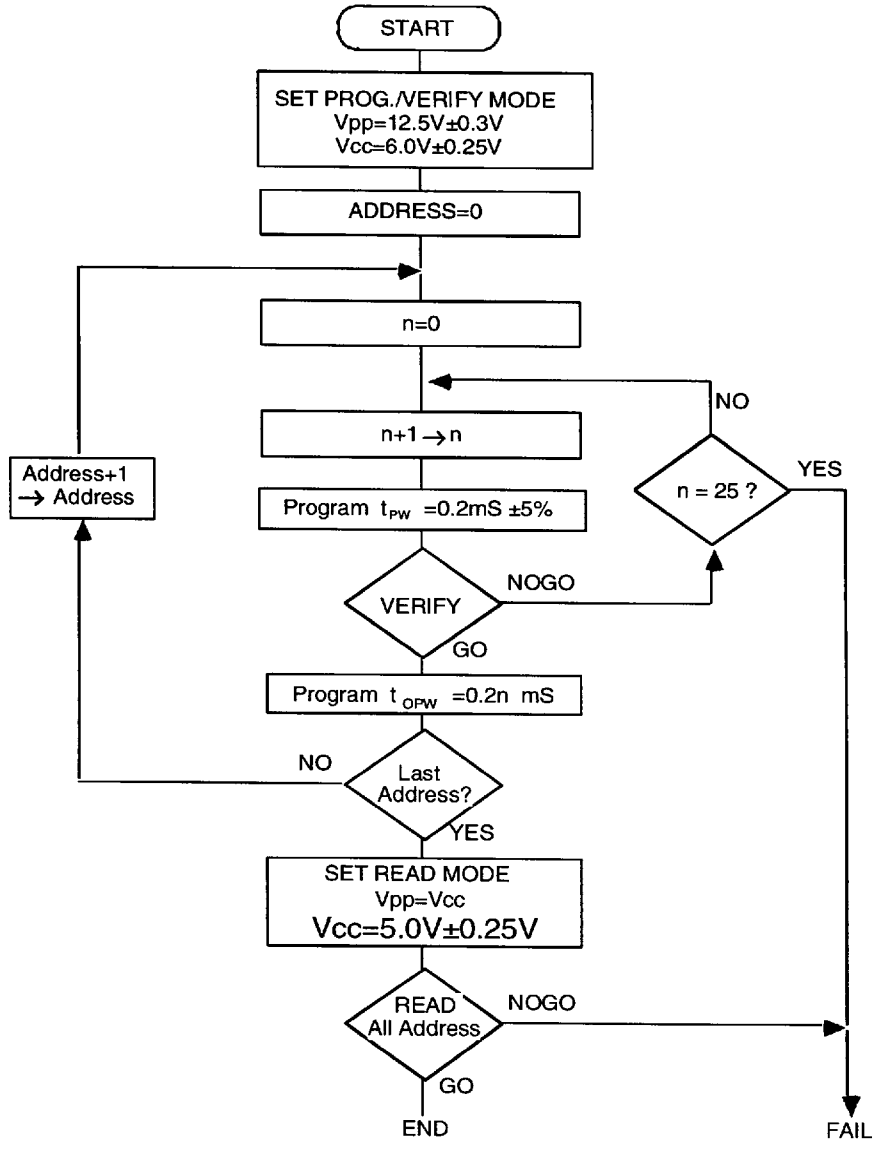
DEVICE OPERATION

High Performance Programming Algorithm

The PUMA 2US2500 can be programmed using either of the algorithms shown below. These allow faster programming times without stressing the device or causing deterioration in Data Retention Time. Two methods are described here, Single Byte and Page Mode; see the Truth Table on page 4 for selection of these modes.

Single Byte

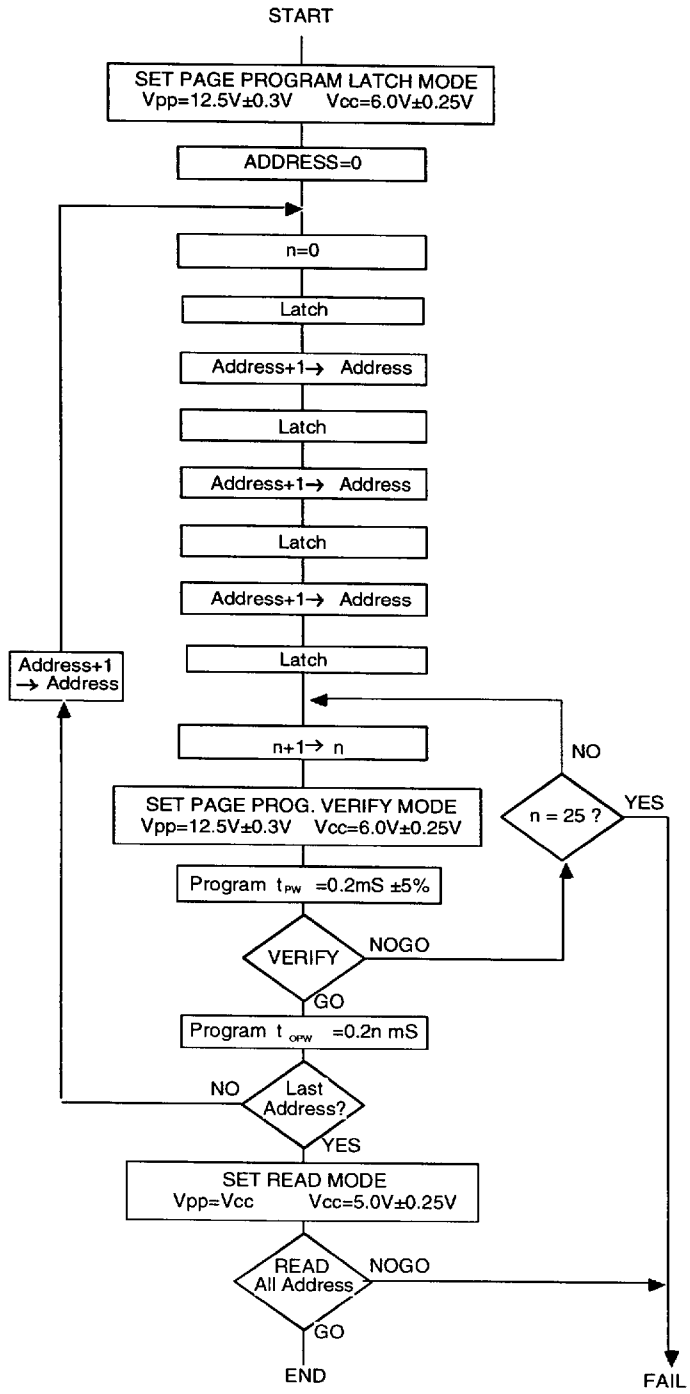
When the Program logic conditions are satisfied, the location is designated by A0~A16, and the data to be programmed is applied 8 bits in parallel on D0~D7. In this state, Byte programming is completed when $\overline{PGM}$ is at a low level.



NOTE: THE ALGORITHM SHOWN HERE MUST BE USED TO ENSURE CORRECT PROGRAMMING OF THE PUMA 2US2500. THIS MAXIMISES THE DATA RETENTION TIME OF THE DEVICE AND DOES NOT STRESS THE MEMORY CELLS.

Page Mode

Page Mode allows 4 bytes of data to be simultaneously programmed. The destination address for a Page Programming operation must reside on the same page i.e. A2~A16 must not change. When the logic conditions in the Truth Table are satisfied, Page Mode Programming is activated. The four locations in the same page are designated by A0~A1, and the data is applied in parallel on D0~D7. In this state the data latch (4 bytes) is completed, and the data is programmed when $\overline{OE}$ is high. Programming is completed when $\overline{PGM}$ is low.



Programming Notes

Upon delivery, or after each erasure, the PUMA 2US2500 has all 2,097,152 bits in the ONE or HIGH state. ZEROs are loaded into the devices through the procedure of programming.

The UV EPROMs are byte/page programmable using a fast high reliability programming algorithm, with complete device programming being possible in 14 seconds (in 16 bit mode). Both of these devices are erased by irradiating them with ultra violet light via the window on the top of the LCC packages. Note that normally, in order to automatically match UV EPROM devices to their correct programming algorithm, both manufacturer and device codes are accessible by placing 12.0V onto address line A9. On this mixed memory technology PUMA this is no***t possible, so the actual device typ***e and relevant codes are given below:

Manufacturer	Code	Device Number	Code
Hitachi	07H	HN27C101A	38H

This mode is entered when 12.5V±0.3V is applied to the V_{PP} pin, $\overline{CS1}$~2 and $\overline{PGM1}$~2 are at V_{IL} and $\overline{OE}$ is at V_{IH}, as shown on the Table on page 4.

The algorithms reduce programming time by using 200µs pulses followed by byte verification to determine if the byte has been successfully programmed. If the data does not verify, up to 25 such pulses (n) can be applied, after which, if verification fails, programming stops. This process is repeated for each memory location within the PUMA 2US2500. After successful programming each memory location is given an overprogram pulse of n times 0.2 ms duration to ensure that all bits have an adequate margin.

The algorithms program at V_{CC}=6.0V in order to ensure that each EPROM bit is programmed to a sufficiently high threshold voltage. After programming is complete, all bytes are compared with the original data with V_{CC}=5.0V±5%.

In order to overcome the voltage drop caused by the inductive effects of the printed circuit board on which the PUMA 2US2500 is used, it is recommended that a 4.7µF electrolytic capacitor is used between V_{CC} and GND for every two devices. This capacitor should be placed close to the point where the power supply is routed to the UV EPROM array.

Erase

Complete erasure of the PUMA 2US2500 is performed by exposure to an ultraviolet light source giving a dosage of 15WS/cm². This dosage can be obtained by using an ultraviolet lamp with a wavelength of 2537 Å at a minimum intensity of 12,000µW/cm², for approximately 15~20 minutes. The PUMA 2US2500 should be directly under and about 1 inch from the light source.

Note that sunlight and fluorescent light may contain sufficient ultraviolet light to erase the programmed information. Although erasure times will be much longer at these levels, the transparent lids on this module should be covered with an opaque label to realise maximum system reliability.

SRAM DATA SECTION

DC Electrical Characteristics (V_{CC}=5V±5%, T_A=-55°C to +125°C)

Read and Write

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
I/P Leakage Current	A0~A14, $\overline{OE}$	I_{LI3}	V_{IN} = 0V to V_{CC}	-	-	±8	µA
	$\overline{WE3~4}$, $\overline{CS3~4}$	I_{LI4}	As above	-	-	±4	µA
Output Leakage Current	D16~D31	I_{LO2}	$\overline{CS}$(2) = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	-	-	±2	µA
Operating Supply Current	16 bit	I_{CC16A}	$\overline{CS}$(2) = V_{IL}, $I_{I/O}$ = 0mA, Inputs Static	-	18	60	mA
Average Supply Current	16 bit	I_{CCV16}	$\overline{CS}$(2) = V_{IL}, Minimum cycle, $I_{I/O}$ = 0mA	-	102	142	mA
	8 bit	I_{CCV8}	As above	-	55	75	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$(2) = V_{IH}	-	2	8	mA
	CMOS levels	I_{SB2}	$\overline{CS}$(2) ≥ V_{IHC}, V_{ILC} ≥ V_{IN} ≥ V_{IHC}	-	0.085	4	mA
Output Voltage Low	D16~D31	V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
Output Voltage High	D16~ D31	V_{OH}	I_{OH} = -1.0mA	2.4	-	-	V

Notes: (1) Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.
(2) $\overline{CS}$ above is accessed through $\overline{CS3~4}$. These inputs must be operated simultaneously for 16 bit mode and singly for 8 bit mode.
(3) **CAUTION**: the PUMA 2US2500 must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.
(4) During the above operation, $\overline{CS1~2}$ and $\overline{WE1~2}$ must be held at a logic high level.
(5) SRAMs are controlled by lines $\overline{CS3}$, $\overline{CS4}$, $\overline{WE3}$, $\overline{WE4}$ and $\overline{OE}$.

Operating Modes

This Table shows the inputs required to control the operating modes of the SRAMs on the PUMA 2US2500 and shows the SRAMs operating in 16 bit mode. If 8 bit operation is required, $\overline{CS3~4}$ and $\overline{WE3~4}$ are controlled independently.

Note that during 16 bit operation, $\overline{CS1~2}$ and $\overline{WE1~2}$, which control the EPROM devices on the PUMA 2US2500, must be at a high level.

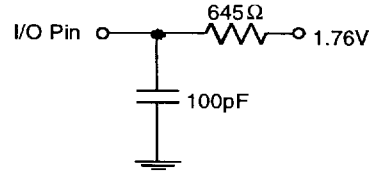
Mode	$\overline{CS3~4}$	$\overline{OE}$	$\overline{WE3~4}$	*D16~D31*	*Reference Cycle*
Standby	1	X	X	High Z	-
Read	0	0	1	D_{OUT}	Read Cycle 1,2,3
Write	0	1	0	D_{IN}	Write Cycle 1
Write	0	0	0	D_{IN}	Write Cycle 2

1 = V_{IH} 0 = V_{IL} X = V_{IL} or V_{IH}

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V.
* Input and Output timing reference levels: 0.8V and 2.0V
* Input rise and fall times: - 10ns.
* Output load : see diagram
* Module is tested in 8 bit mode.

Output Load



Electrical Characteristics & Recommended AC Operating Conditions

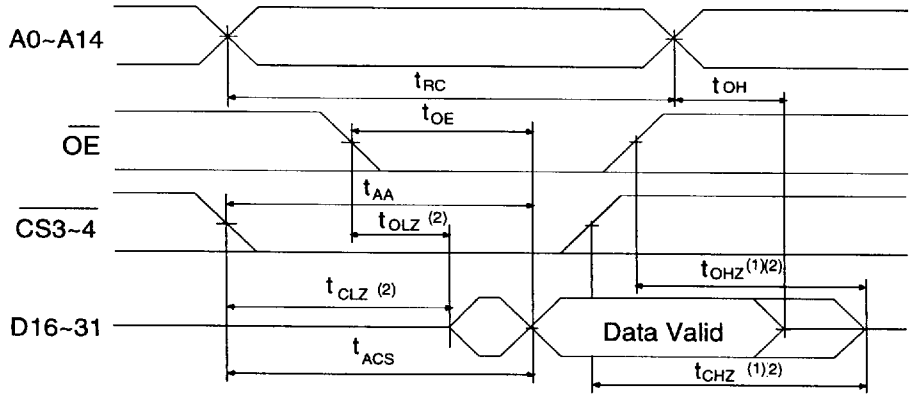
Read Cycle

Parameter	Symbol	-85 min	-85 max	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Read Cycle Time	t_{RC}	85	-	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	85	-	100	-	120	-	150	ns
Chip Select Access Time	t_{ACS}	-	85	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	45	-	50	-	60	-	70	ns
Output Hold from Address Change	t_{OH}	5	-	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z[3]	t_{CLZ}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z[3]	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z[3]	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z[3]	t_{OHZ}	0	30	0	35	0	40	0	50	ns

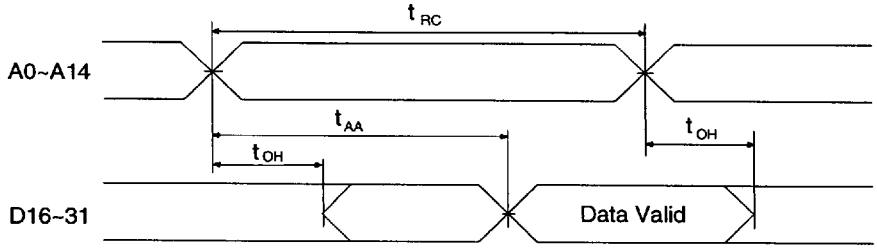
Write Cycle

Parameter	Symbol	-85 min	-85 max	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	85	-	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	75	-	80	-	85	-	100	-	ns
Address Valid to End of Write	t_{AW}	75	-	80	-	85	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	60	-	60	-	70	-	90	-	ns
Write Recovery Time	t_{WR}	10	-	0	-	0	-	0	-	ns
Write to Output in High Z[11]	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	-	40	-	50	-	60	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Disable to Output in High Z[11]	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	5	-	ns

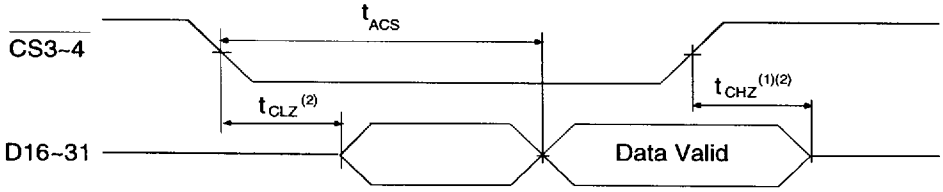
Read Cycle 1 Timing Waveform (3)



Read Cycle 2 Timing Waveform (3)(4)(6)

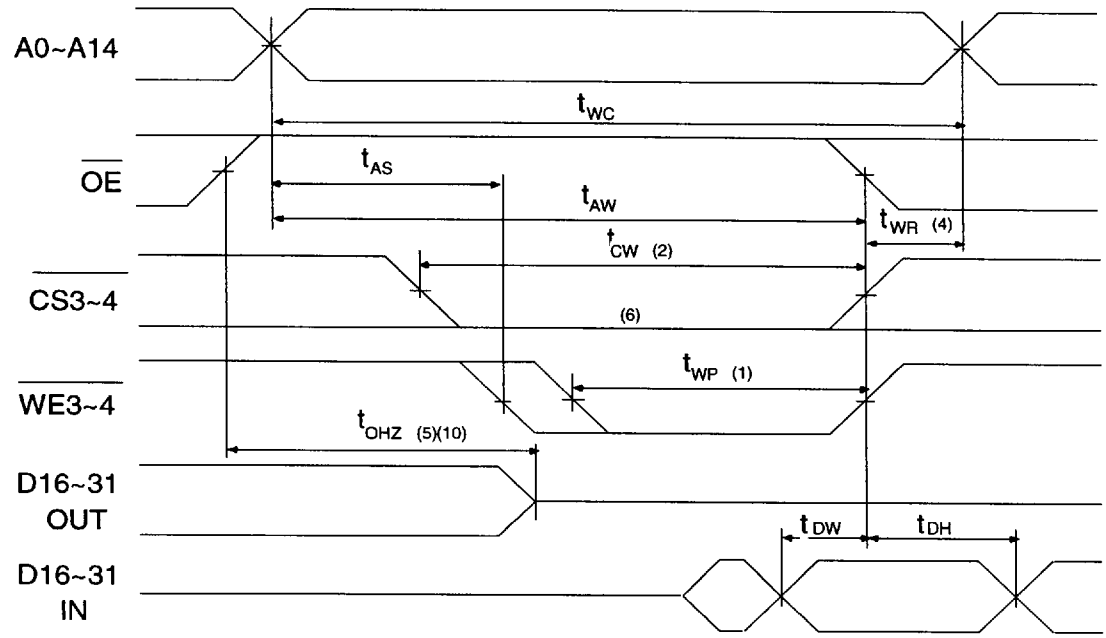


Read Cycle 3 Timing Waveform (3)(5)(6)

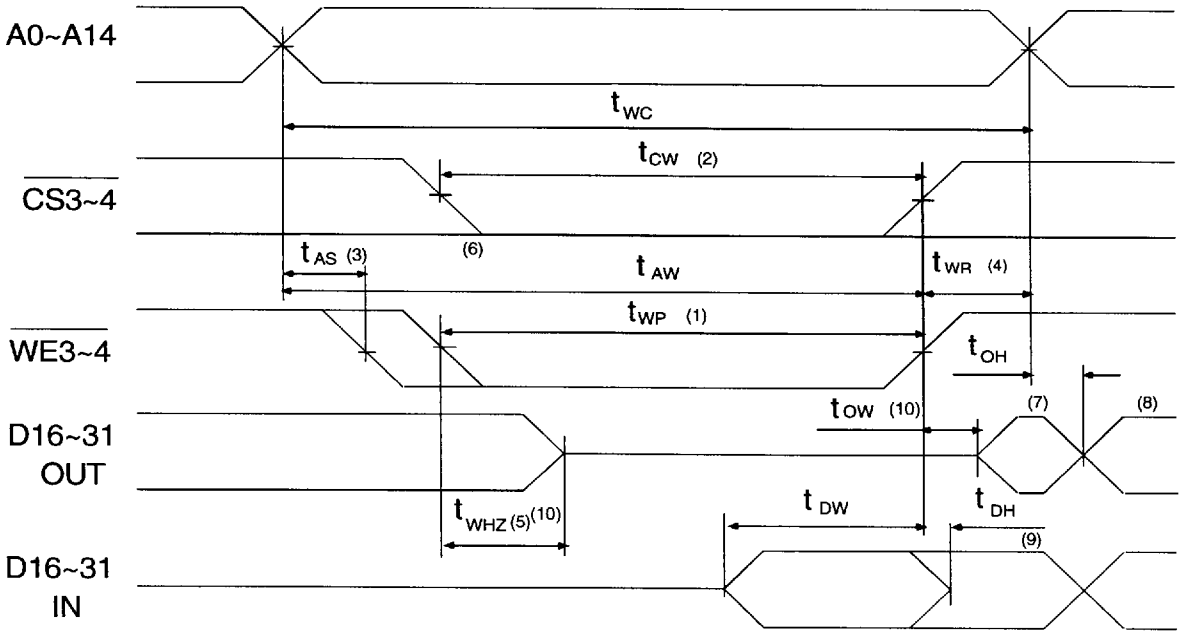


Notes: (1) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
(2) These parameters are sampled and not 100% tested.
(3) $\overline{WE}$ is High for Read Cycle.
(4) Device is continuously selected, $\overline{CS}=V_{IL}$.
(5) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(6) $\overline{OE}=V_{IL}$.

Write Cycle 1 Timing Waveform ($\overline{OE}$ Clock)



Write Cycle 2 Timing Waveform ($\overline{OE}$ Low)



AC Write Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low Chip Select and a low Write Enable. A write begins at the later transition of Chip Select going low or Write Enable going low. A write ends at the earlier transition of Chip Select going high or Write Enable going high. t_{WP} is measured from the beginning of write to the end of write.

(2) t_{CW} is measured from Chip Select going low to the end of write cycle.

(3) t_{AS} is measured from the address valid to the beginning of write.

(4) t_{WR} is measured from the earlier of Chip Select or Write Enable going high to the end of write cycle.

(5) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(6) If the Chip Select low transition occurs simultaneously with the Write Enable low transition or after the Write Enable low transition, outputs remain in a high impedance state.

(7) D_{OUT} is in the same phase as written data of this write cycle.

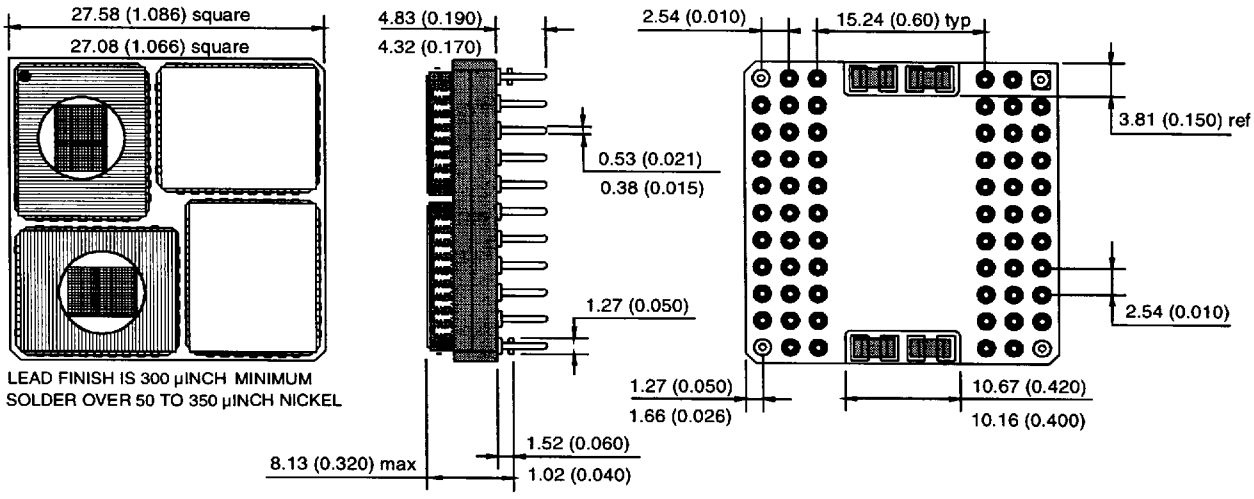
(8) D_{OUT} is the read data of next address.

(9) If Chip Select is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

(10) This parameter is sampled and not 100% tested.

(11) t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Package Details - Dimensions in Inches (Milimeters)



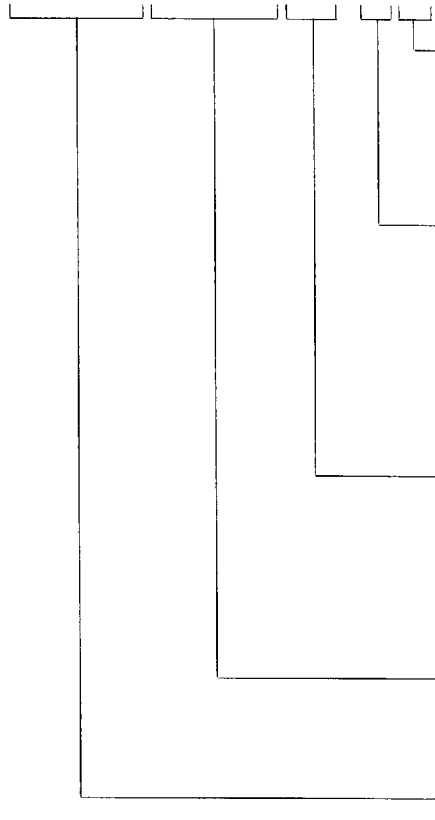
Military Screening Procedure

Module Screening Flow for high reliability product, in accordance with MIL-STD-883, is shown below

MB MODULE SCREENING FLOW		
SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Condition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A = +25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA2US2500MB-1085



SRAM Speed	85	= 85ns
	10	= 100ns
	12	= 120ns
	15	= 150ns
EPROM Speed	10	= 100ns
	12	= 120ns
	15	= 150ns
	17	= 170ns
	20	= 200ns
	25	= 250ns
Temperature range	Blank	= Commercial Temperature Range.
	I	= Industrial Temperature Range.
	M	= Military Temperature Range.
	MB	= Screened in accordance with MIL-STD-883
Organisation	US2500	= 128K x 16 EPROM on sites 1 and 2 32K x 16 SRAM on sites 3 and 4 (both user configurable as x8)
Module Type	PUMA2	= Ceramic 66 Pin Grid Array

Mosaic Semiconductor, Inc., 7420 Carroll Rd. Suite 300, San Diego, CA 92121 Tel: 619.271.4565 Fax: 619.271.6058