

## Low-Power, High-Speed CMOS Analog Switches

### DESCRIPTION

The DG401, DG403, DG405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35  $\mu$ W, typ.) with high speed ( $t_{ON}$ : 75 ns, typ.), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

### FEATURES

- 44 V supply max. rating
- $\pm 15$  V analog signal range
- On-resistance -  $R_{DS(on)}$ : 30  $\Omega$
- Low leakage -  $I_{D(on)}$ : 40 pA
- Fast switching -  $t_{ON}$ : 75 ns
- Ultra low power requirements -  $P_D$ : 0.35  $\mu$ W
- TTL, CMOS compatible
- Single supply capability
- **Compliant to RoHS directive 2002/95/EC**



**RoHS\***  
COMPLIANT

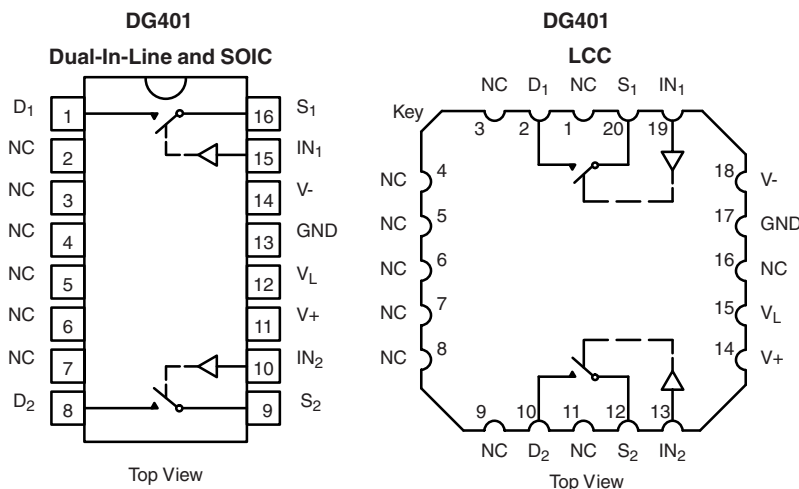
### BENEFITS

- Wide dynamic range
- Break-before-make switching action
- Simple interfacing

### APPLICATIONS

- Audio and video switching
- Sample-and-hold circuits
- Battery operation
- Test equipment
- Communications systems
- PBX, PABX

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



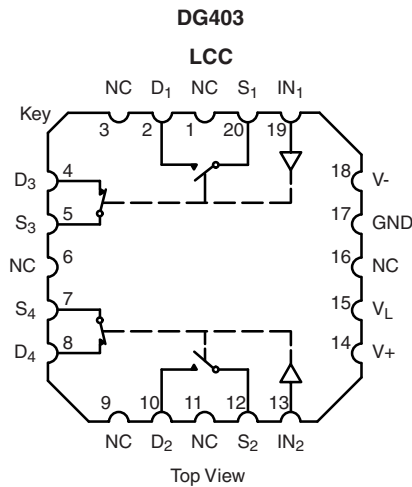
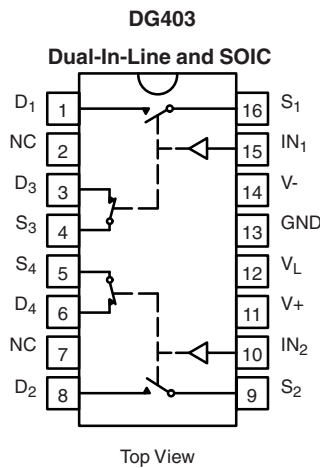
Two SPST Switches per Package

| TRUTH TABLE |        |
|-------------|--------|
| Logic       | Switch |
| 0           | OFF    |
| 1           | ON     |

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

\* Pb containing terminations are not RoHS compliant, exemptions may apply

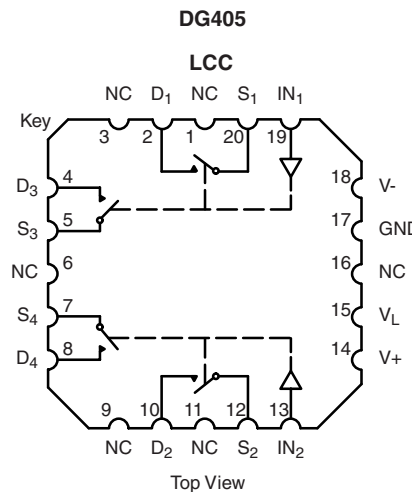
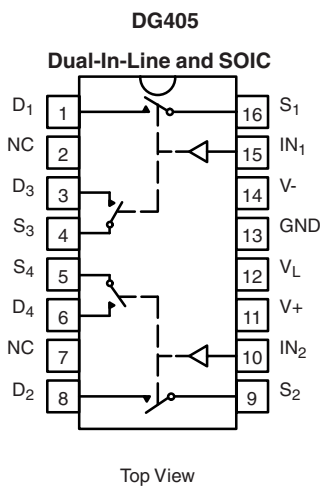
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Two SPDT Switches per Package

| TRUTH TABLE |                                   |                                   |
|-------------|-----------------------------------|-----------------------------------|
| Logic       | SW <sub>1</sub> , SW <sub>2</sub> | SW <sub>3</sub> , SW <sub>4</sub> |
| 0           | OFF                               | ON                                |
| 1           | ON                                | OFF                               |

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V



Two DPST Switches per Package

| TRUTH TABLE |        |
|-------------|--------|
| Logic       | Switch |
| 0           | OFF    |
| 1           | ON     |

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V



| ORDERING INFORMATION |                    |                                                      |
|----------------------|--------------------|------------------------------------------------------|
| Temp. Range          | Package            | Part Number                                          |
| <b>DG401</b>         |                    |                                                      |
| - 40 °C to 85 °C     | 16-Pin Plastic DIP | DG401DJ<br>DG401DJ-E3                                |
|                      | 16-Pin Narrow SOIC | DG401DY<br>DG401DY-T1<br>DG401DY-E3<br>DG401DY-T1-E3 |
| <b>DG403</b>         |                    |                                                      |
| - 40 °C to 85 °C     | 16-Pin Plastic DIP | DG403DJ<br>DG403DJ-E3                                |
|                      | 16-Pin Narrow SOIC | DG403DY<br>DG403DY-E3<br>DG403DY-T1<br>DG403DY-T1-E3 |
| <b>DG405</b>         |                    |                                                      |
| - 40 °C to 85 °C     | 16-Pin Plastic DIP | DG405DJ<br>DG405DJ-E3                                |
|                      | 16-Pin Narrow SOIC | DG405DY<br>DG405DY-E3<br>DG405DY-T1<br>DG405DY-T1-E3 |

| ABSOLUTE MAXIMUM RATINGS                                      |                                 |                                                          |      |
|---------------------------------------------------------------|---------------------------------|----------------------------------------------------------|------|
| Parameter                                                     |                                 | Limit                                                    | Unit |
| V+ to V-                                                      |                                 | 44                                                       | V    |
| GND to V-                                                     |                                 | 25                                                       |      |
| V <sub>L</sub>                                                |                                 | (GND - 0.3) to (V+) + 0.3                                |      |
| Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> |                                 | (V-) - 2 to (V+) + 2<br>or 30 mA, whichever occurs first |      |
| Current (Any Terminal) Continuous                             |                                 | 30                                                       | mA   |
| Current, S or D (Pulsed 1 ms, 10 % Duty)                      |                                 | 100                                                      |      |
| Storage Temperature                                           | (DJ, DY Suffix)                 | - 65 to 125                                              | °C   |
| Power Dissipation (Package) <sup>b</sup>                      | 16-Pin Plastic DIP <sup>c</sup> | 450                                                      | mW   |
|                                                               | 16-Pin SOIC <sup>d</sup>        | 600                                                      |      |

Notes:

a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC board.

c. Derate 6 mW/°C above 75 °C.

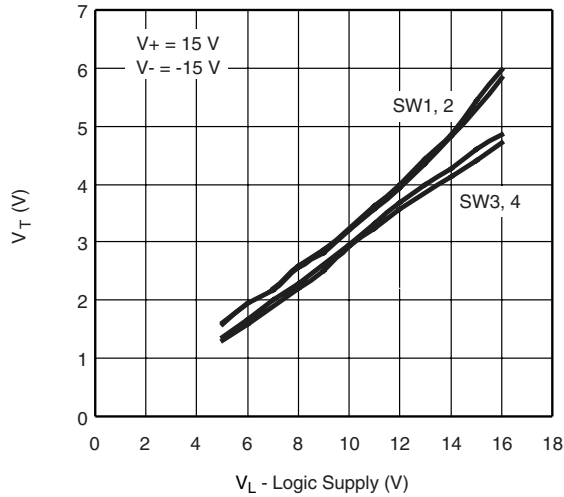
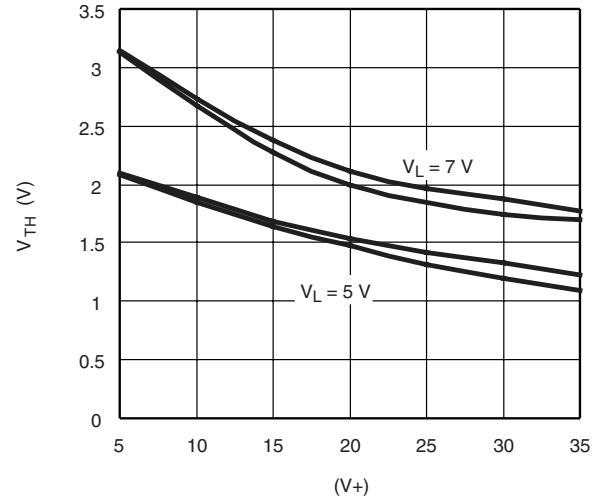
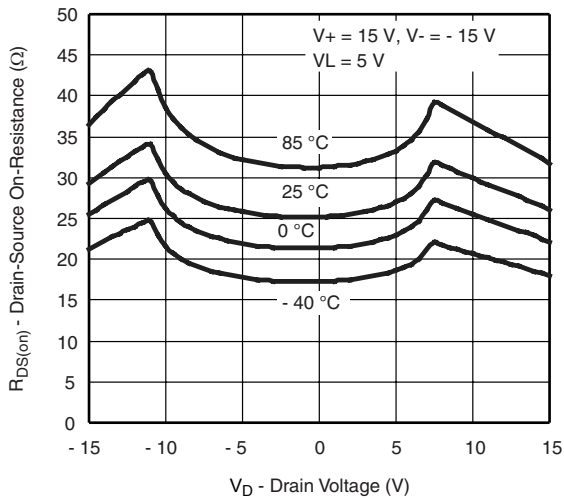
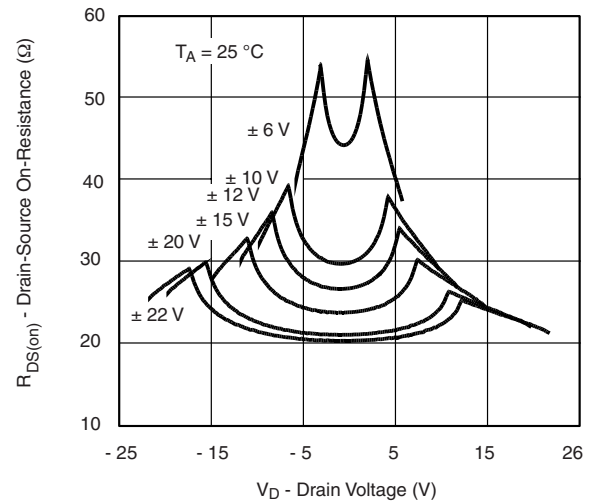
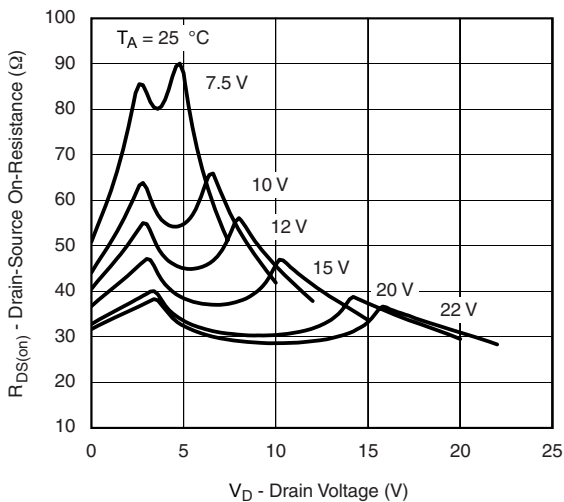
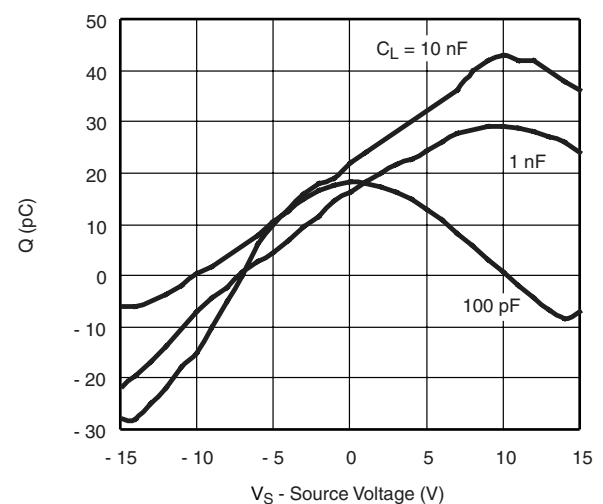
d. Derate 7.6 mW/°C above 75 °C.

| SPECIFICATIONS <sup>a</sup>          |                                     |                                                                                                                                                            |                    |                   |                              |                   |      |
|--------------------------------------|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------|------------------------------|-------------------|------|
| Parameter                            | Symbol                              | Test Conditions<br>Unless Specified<br>V <sub>+</sub> = 15 V, V <sub>-</sub> = - 15 V<br>V <sub>L</sub> = 5 V, V <sub>IN</sub> = 2.4 V, 0.8 V <sup>f</sup> | Temp. <sup>b</sup> | Typ. <sup>c</sup> | D Suffix<br>- 40 °C to 85 °C |                   | Unit |
|                                      |                                     |                                                                                                                                                            |                    |                   | Min. <sup>d</sup>            | Max. <sup>d</sup> |      |
| Analog Switch                        |                                     |                                                                                                                                                            |                    |                   |                              |                   |      |
| Analog Signal Range <sup>e</sup>     | V <sub>ANALOG</sub>                 |                                                                                                                                                            | Full               |                   | - 15                         | 15                | V    |
| Drain-Source On-Resistance           | R <sub>DS(on)</sub>                 | I <sub>S</sub> = - 10 mA, V <sub>D</sub> = ± 10 V<br>V <sub>+</sub> = 13.5 V, V <sub>-</sub> = - 13.5 V                                                    | Room Full          | 30                |                              | 45<br>55          | Ω    |
| Δ Drain-Source On-Resistance         | ΔR <sub>DS(on)</sub>                | I <sub>S</sub> = - 10 mA, V <sub>D</sub> = ± 5 V, 0 V<br>V <sub>+</sub> = 16.5 V, V <sub>-</sub> = - 16.5 V                                                | Room Full          | 3                 |                              | 3<br>5            |      |
| Switch Off Leakage Current           | I <sub>S(off)</sub>                 | V <sub>+</sub> = 16.5 V, V <sub>-</sub> = - 16.5 V<br>V <sub>D</sub> = ± 15.5 V, V <sub>S</sub> = ± 15.5 V                                                 | Room Hot           | - 0.01            | - 0.5<br>- 5                 | 0.5<br>5          | nA   |
|                                      | I <sub>D(off)</sub>                 |                                                                                                                                                            | Room Hot           | - 0.01            | - 0.5<br>- 5                 | 0.5<br>5          |      |
| Channel On Leakage Current           | I <sub>D(on)</sub>                  | V <sub>+</sub> = 16.5 V, V <sub>-</sub> = - 16.5 V<br>V <sub>S</sub> = V <sub>D</sub> = ± 15.5 V                                                           | Room Hot           | - 0.04            | - 1<br>- 10                  | 1<br>10           |      |
| Digital Control                      |                                     |                                                                                                                                                            |                    |                   |                              |                   |      |
| Input Current V <sub>IN</sub> Low    | I <sub>IL</sub>                     | V <sub>IN</sub> under test = 0.8 V<br>All Other = 2.4 V                                                                                                    | Full               | 0.005             | - 1                          | 1                 | μA   |
| Input Current V <sub>IN</sub> High   | I <sub>IH</sub>                     | V <sub>IN</sub> under test = 2.4 V<br>All Other = 0.8 V                                                                                                    | Full               | 0.005             | - 1                          | 1                 |      |
| Dynamic Characteristics              |                                     |                                                                                                                                                            |                    |                   |                              |                   |      |
| Turn-On Time                         | t <sub>ON</sub>                     | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF<br>See Figure 2                                                                                             | Room               | 75                |                              | 150               | ns   |
| Turn-Off Time                        | t <sub>OFF</sub>                    |                                                                                                                                                            | Room               | 30                |                              | 100               |      |
| Break-Before-Make Time Delay (DG403) | t <sub>D</sub>                      | R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF                                                                                                             | Room               | 35                | 5                            |                   |      |
| Charge Injection                     | Q                                   | C <sub>L</sub> = 10 nF<br>V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω                                                                                   | Room               | 60                |                              |                   | pC   |
| Off Isolation Reject Ratio           | OIRR                                | R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 5 pF<br>f = 1 MHz                                                                                                 | Room               | 72                |                              |                   | dB   |
| Channel-to-Channel Crosstalk         | X <sub>TALK</sub>                   |                                                                                                                                                            | Room               | 90                |                              |                   |      |
| Source Off Capacitance               | C <sub>S(off)</sub>                 | f = 1 MHz, V <sub>S</sub> = 0 V                                                                                                                            | Room               | 12                |                              |                   | pF   |
| Drain Off Capacitance                | C <sub>D(off)</sub>                 |                                                                                                                                                            | Room               | 12                |                              |                   |      |
| Channel On Capacitance               | C <sub>D</sub> , C <sub>S(on)</sub> |                                                                                                                                                            | Room               | 39                |                              |                   |      |
| Power Supplies                       |                                     |                                                                                                                                                            |                    |                   |                              |                   |      |
| Positive Supply Current              | I <sub>+</sub>                      | V <sub>+</sub> = 16.5 V, V <sub>-</sub> = - 16.5 V<br>V <sub>IN</sub> = 0 or 5 V                                                                           | Room Full          | 0.01              |                              | 1<br>5            | μA   |
| Negative Supply Current              | I <sub>-</sub>                      |                                                                                                                                                            | Room Full          | - 0.01            | - 1<br>- 5                   |                   |      |
| Logic Supply Current                 | I <sub>L</sub>                      |                                                                                                                                                            | Room Full          | 0.01              |                              | 1<br>5            |      |
| Ground Current                       | I <sub>GND</sub>                    |                                                                                                                                                            | Room Full          | - 0.01            | - 1<br>- 5                   |                   |      |

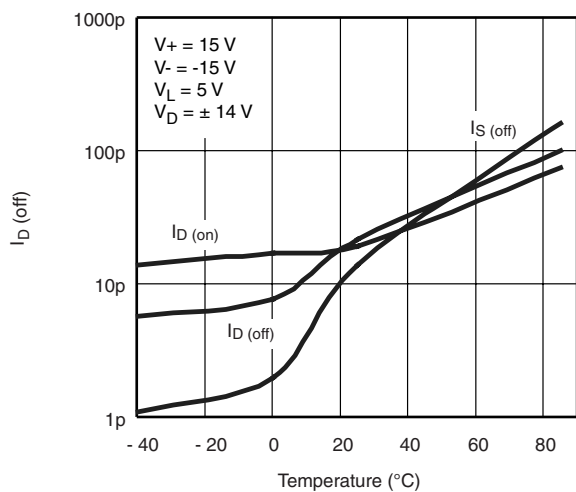
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

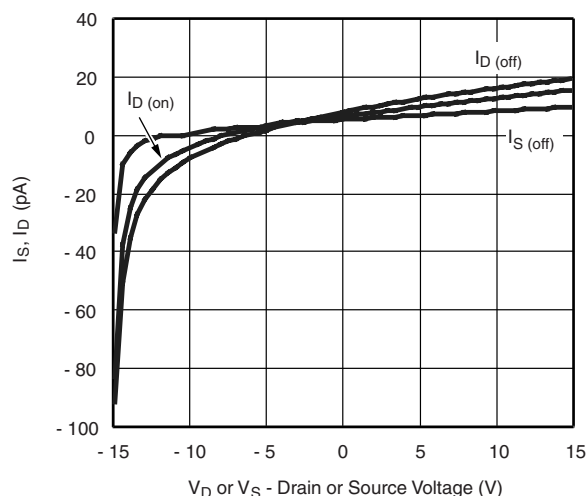
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Input Switching Threshold vs. Logic Supply Voltage**

**Input Switching Threshold vs. Supply Voltages**

 **$R_{DS(on)}$  vs.  $V_D$  and Temperature**

 **$R_{DS(on)}$  vs.  $V_D$  and Power Supply Voltage**

 **$R_{DS(on)}$  vs.  $V_D$  and Power Supply Voltage ( $V_- = 0\text{ V}$ )**

**Charge Injection vs. Analog Voltage**

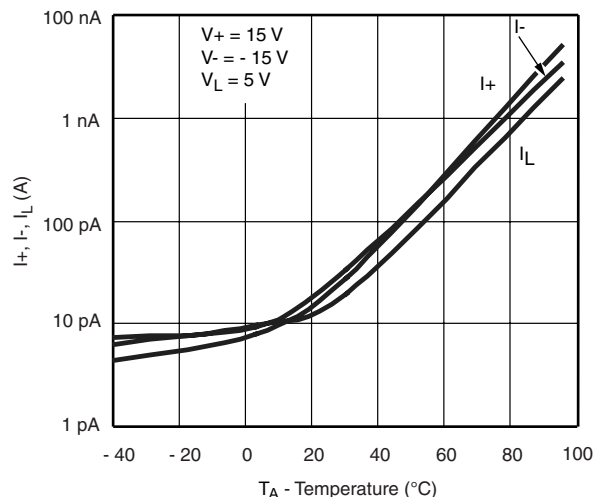
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



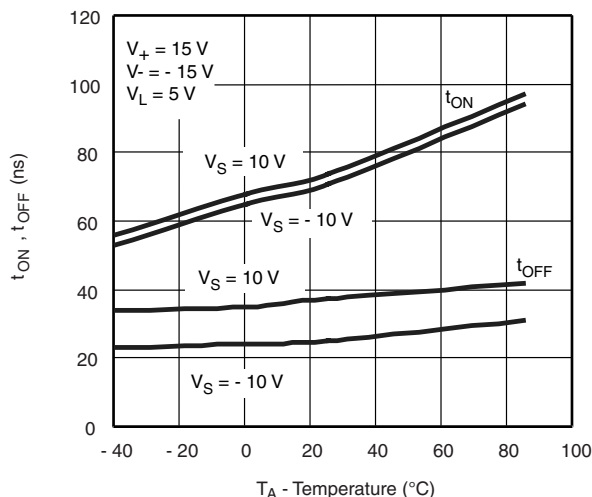
Leakage Current vs. Temperature



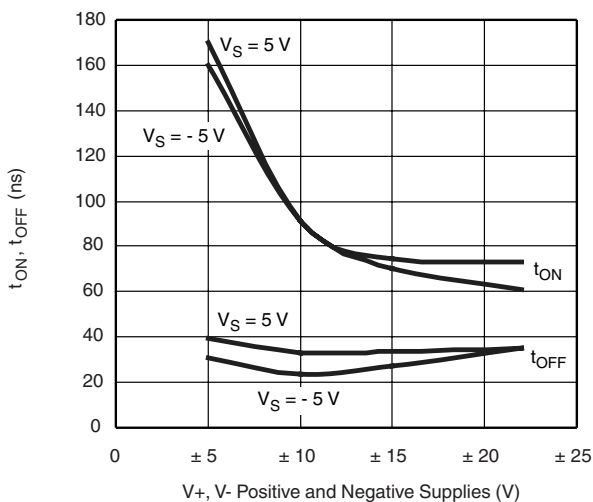
Leakage Current vs. Analog Voltage



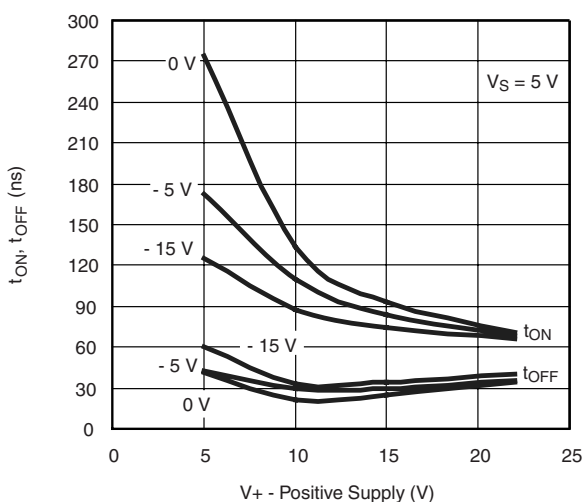
Supply Current vs. Temperature



Switching Time vs. Temperature\*

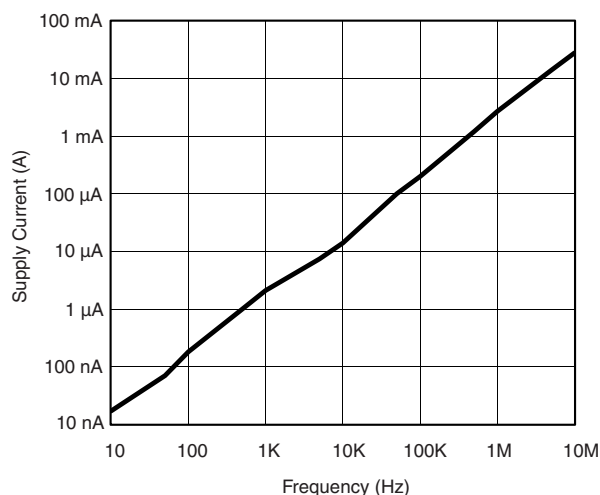
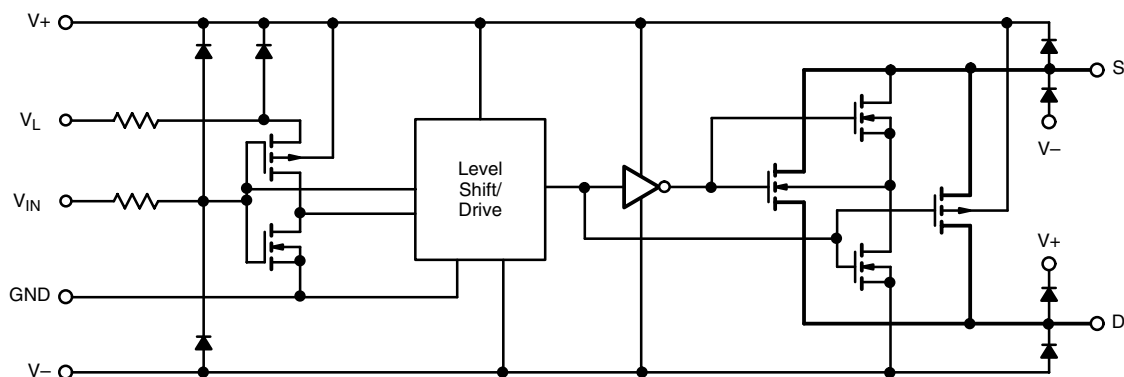


Switching Time vs. Power Supply Voltage\*



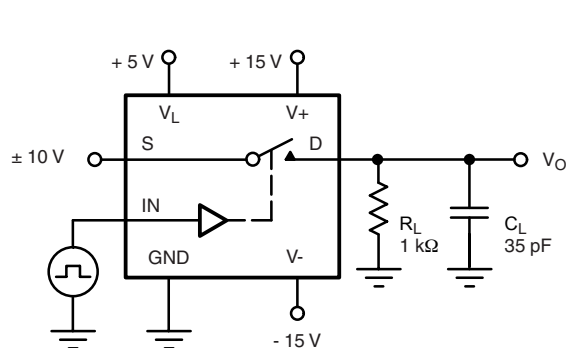
Switching Time vs. Positive Supply Voltage\*

\* Refer to Figure 2 for test conditions.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Supply Current vs. Switching Frequency**
**SCHEMATIC DIAGRAM** Typical Channel

**Figure 1.**

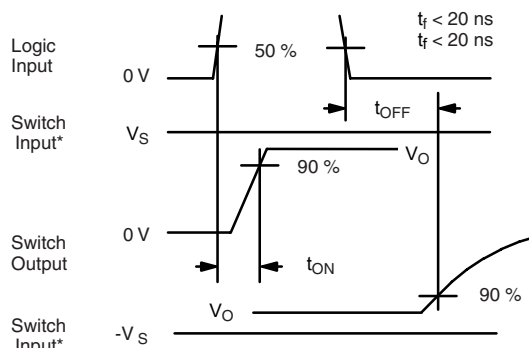
## TEST CIRCUITS

$V_O$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



$C_L$  (includes fixture and stray capacitance)

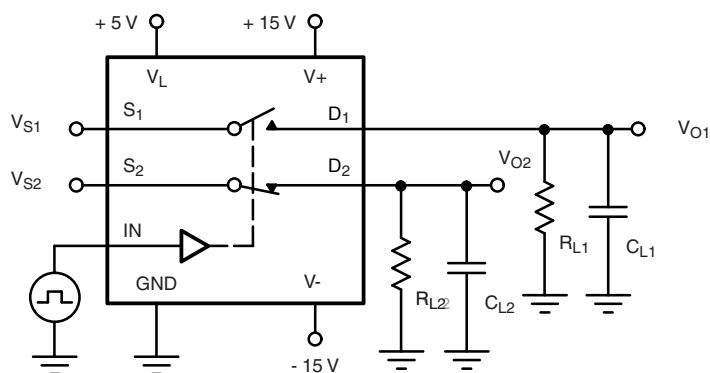
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



\*  $V_S = 10\text{ V}$  for  $t_{ON}$ ,  $V_S = -10\text{ V}$  for  $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time



$C_L$  (includes fixture and stray capacitance)

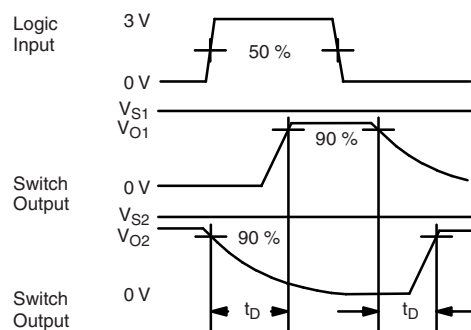


Figure 3. Break-Before-Make

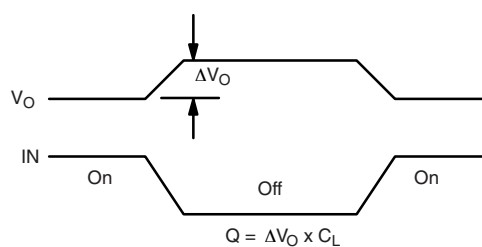
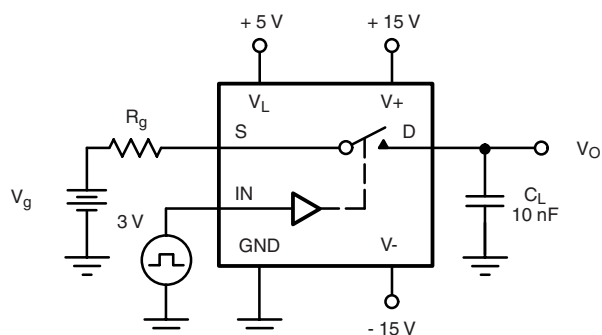
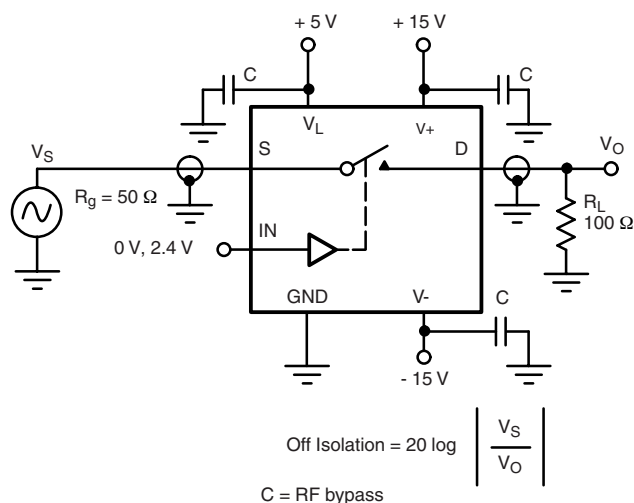
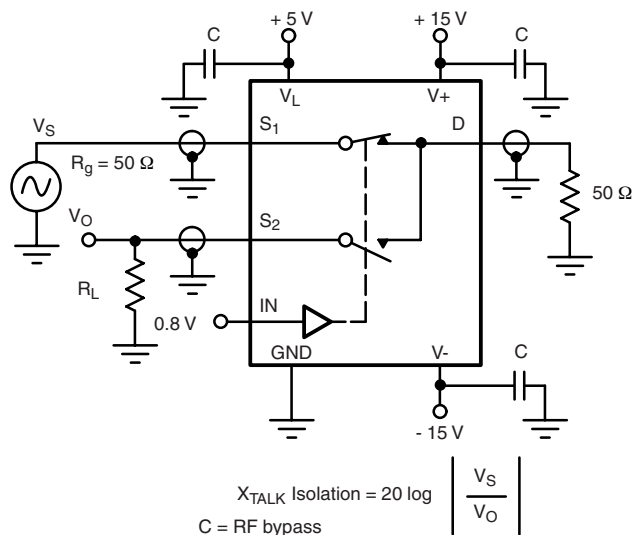
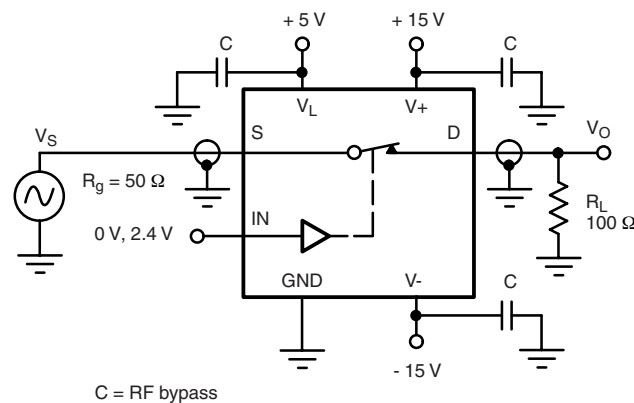
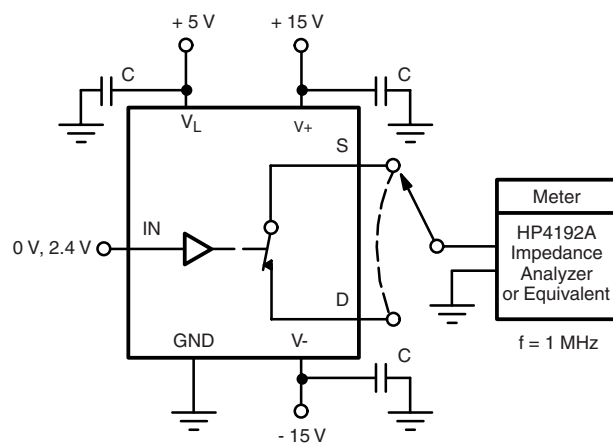


Figure 4. Charge Injection



**TEST CIRCUITS**

**Figure 5. Off Isolation**

**Figure 7. Crosstalk**

**Figure 6. Insertion Loss**

**Figure 8. Capacitances**

## APPLICATIONS

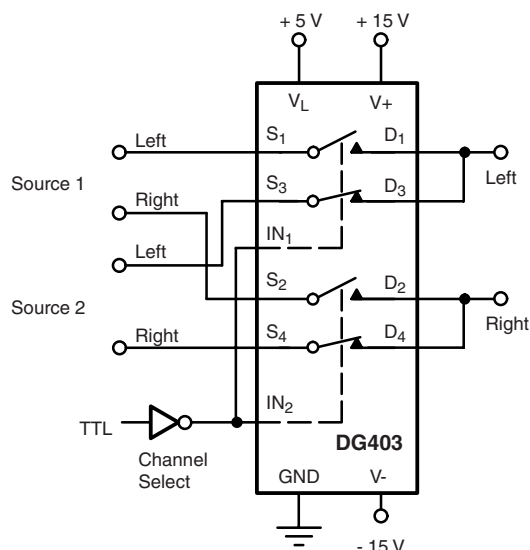


Figure 9. Stereo Source Selector

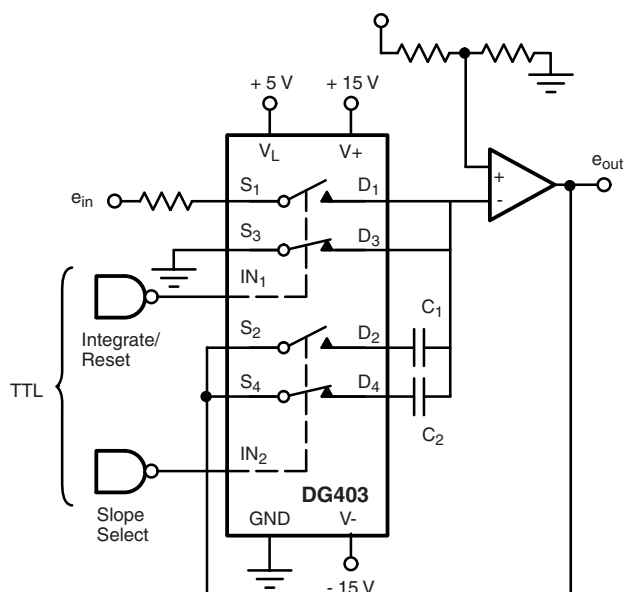


Figure 10. Dual Slope Integrator

### Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor  $C_1$  or  $C_2$ . Another one selects  $e_{in}$  or discharges the capacitor in preparation for the next integration cycle.

### Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

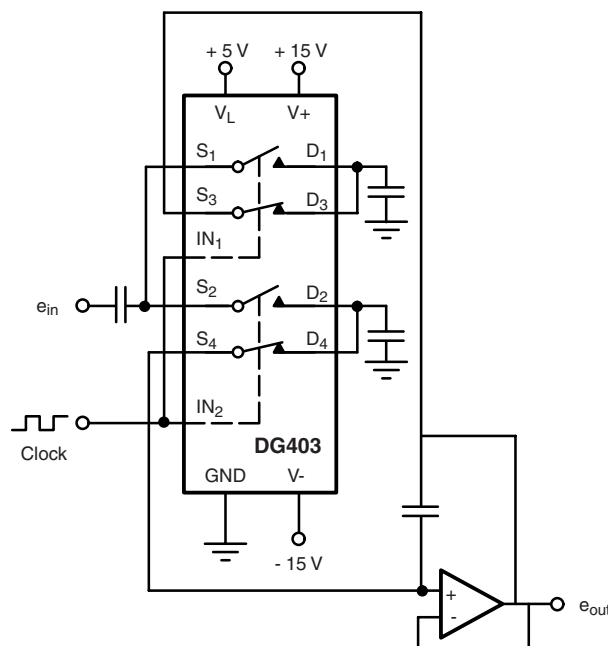


Figure 11. Band-Pass Switched Capacitor Filter

## APPLICATIONS

### Peak Detector:

$A_3$  acting as a comparator provides the logic drive for operating  $SW_1$ . The output of  $A_2$  is fed back to  $A_3$  and compared to the analog input  $e_{in}$ . If  $e_{in} > e_{out}$  the output of  $A_3$  is high keeping  $SW_1$  closed. This allows  $C_1$  to charge up to

the analog input voltage. When  $e_{in}$  goes below  $e_{out}$   $A_3$  goes negative, turning  $SW_1$  off. The system will therefore store the most positive analog input experienced.

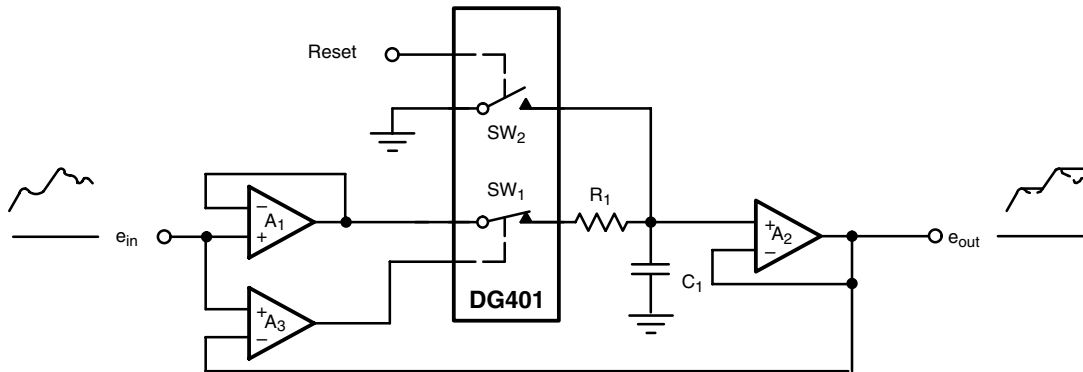


Figure 12. Positive Peak Detector

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?70049](http://www.vishay.com/ppg?70049).



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