Design Considerations for the Am79761 Gigabit Ethernet Physical Layer GigaPHY™-SD Device

Application Note

This document is intended to assist customers in using AMD's Gigabit Ethernet Physical Layer devices. Details concerning application information, circuit design, PCB layout, and component selection are provided to help ensure first-pass success in implementing a functional design which has optimized signal quality.

INTRODUCTION

This document is applicable to the Am79761 GigaPHY-SD product. This document should be used in conjunction with the product data sheet. An elementary knowledge of Ethernet and high speed printed circuit layout techniques is assumed. Contact your local AMD Field Applications Engineer or Sales Office to discuss any questions and concerns you may have.

CLOCK GENERATION

One of the most important aspects of the design is generation of the REFCLK signal. This input provides the reference clock for the internal PLL which is multiplied by 10x or 20x to generate the baud rate clock.The rising edge of REFCLK is continuously phase compared to the internal baud rate clock so that the PLL will speed up or slow down the VCO in order to keep these two signals aligned. It is therefore important that the REFCLK be as jitter-free as possible in order to minimize jitter introduced into the PLL and its baud rate clock. It is also desirable to have fast rising edges on this clock to minimize the time in which the signal transitions from a LOW level to a HIGH level. A fast edge will reduce edge-detection ambiguity in the input buffer and therefore reduce jitter in the PLL.

Note: *The rising edge of this clock also latches the data on the transmit bus into the input latch so care must be taken to ensure that the transmit data bus meets the setup and hold time requirements of the transmitter.*

The most desirable solution for generating REFCLK is to have a crystal oscillator drive the input to an Encoder/Decoder that interfaces to the GigaPHY-SD or MAC device. In some cases, this oscillator will also have to drive a clock input to the Encoder/Decoder. Care must be taken to ensure that good quality signals are present at all inputs (GigaPHY-SD and Encoder/Decoder), and that the proper phase relationship is maintained between the GigaPHY-SD device and Encoder/Decoder chip, since the GigaPHY-SD device latches data on the rising edge of this clock. The GigaPHY-SD device provides a TTL input buffer which does not support AC-coupling of the REFCLK signal.

Although oscillators provide the cleanest source for REFCLK, oscillators over 100 MHz often cost more than may be acceptable for a specific design. In this case, customers have used clock generator chips to provide REFCLK at a lower cost than an oscillator. Unfortunately, the cost reduction is accompanied by a significant increase in REFCLK jitter, which adds jitter to the transmitted serial data resulting in a reduction in the maximum transmission distance.

Another configuration is to generate the REFCLK in the Encoder/Decoder chip. This is desirable where the REFCLK is used to latch incoming transmit data, since it may be easier to meet the setup/hold time requirements of the transmitter, especially when using a 10-bit interface at 125 MHz. When the oscillator drives REFCLK and the Encoder/Decoder chip, the clock-to-output delay of the Encoder/Decoder chip impacts the setup/hold time of the data bus with respect to the REFCLK. When the Encoder/Decoder chip generates REFCLK, the output buffer for REFCLK and the output latch for transmit data track each other and thereby increase setup time. However, the penalty for this scheme is increased jitter added by the Encoder/Decoder chip to the REFCLK. The two configurations for REFCLK generation are shown in Figure 1.

Where possible, it is recommended to let the oscillator drive both the Encoder/Decoder chip and the GigaPHY-SD device in order to provide the cleanest REFCLK.

Publication# **21582** Rev: **B** Amendment/**0**
Issue Date: **May 1998**

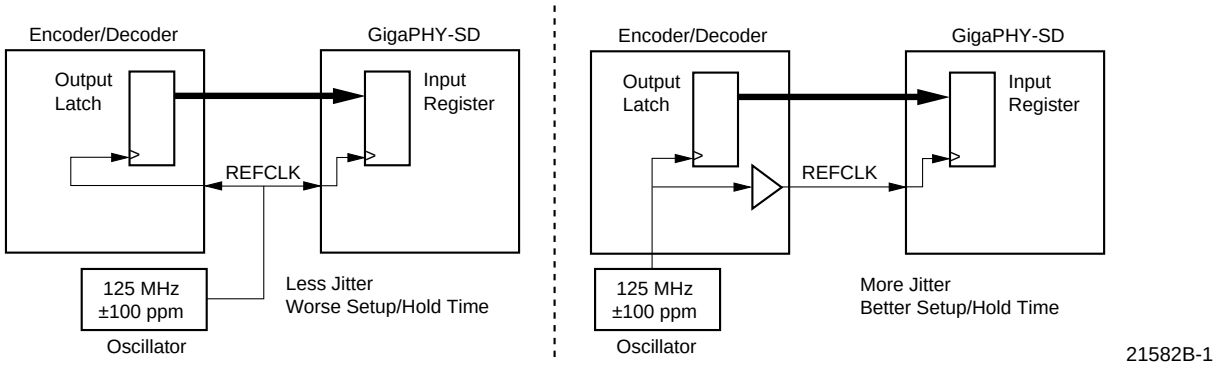


Figure 1. Common REFCLK versus Separate REFCLK

HIGH SPEED SIGNAL TERMINATION

The differential high speed outputs of the transmitter (TX+ and TX-) are PECL outputs, which require unique termination to ensure proper operation and optimize signal quality. Since these signals are clocked at 1.25 GHz and transmit 8B/10B encoded data, they carry digital signals between 125 MHz and 625 MHz. Careful design and layout of the terminations and traces are required to maximize transmission distance and minimize signal degradation. The multiple media choices further complicate the use of these circuits. For the purposes of this discussion, four applications will be described for both the transmitter outputs (TX±) and the receiver inputs (RX±):

- Single-Ended/Differential Coaxial Cable using 50-Ω SMA connectors for test equipment connectivity.
- Single Ended, 75-Ω Coaxial Cable using BNC/TNC connectors for Fibre Channel and Gigabit Ethernet compatibility
- Differential, 150-Ω Duplex Twinax Cable using DB-9 connectors for Fibre Channel and Gigabit Ethernet compatibility.
- Fiber Optic Module interface at 50-Ω.

The transmitter outputs (TX±) are PECL outputs which are capable of sourcing current but not sinking it. Therefore a pull-down resistor (traditionally to VDD - 2.0 V) is required to drive a LOW on the output when the output FET is turned off. The resistance of this pull-down is determined by the parametrics of the part and impedance of the signal trace. Since VDD -2.0 V is usually not present in the system, the output should be terminated to ground (VSS) for convenience. Also, PECL outputs do not conform to ECL input levels, therefore, all high speed I/O should be AC-coupled to eliminate mismatches in signal levels.

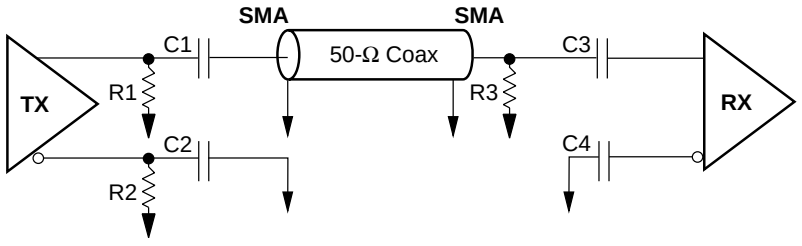
The receiver inputs (RX±) are differential PECL inputs which include resistor dividers to set the bias point of the input (usually at VDD/2). Normally, the user supplies resistors to terminate the transmission line and minimize reflections. An AC-coupling capacitor is provided to isolate the PECL input from the transmission line to let the input buffer set its own DC bias point.

Lastly, a mechanism may be added to provide a DC offset, so that if the input is open, the input buffer will not oscillate. The following sections describe the designs of various termination schemes which provide some, but certainly not all, of the options open to the user.

Single-Ended, 50-Ω Termination

This application is ideal for connecting to test equipment such as oscilloscopes and BERTs but does not conform to the Gigabit Ethernet specification. On the transmitter outputs, a 182-Ω pull-down resistor is located near the pin of the device in order to pull the signal to a LOW level when the output FET is turned off. The value of 182 Ω is used with 50-Ω impedance traces/cables. An AC-coupling capacitor (usually 0.01 µF) is added in series to eliminate the DC component of the output signal allowing general-purpose connectivity.

On the receiver inputs, a 51.1-Ω line termination resistor is provided to match the impedance of the trace and coaxial cable to reduce reflections and optimize signal quality. An AC-coupling capacitor is added in series to allow the input buffer to establish the optimal DC-level provided by its internal resistor dividers. This will restore signal levels to meet the input requirements of the high speed buffer. The unused receiver input is AC-coupled to ground to reduce noise susceptibility, but keeps the input at the internal bias point. The 50-Ω coaxial cable would normally be connected using SMA connectors for ease of use with test equipment. The shells of the SMA connectors are grounded. The typical circuit for this application is shown in Figure 2.



R1=R2=182 Ω, 1% R3=51.1 Ω, 1%
C1=C2=C3=C4=0.01 µF

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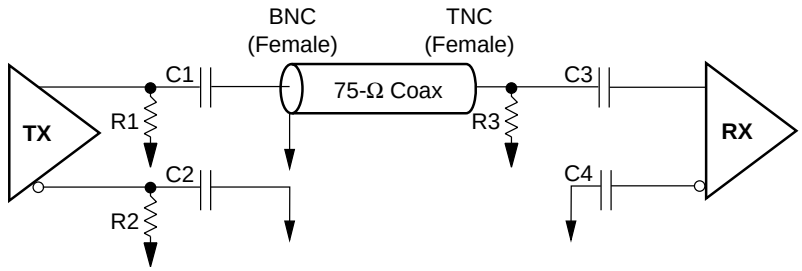
Figure 2. Termination Example: 50-Ω Single-Ended

Single-Ended, 75-Ω Termination

This is a Gigabit Ethernet-compatible application which is similar to the previous example. However, in this example, the pull down resistors R1=R2=267 Ω, instead of 182 Ω to match the 75-Ω transmission lines. Also, the coaxial cabling and connectors are different in order to meet the 75-Ω impedance required by Gigabit Ethernet. The connector of the transmit side is a 75-Ω BNC (female on the board, male on the cable). The connector on the receive side is a 75-Ω TNC (female on the board, male on the cable). The shell of the BNC is grounded, but the TNC shell is left open. These mismatched connectors provide built-in polarization. The typical circuit for this application is shown in Figure 3.



R1=R2=267 Ω, 1% R3=75 Ω, 1%
C1=C2=C3=C4=0.01 µF

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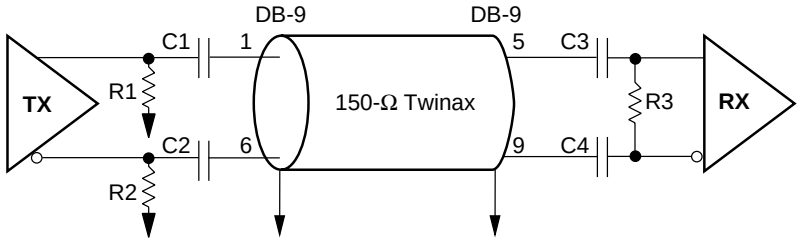
Figure 3. Termination Example: 75-Ω Single-Ended

Differential, 150-Ω Twinax Termination

A more popular Gigabit Ethernet-compatible application is for 150-Ω differential signals using 9-pin D-Subminiature connectors (also known as DB-9) and duplex twinax cable. This provides better signal quality, longer transmission distance, and reduced emissions as compared to single-ended configurations. Both outputs from the transmitter are terminated with 267-Ω pull downs. One percent components are used to maintain a balanced load between the two differential outputs. On the receive side, a single 150-Ω line termination resistor is used for impedance matching. This is located on the receiver side of the AC-coupling capacitors since this resistor will not affect the DC bias circuit. The connector for this application is a 9-pin D-Subminiature (female on the board, male on the cable) with TX+ on pin 1, TX- on pin 6, RX+ on pin 5, and RX- on pin 9. The shield of the cable is connected to chassis ground on both ends to provide a low impedance grounded shield. A cost-effective duplex twinax cable having an effective shielding scheme that reduces emissions to the point that systems pass the FCC-B and CISPR EMI levels is available from W. L. Gore. The typical circuit for this application is shown in Figure 4.



R1=R2=267 Ω, 1%
C1=C2=C3=C4=0.01 μF
R3=150 Ω, 1%

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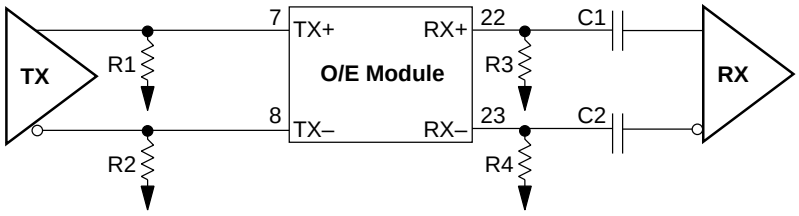
Figure 4. Termination Example: 150-Ω Differential

Fiber Optic Module Termination

Many customers wish to use Gigabit Ethernet over fiber optic cable for increased distance, reduced EMI, or other reasons. In general, this is a 50-Ω application. However, each vendor of fiber optic transceivers may have slightly unique interfacing requirements, so it is recommended that the user contact the vendor prior to design. For the purposes of this example, a circuit which interfaces to Finisar's FTR-8510 and Methode's MTR-8510 800 nm transceiver module is described.

No AC-coupling capacitors are required on the transmit side, so only 180-Ω pull-down resistors are provided. This application example assumes short traces (less than 2 inches), so that termination resistors are not required at the end of the traces on the transmit side. On the receive side, the normal 51.1-Ω and AC-coupling capacitor is provided. This is illustrated in Figure 5.



R1=R2=182 Ω, 1%
C1=C2 = 0.01 μF
R3, R4=51.1 Ω, 1%

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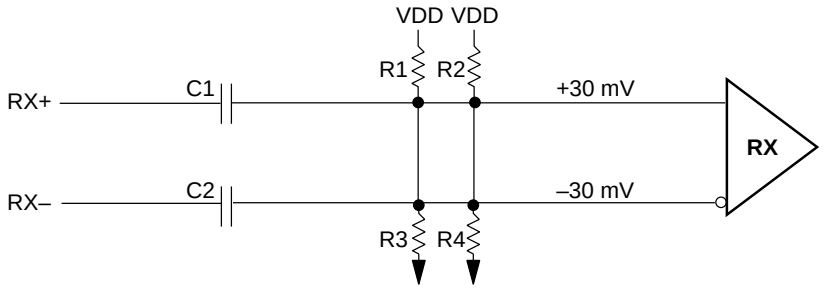
Figure 5. Termination Example: Fiber Optic Transceiver

PREVENTING OSCILLATIONS

Since a link can be disconnected or a transmitter can be disabled, there are times when the receiver's inputs might not carry a valid signal. In the absence of a signal, both inputs of the receiver (RX±) will be at their internally determined bias points which are, by design, identical. When a differential input buffer's inputs are identical, the buffer is susceptible to oscillations which could cause noise within the receiver. AMD's input buffers do not oscillate normally; however, in a noisy environment oscillations may occur. To prevent this problem, a Thevenin-equivalent resistor pair is used to both terminate the transmission line and provide a small DC offset to the receiver. This offset is kept as low as possible so as not to introduce an offset under normal conditions, which might add to the input jitter seen by the receiver. An example of this is shown in Figure 6 with values for both 50-Ω and 75-Ω impedance applications.

Unused Inputs

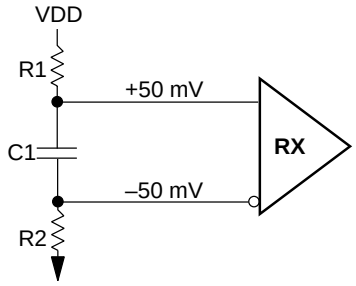
In many applications the receiver inputs might not be used. In this situation, it is important to terminate the inputs so that they will not oscillate. In a single-ended application, the unused receiver input is AC-coupled to ground to reduce noise susceptibility, but the input at the internal bias point is kept. If the differential inputs are not used, then the circuit shown below is recommended. A variety of useful circuits may be used for this purpose, but two considerations are as follows: (1) provide a DC-offset and (2) provide a low-impedance noise attenuation path.



R1=R4=97.6 Ω, 1% R2=R3=102 Ω, 1% for 50 Ω impedance, [72 mV offset]
R1=R4=147 Ω, 1% R2=R3=154 Ω, 1% for 75 Ω impedance, [76 mV offset]
C1=C2=0.01 µF

Figure 6. Termination Example: Preventing Oscillation

In the circuit shown in Figure 7, 47K Ω external resistors are added in parallel with the internal 3 K Ω pair. This results in a 50-mV offset. The capacitor across the inputs provides a low-impedance path to reduce noise susceptibility.



R1=R2=47K Ω, 5%
C1=0.01 µF

Figure 7. Termination Example: Unused Inputs

POWER SUPPLY CONSIDERATIONS

Generating 3.3 V from a Linear Regulator

AMD's Gigabit Ethernet PHYs operate with a 3.3 V ±5% power supply. Although the migration to 3.3 V logic power supplies is underway, many systems do not have an available 3.3 V supply. The easiest, smallest, and cheapest way to convert from a 5 V power supply to a 3.3 V level is through the use of a linear regulator. Converting from a +12 V supply to a 3.3 V supply is more difficult due to the additional power dissipation in the regulator that must be handled correctly. At 5 V ±10%, the power dissipated in the regulator is calculated as (5.25 V - 3.3 V)*IDD(max). The advantage of a linear regulator is that it provides a very quiet output that is isolated from the noise on the 5 V supply. Since signal jitter is sensitive to power supply noise, the clean outputs of the linear regulator contribute to improved signal quality.

A readily available, multiple-sourced linear regulator is the Linear Technology LT1086CM-3.3, which is a fixed 3.3 V output voltage regulator that provides up to 1.5 A output current. This is more than adequate to power the GigaPHY-SD device. A simple application circuit is shown in Figure 8. Minimum values of input and output capacitance are required to provide stability to the regulator. Additional bypass capacitors must be added for additional power supply filtering at the pins of the chip. Similar linear regulators with different current limits are the LT1117CST-3.3 (800 mA, SOT-223) and the LT1586CM-3.3 (4A, TO-220), both from Linear Technology.

Generating 3.3 V from a DC/DC Converter

The limitation of a linear regulator is that it is not efficient, therefore, heat is generated. In applications where excessive heat is not acceptable, a DC/DC Converter may be used to convert either the 5 V or 12 V supplies into a 3.3 V supply. The DC/DC converters available for the current levels needed in this application have excellent efficiency, between 85% and 95%, which reduces heat generation. However, the DC/DC converters are more expensive, require more real estate, require more components, are not trivial to use, and add noise to the 3.3 V supply. The noise is a concern since power supply noise will couple into the PLL circuits and buffers of the transmitter and receiver, thereby, increasing jitter generation in the transmitter and reducing jitter tolerance in the receiver. If a DC/DC converter is used, extra care should be taken to reduce output noise.

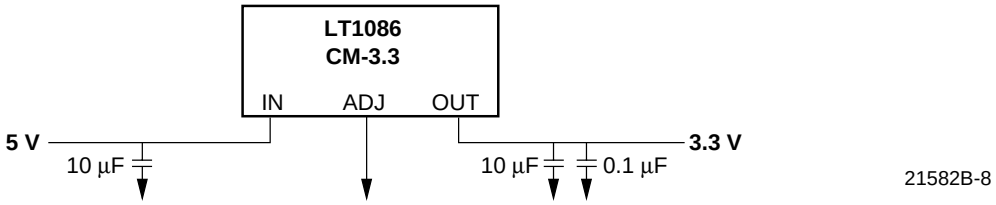


Figure 8. 5 V to 3.3 V Conversion using a Linear Regulator

A DC/DC Converter that is appropriate for powering the GigaPHY-SD device is the Linear Technology, LT1256 1.5A part. The DC/DC converter circuit is not shown here since excellent application notes are provided by the manufacturer.

BYPASSING

The method in which bypass capacitors are used to filter the power supply to the GigaPHY-SD device has a significant impact upon signal quality. First, it is mandatory that the design include a power plane for VSS (Ground) which is at least 1 oz. copper. Secondly, a similar power plane for VDD (3.3 V) is strongly recommended. To reduce inductance, vias used to connect to these planes should not include thermal cut-outs similar to those found on VDD/VSS connections to through-hole components. It is strongly suggested that each power and ground pin be supplied from their own vias. Bypass capacitors are more effective when located on the same side of the PCB as the GigaPHY-SD device. Of course, the capacitors *must* be located as closely as possible to the VDD and VSS pins of the chips. Furthermore, it is recommended that the capacitor be located between the pin and the via to the plane. The preferred method for the layout of the bypassing capacitors is shown in Figure 9. Since AMD's GigaPHY-SD device has roughly constant power supply current, there is no need for exotic bypassing methods (i.e., two capacitors in parallel aimed at the switching frequency of the internal circuit). It is also recommended that the power and ground planes remain intact rather than attempting to steer current paths through sculpted planes. Most customers who have tried to isolate the planes for the transmitters and receivers usually produce more noise, rather than reduce noise.

The GigaPHY-SD has internal PLLs which are powered from separate supply pins usually called AVDD/AVSS where the "A" denotes analog. These pins are particularly sensitive to noise, so additional care must be taken to filter out noise. It is recommended that AVDD pass through a ferrite bead (i.e., TDK CB50-1206) to a bypass capacitor (at least one 0.1 µF) and the power pin. The layout shown in Figure 9 indicates the preferred method for layout of this circuit.

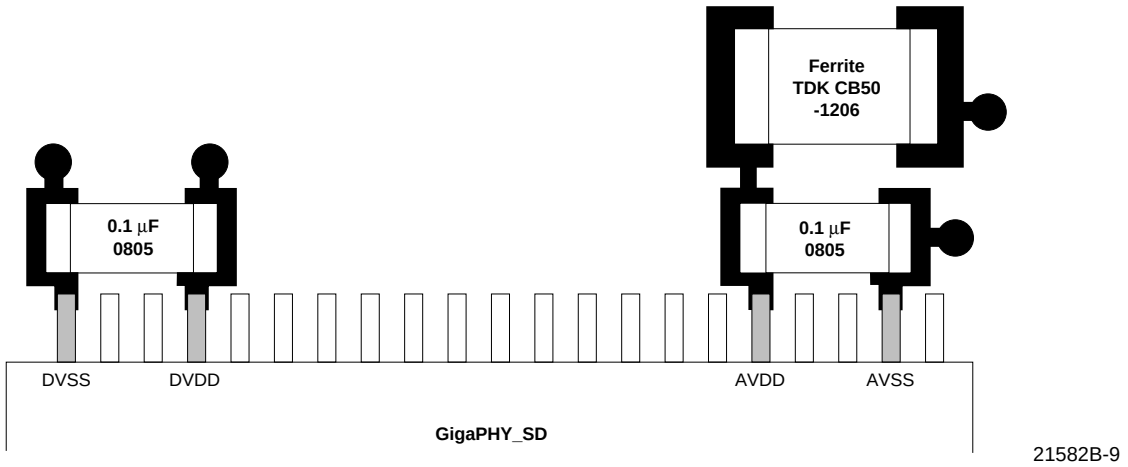


Figure 9. Bypassing Layout Example

LAYOUT CONSIDERATIONS

When implementing a 1-Gbps serial communications link, the importance of the layout cannot be overstressed. However, following general, simple-to-use guidelines will ensure success and prove easier than most designers anticipate. The prioritization of signals is as follows:

- High speed serial I/O lines
- REFCLK traces
- Power supplies and bypass capacitors
- Control signals
- Data busses

Careful placement of components and the use of passives on both the top and bottom sides will generally ensure optimal layout. As mentioned previously, a solid ground and power plane are quite useful in distributing clean power.

High Speed Serial I/O Layout

These signals contain digital data at frequencies between 125 MHz to 625 MHz and require excellent frequency and phase response up to at least the 3rd harmonic, if not the 7th harmonic. Improved signal quality and longer practical transmission distances will result when the designer follows the general rules below:

- Keep traces as short as possible. Initial component placement should be very carefully considered.
- The impedance of the traces must match that of the termination resistors, connectors, and cable in order to reduce reflections due to impedance mismatches.
- Impedance matching termination resistors (i.e., 51.1 Ω, 75 Ω or 150 Ω) should be located as close as possible to the input pin of the receiver to minimize stub length. Since an AC-coupling capacitor is often inserted between the pin and the termination resistor, this is sometimes difficult to optimize.
- Differential impedance must be maintained in a 150-Ω differential application. Routing two 75-Ω traces is *not* adequate. The two traces must be separated by enough distance to maintain 150-Ω differential impedance. A good rule of thumb is that the trace separation should be at least 2.5 times the trace width.
- When routing differential pairs, keep the trace length identical between the two traces. Differences in trace lengths translate directly into signal skew. When separations occur, the differential impedance may be affected so take care when this is done.
- Keep differential pair traces on the same side of the PCB to minimize impedance discontinuities.
- Place any impedance discontinuities close to the transmitter or receiver and locate them together. This will minimize their impact on signal quality.
- Eliminate or reduce stub lengths.
- Reduce, if not eliminate, vias to minimize impedance discontinuities.
- Use rounded corners rather than 90° or 45° corners.
- Keep signal traces far from other signals which might capacitively couple noise into the signals. This includes the other trace of a differential pair.
- Do not route digital signals from other circuits across the area of the transmitter and receiver.
- Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less.

REFCLK Layout

The most difficult issue with regard to the REFCLK is that the signal goes to multiple inputs which all require an extremely clean clock with fast edges. This becomes a clock distribution challenge. Of course, from an emissions point of view, the goal is to eliminate the high-frequency harmonics in order to reduce radiated emissions. Therefore, a system developer may have contradictory goals requiring a compromise position.

Power Supply Layout

These issues have been discussed previously and will not be detailed here. Vias used to connect the power planes to the DVDD and DVSS pins of the chips should be at least 0.010 inches in diameter, preferably with no thermal relief and plated closed with copper or solder. Also, the via should be located on the opposite side of the bypass capacitor from the pin.

Control Signal Layout

There are no time-critical control signals on the GigaPHY-SD device. However, it is important to route control lines to the chips in such a way as to avoid crosstalk and noise injection.

Data Bus Layout

The problem with the data busses is that there are a lot of signals in a small area. The only consideration here is to keep the traces roughly the same length as the clock used to latch them, so that trace length differences do not reduce the setup/hold times of the chips.

CONCLUSION

Following the general guidelines described in this design guide will help ensure that customers integrating Gigabit Ethernet components experience first-time success. Contact your local Field Applications Engineer who will be happy to work with customers in any way to promote the success of their designs, including providing schematic and layout reviews.

COMPONENT SUPPLIER LIST

The following table is a list of vendors who supply components of interest to Gigabit Ethernet customers. Where applicable, a part number and description have been provided for key components required for specific applications.

Component Supplier List		
Copper Cable Assemblies		
AMP	(800) 52A-MP52	High Frequency Coax, Twinax & Quad Cable Assemblies
Berg	(717) 764-7200	Cable Assemblies
Trompeter Electronics	(818) 707-2020	Coaxial Cable Assemblies
W. L. Gore	(302) 368-2575	Quad Cable, P/N FCN1008-xx, where xx is distance in meters
Connectors		
AMP	(800) 52A-MP52	RF, Coax, DB-9 & Fibre Channel specific (HSSDC) connectors.
E. F. Johnson	(800) 247-8256	RF, Coaxial connectors
Fiber Optic Modules		
AMP/Lytel	(800) 52A-MP52	O/E Modules
BCP	(407) 984-3671	51T Transmitter & 51R Receiver
Finisar	(415) 691-4000	Gbps O/E Modules at 800 nm, FTR-8510
Force Electronics	(703) 382-0462	2684T Transmitter and 2684R Receiver
Fujikura Technology	(408) 748-6991	O/E Modules
Methode Electronics	(708) 867-9600	Gbps transceivers at 800 nm, MTR-8510.
Fiber Optic Cable		
3M Fiber Optics	(908)544-9119	
Alcoa/Fujikura	(800)866-3953	
Methode Electronics	(800)323-6858	
Magnetics		
Coilcraft	(800) 322-2654	Transformers for Line interfacing
Technitrol	(215) 426-9105	Active and Passive Equalizer/Buffers
Oscillators		
Connor-Winfield	(708) 851-4722	
Fox	(888) GET-2FOX	
Motorola Semiconductor	(800) 441-2447	PLLs and Clock Distribution ICs
Pletronics	(206) 776-1880	A variety of oscillators, spectrum analyzers, etc.
Saronix	(415) 856-6900	
Valpey Fisher	(508) 435-6831 X607	
Clock Generators		
IC Works	(408) 922-0202	Clock Synthesizer