4 Mbit ROM + 1 Mbit / 256 Kbit SRAM ROM/RAM Combo

SST30VR041 / SST30VR043

Data Sheet

FEATURES:

- **ROM + SRAM ROM/RAM Combo**
  - SST30VR041: 512K x8 ROM + 128K x8 SRAM
  - SST30VR043: 512K x8 ROM + 32K x8 SRAM
- **ROM/RAM combo on a monolithic chip**
- **Equivalent ComboMemory (Flash + SRAM): SST31LF041A for code development and pre-production**
- **Wide Operating Voltage Range: 2.7-3.3V**
- **Chip Access Time**
  - SST30VR041 70 ns and 150 ns
  - SST30VR043 150 ns
- **Low Power Dissipation:**
  - Standby: 1.0 µW (Typical)
  - Operating: 3.0 mW (Typical)
- **Fully Static Operation**
  - No clock or refresh required
- **Three-state Outputs**
- **Packages Available**
  - 32-lead TSOP (8mm x14mm)

PRODUCT DESCRIPTION

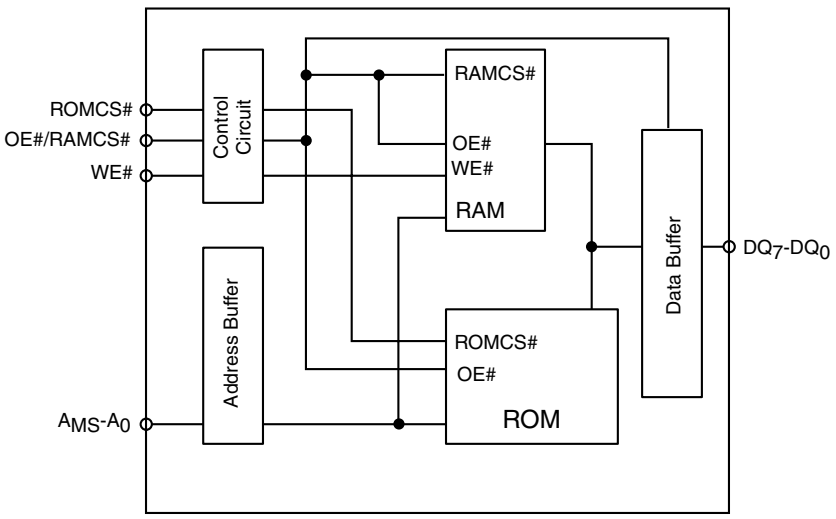
The SST30VR041/043 are ROM/RAM combo chips consisting of 4 Mbit Read-Only Memory (ROM) organized as 512 KByte and a Static Random Access Memory (SRAM) organized as either 128 or 32 KByte. Output Enable Input (OE#) is pin-shared with RAMCS# (RAM Enable Input) signal in order to maintain the standard 32-lead TSOP package.

The device is fabricated using SST's advanced CMOS low power process technology.

The SST30VR041/043 have an output enable input for precise control of the data outputs. It also has two (2) separate chip enable inputs for selection of either SRAM or ROM and for minimizing current drain during power-down mode.

The SST30VR041/043 is particularly well suited for use in low voltage (2.7-3.3V) supplies such as pagers, organizers and other handheld applications.

FUNCTIONAL BLOCK DIAGRAM



Note: A_{MS} = Most Significant Address

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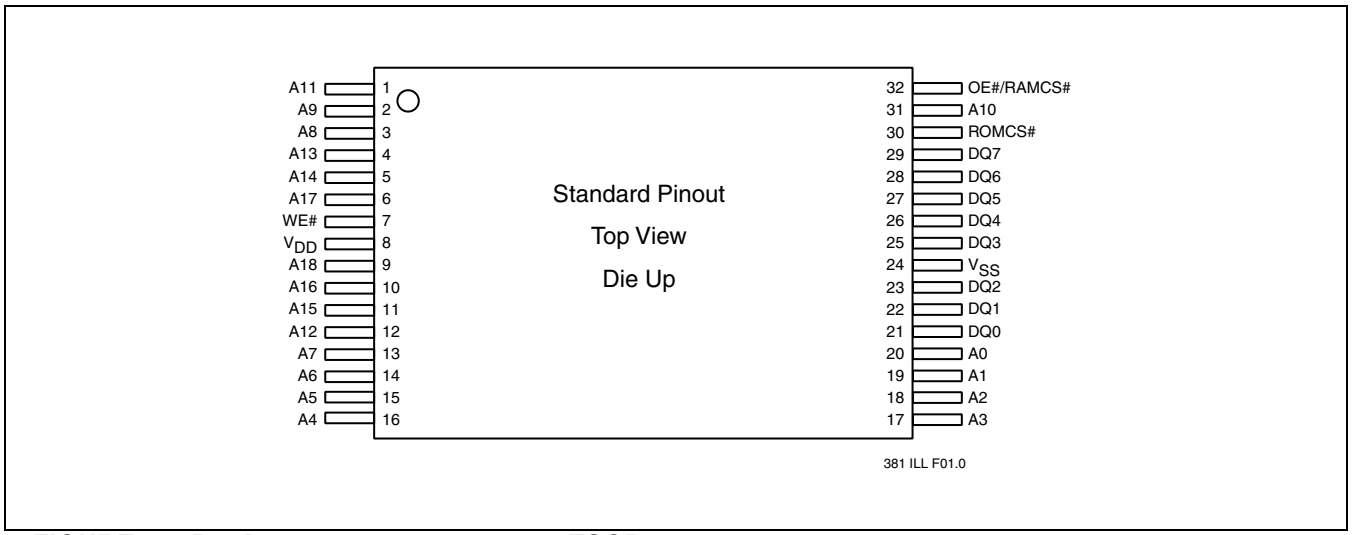

FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD TSOP

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name
A_{MS}[1]-A_0	Address Inputs: ROM: A_{MS} = A_{18} RAM: A_{MS} = A_{16} for SST30VR041 A_{14} for SST30VR043
WE#	Write Enable Input
OE#/RAMCS#	Output Enable/RAM Enable Input
ROMCS#	ROM Enable Input
DQ_7-DQ_0	Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground

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1. A_{MS} = Most significant address

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin Relative to V_{SS} . . . . . -0.5V to V_{DD}+0.5V
Voltage on V_{DD} Supply Relative to V_{SS} . . . . . -0.5V to 4.0V
Power Dissipation. 1.0W
Soldering Temperature (10 Seconds Lead Only) . . . . . 260°C

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Pulse Level	0-V_{DD}
Input & Output Timing Reference Levels	V_{DD}/2
Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF for 70 ns
Output Load	C_L = 100 pF for 150 ns

TABLE 2: RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	2.7	3.3	V
V_{SS}	Ground	0	0	V
V_{IH}	Input High Voltage	2.4	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	-0.3	0.3	V

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TABLE 3: DC OPERATING CHARACTERISTICS

		V_{DD} = 2.7-3.3V			
Symbol	Parameter	Min	Max	Units	Test Conditions
I_{DD1}	ROM Operating Supply Current		4.0+1.1(f)[1]	mA	ROMCS#=V_{IL}, RAMCS#=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=Opens
I_{DD2}	SRAM Operating Supply Current		2.5+1(f)[1]	mA	ROMCS#=V_{IH}, RAMCS#=V_{IL}, $I_{I/O}$=Opens
I_{SB}	Standby V_{DD} Current		10	µA	ROMCS# ≥ V_{DD}-0.2V, RAMCS# ≥ V_{DD}-0.2V V_{IN} ≥ V_{DD}-0.2V or V_{IN} ≤ 0.2V
I_{LI}	Input Leakage Current	-1	1	µA	V_{IN}=V_{SS} to V_{DD}
I_{LO}	Output Leakage Current	-1	1	µA	ROMCS#=RAMCS#=V_{IH} or OE#=V_{IH} or WE#=V_{IL}, $V_{I/O}$=V_{SS} to V_{DD}
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=1.0 mA
V_{OH}	Output High Voltage	2.2		V	I_{OH}=-0.5 mA

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1. f = Frequency of operation (MHz) = 1/cycle time

TABLE 4: CAPACITANCE (Ta = 25°C, f=1 Mhz)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	8 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

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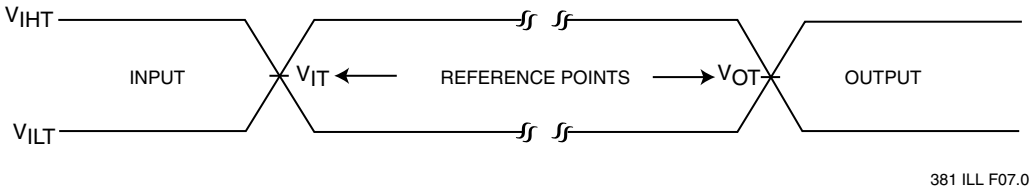
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 2: AC INPUT/OUTPUT REFERENCE WAVEFORMS

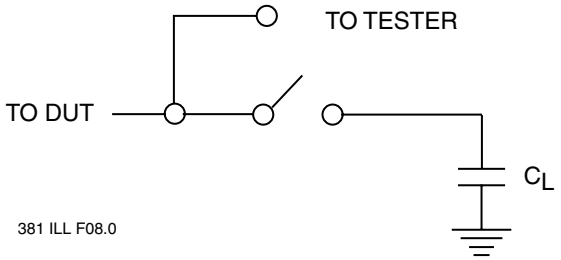


FIGURE 3: A TEST LOAD EXAMPLE

AC CHARACTERISTICS

I. ROM Operation

TABLE 5: READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	SST30VR041-70		SST30VR041/043-150		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		150		ns
T_{AA}	Address Access Time		70		150	ns
T_{CO}	Chip Select to Output		70		150	ns
T_{OE}	Output Enable to Valid Output		35		70	ns
T_{LZ}	Chip Select to Low-Z Output	0		0		ns
T_{OLZ}	Output Enable to Low-Z Output	0		0		ns
T_{HZ}	Chip Disable to High-Z Output		25		30	ns
T_{OHZ}	Output Disable to High-Z Output		25		30	ns
T_{OH}	Output Hold from Address Change	10		15		ns

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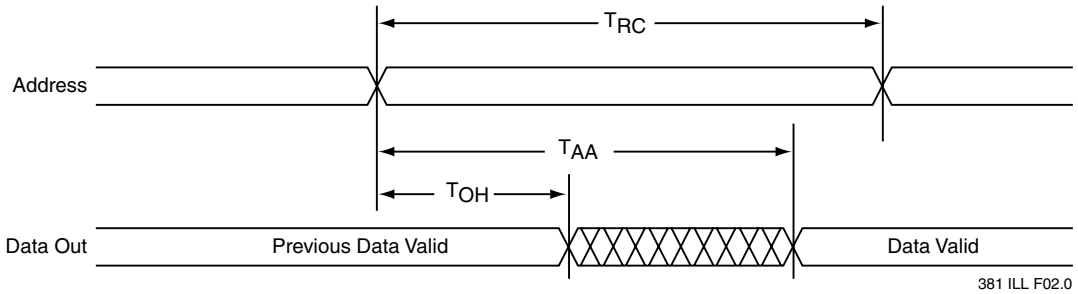
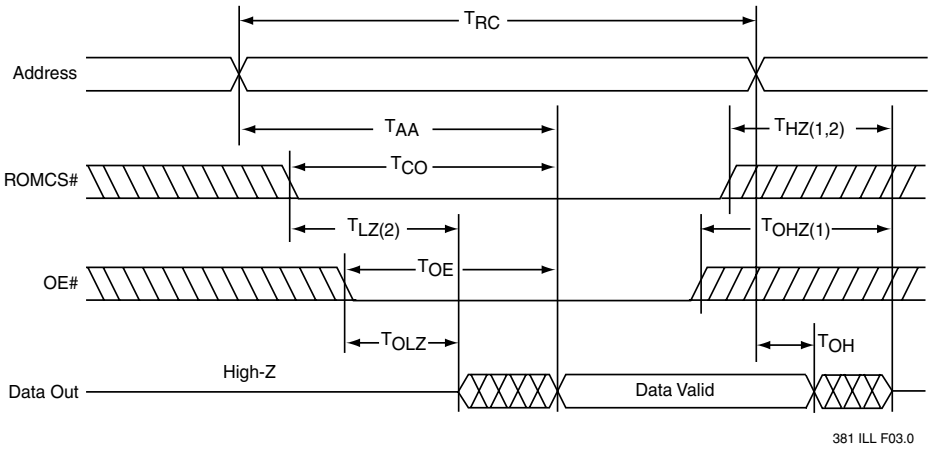


FIGURE 4: ROM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) (ROMCS# = OE# = V_{IL})



Notes: 1. T_{HZ} and T_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition T_{HZ}(max) is less than T_{LZ}(min) both for a given device and from device to device.

FIGURE 5: ROM READ CYCLE TIMING DIAGRAM (ROMCS# & OE# CONTROLLED)

II. SRAM Operation (ROMCS# = V_{IH})

TABLE 6: READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	SST30VR041-70		SST30VR041/043-150		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		150		ns
T_{AA}	Address Access Time		70		150	ns
T_{CO}	Chip Select to Output		70		150	ns
T_{LZ}	Chip Select to Low-Z Output	0		0		ns
T_{HZ}	Chip Disable to High-Z Output		25		30	ns
T_{OH}	Output Hold from Address Change	10		15		ns

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TABLE 7: WRITE CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	SST30VR041-70		SST30VR041/043-150		Units
		Min	Max	Min	Max	
T_{WC}	Write Cycle Time	70		150		ns
T_{CW}	Chip Select to End-of-Write	60		120		ns
T_{AW}	Address Valid to End-of-Write	60		120		ns
T_{AS}	Address Set-up Time	0		0		ns
T_{WP}	Write Pulse Width	60		120		ns
T_{WR}	Write Recovery Time	0		0		ns
T_{WHZ}	Write to Output High-Z		30		60	ns
T_{DW}	Data to Write Time Overlap	30		60		ns
T_{DH}	Data Hold from Write Time	0		0		ns
T_{OW}	End Write to Output Low-Z	0		10		ns

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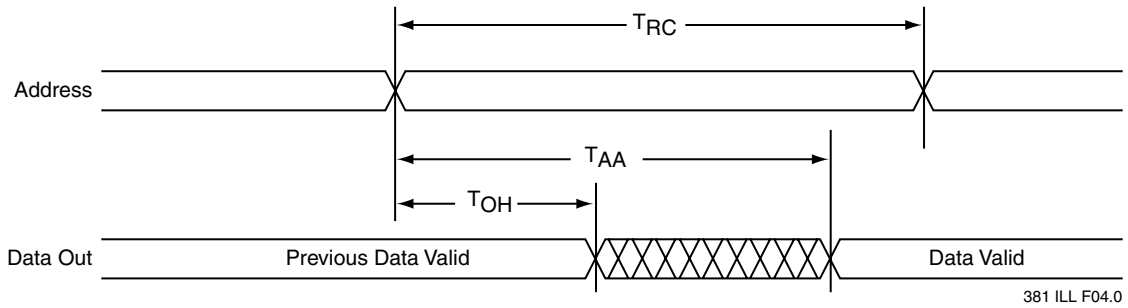
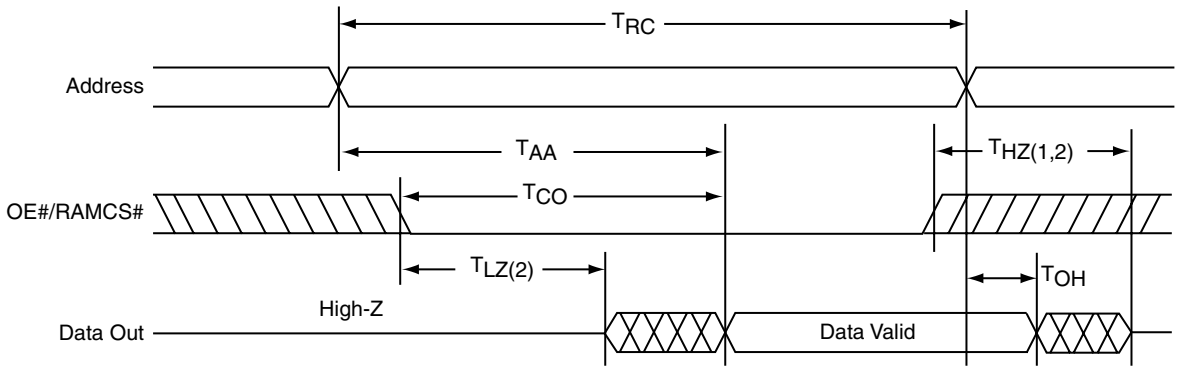
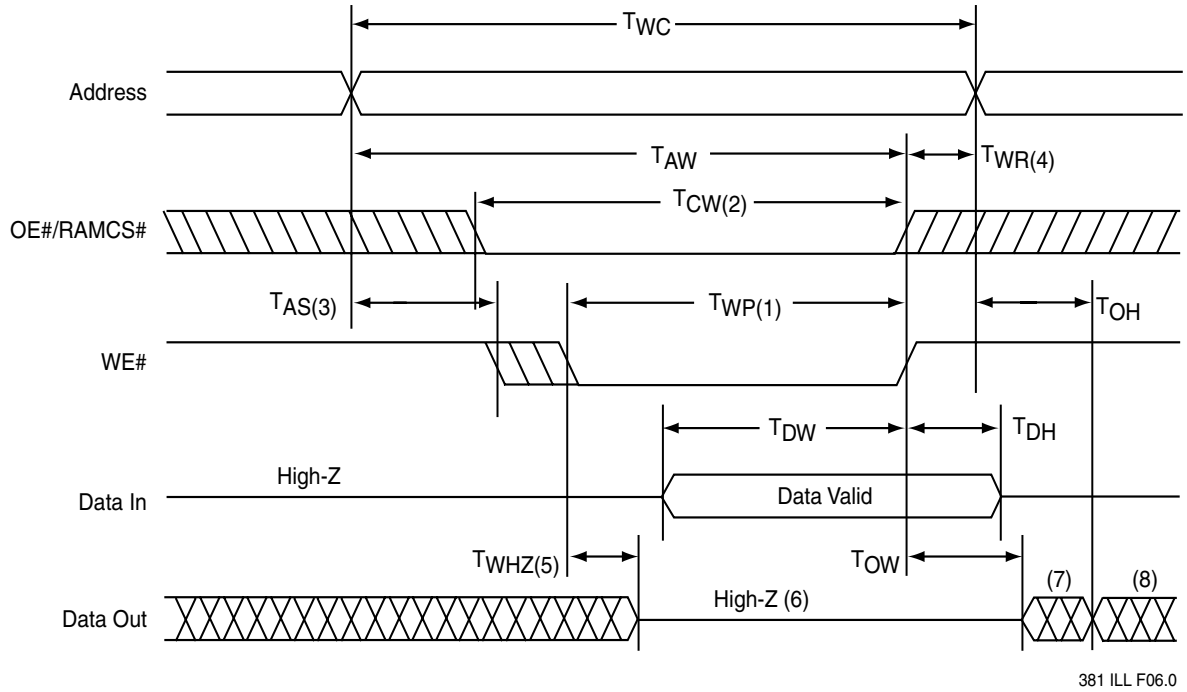


FIGURE 6: SRAM READ CYCLE TIMING DIAGRAM (ADDRESS CONTROLLED) (OE#/RAMCS# = V_{IL}, WE# = V_{IH})



Notes:
1. T_{HZ} and T_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are referenced to the V_{OH} or V_{OL}.
2. At any given temperature and voltage condition T_{HZ}(max) is less than T_{LZ}(min) both for a given device and from device to device.
3. WE# is high for Read cycle.

FIGURE 7: SRAM READ CYCLE TIMING DIAGRAM (OE#/RAMCS# CONTROLLED)



Notes:
1. A write occurs during the overlap (T_{WP}) of a low RAMCS# and low WE#. A write begins at the latest transition among RAMCS# going low and WE# going low: A write end at the earliest transition among RAMCS# going high and WE# going high, T_{WP} is measured from the beginning of write to the end of write.
2. T_{CW} is measured from the later of RAMCS# going low to the end of write.
3. T_{AS} is measured from the address valid to the beginning of write.
4. T_{WR} is measured from the end of write to the address change.
5. If RAMCS#, WE# are in the read mode during this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If RAMCS# goes low simultaneously with WE# going low or after WE# going low, the outputs remain high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of new address
9. ROMCS# = V_{IH}

FIGURE 8: SRAM WRITE CYCLE TIMING DIAGRAM

TABLE 8: FUNCTIONAL DESCRIPTION/TRUTH TABLE

Address Inputs	ROMCS#	OE#/RAMCS#[1] (Pin 32)	WE#	DQ_7-DQ_0	
X[2]	V_{IH}	V_{IH}	X	Z	Standby
A_{MS}[3]-A_0	V_{IL}	OE# (H)	X	Z	Output Floating
	V_{IL}	OE# (L)	X	D_{OUT}	ROM Read
Only A_{MS}[4]-A_0 are valid	V_{IH}	RAMCS# (L)	V_{IH}	D_{OUT}	RAM Read
	V_{IH}	RAMCS# (L)	V_{IL}	D_{IN}	RAM Write

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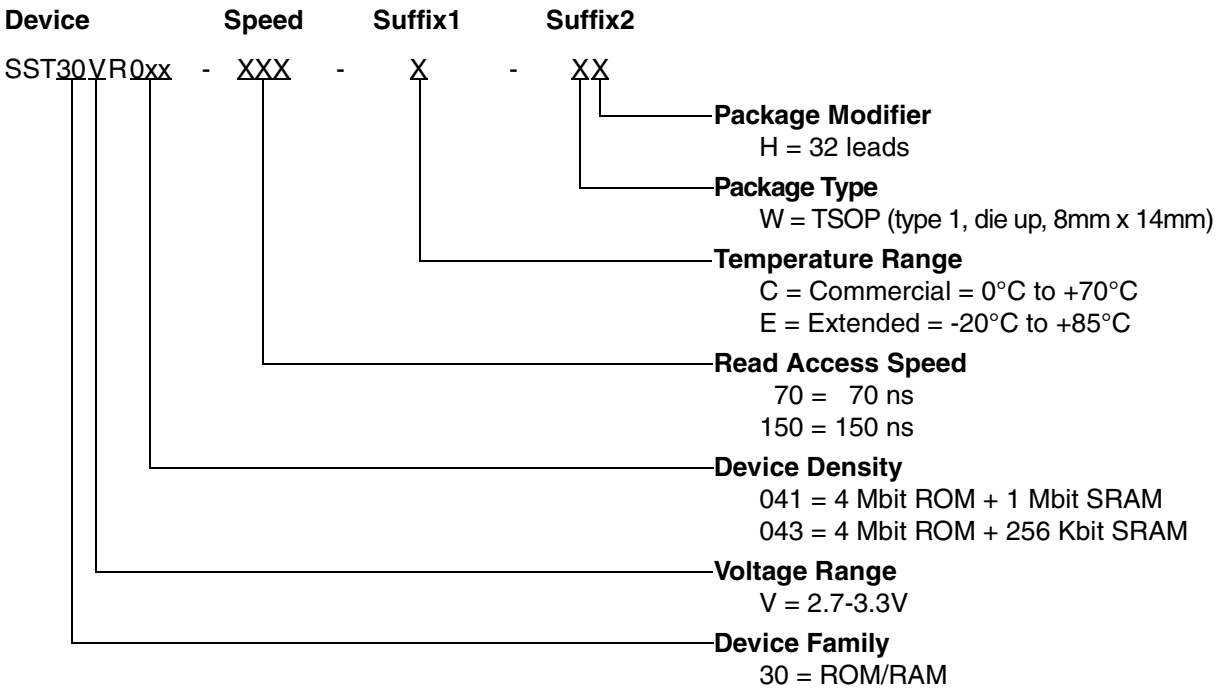
1. OE# & RAMCS# are pin-shared
2. X can be V_{IL} or V_{IH}, but no other value.
3. For ROM: $A_{MS} = A_{18}$ for SST30VR041 and SST30VR043
4. For SRAM:$A_{MS} = A_{16}$ for SST30VR041, A_{18}-A_{17} must be fixed to "V_{IL}" or "V_{IH}"
   $A_{MS} = A_{14}$ for SST30VR043, A_{18}-A_{15} must be fixed to "V_{IL}" or "V_{IH}"

PRODUCT ORDERING INFORMATION



Valid combinations for SST30VR041

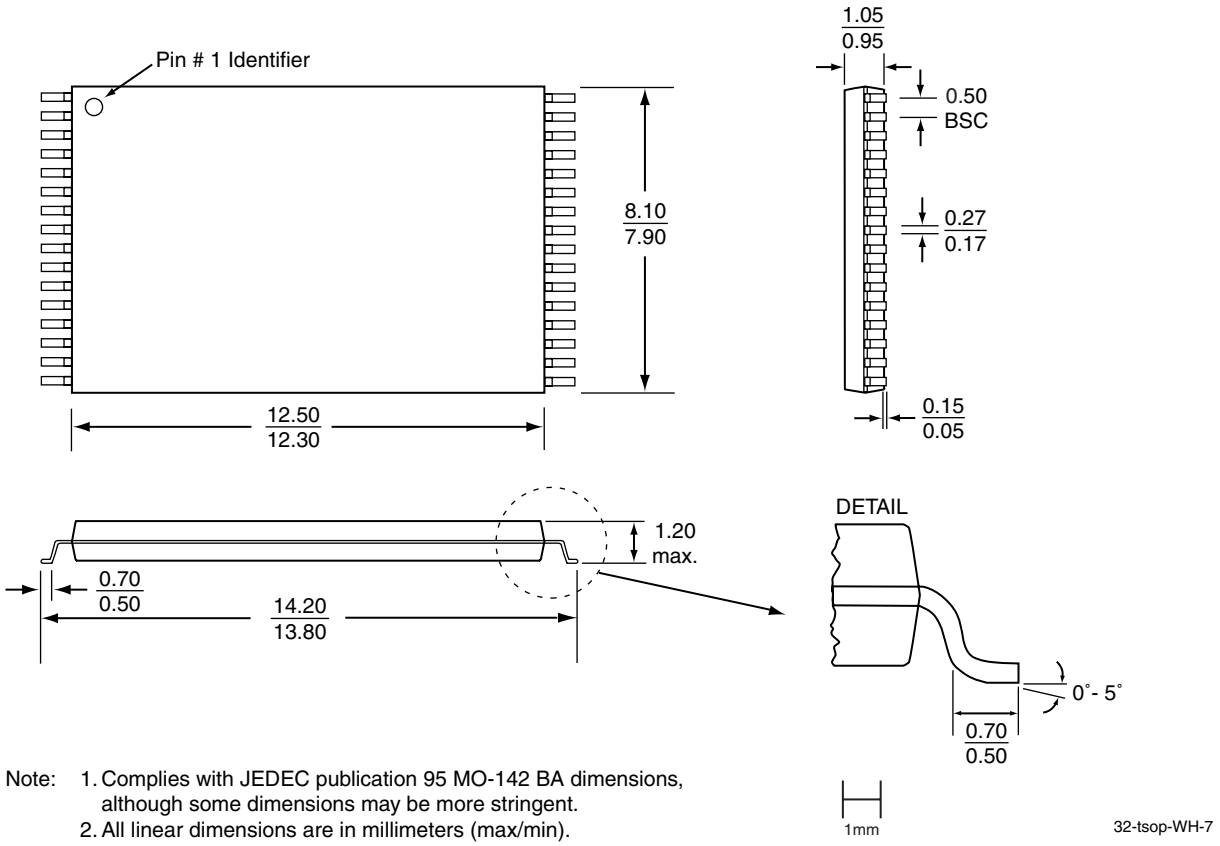
SST30VR041-70-C-WH
SST30VR041-150-C-WH
SST30VR041-70-E-WH
SST30VR041-150-E-WH

Valid combinations for SST30VR043

SST30VR043-150-C-WH
SST30VR043-150-E-WH

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH