Advance Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

960JX
Embedded 32-Bit RISC Processor

Features

- Functionally equivalent to *Intel*'s* 80960JA/JF embedded 32-bit microprocessor
- High-performance embedded architecture
- High-speed interrupt controller
- Two on-chip timers
- Two-way set associative instruction cache
- Direct mapped data cache
- On-chip stack frame cache
- On-chip data RAM
- High bandwidth burst bus
- Halt mode for low-power operation
- *IEEE*† 1149.1 (JTAG) boundary-scan compatibility
- Samples available for system emulation:
- 132-pin, plastic bumpered quad flat pack (BQFP)

Description

The 960JX provides high performance to low-cost 32-bit embedded applications. The 960JX features a generous instruction cache, data cache, and data RAM. It also has a fast interrupt mechanism, dual programmable timer units, and new instructions.

The processor combines two important peripherals: a timer unit and an interrupt controller. These and other hardware resources are programmed through memory-mapped control registers.

The timer unit offers two independent 32-bit timers for use as real-time system clocks and general-purpose system timing. These operate in either single-shot or auto reload mode and can generate interrupts.

The interrupt controller unit (ICU) has a flexible, low-latency means for processing and handling interrupts. The ICU provides full programmability of up to 240 interrupt sources into 31 priority levels and takes advantage of a cached priority table and optional routine caching to minimize interrupt latency. The ICU, independent from the core, compares the priorities of posted interrupts with the current process priority. The ICU also supports the integrated timer interrupts.

When using memory subsystems for low-cost embedded applications, substantial wait-state penalties are often required. The 960JX integrates considerable storage resources on-chip to decouple CPU execution from the external bus.

Both the instruction cache and data cache included in the 960JX can be configured for different sizes. For details, please refer to Figure 1 on the next page.

The 32-bit multiplexed burst bus provides a high-speed interface to system memory and I/O. A full complement of control signals makes the connection of the 960JX to external components easier. The user programs physical and logical memory attributes through memory-mapped control registers (MMRs). Physical and logical configuration registers enable the processor to operate with multiple combinations of bus width and byte ordering. The processor supports a homogeneous byte ordering model.

A halt mode is included to support applications where low power consumption is critical. The halt instruction enables the shutdown of instruction execution, which results in a power savings of up to 90%.

* *Intel* is a registered Intel Corporation.
† *IEEE* is a registered trademark of the Institute of Electrical and Electronics Engineers, Inc.

Description (continued)

The 960JX's testability features, which include ONCE (on-circuit emulation) mode and boundary scan (JTAG), provide a powerful environment for design debug and fault diagnosis.

Figure 1 shows the main blocks of the 960JX. Figure 2 shows pin assignments for a 132-pin BQFP package.

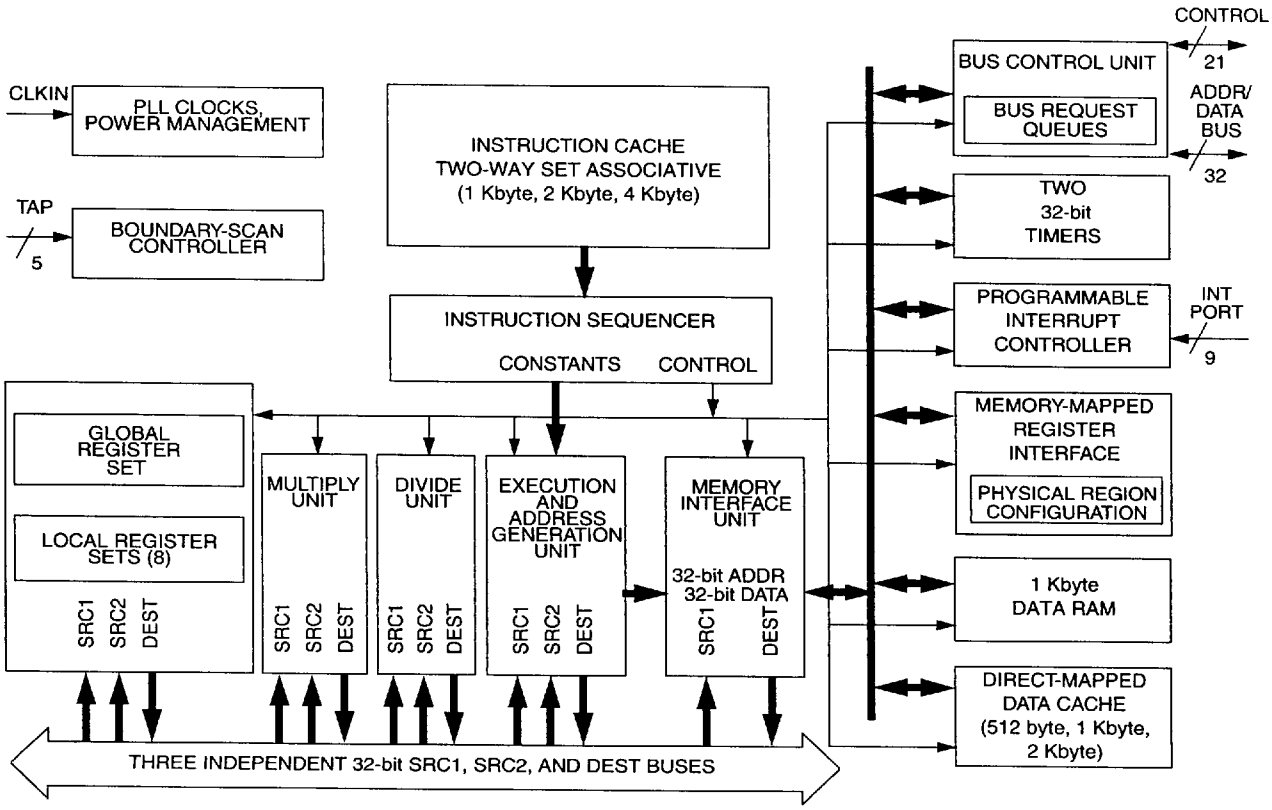

Figure 1. Block Diagram

Description (continued)

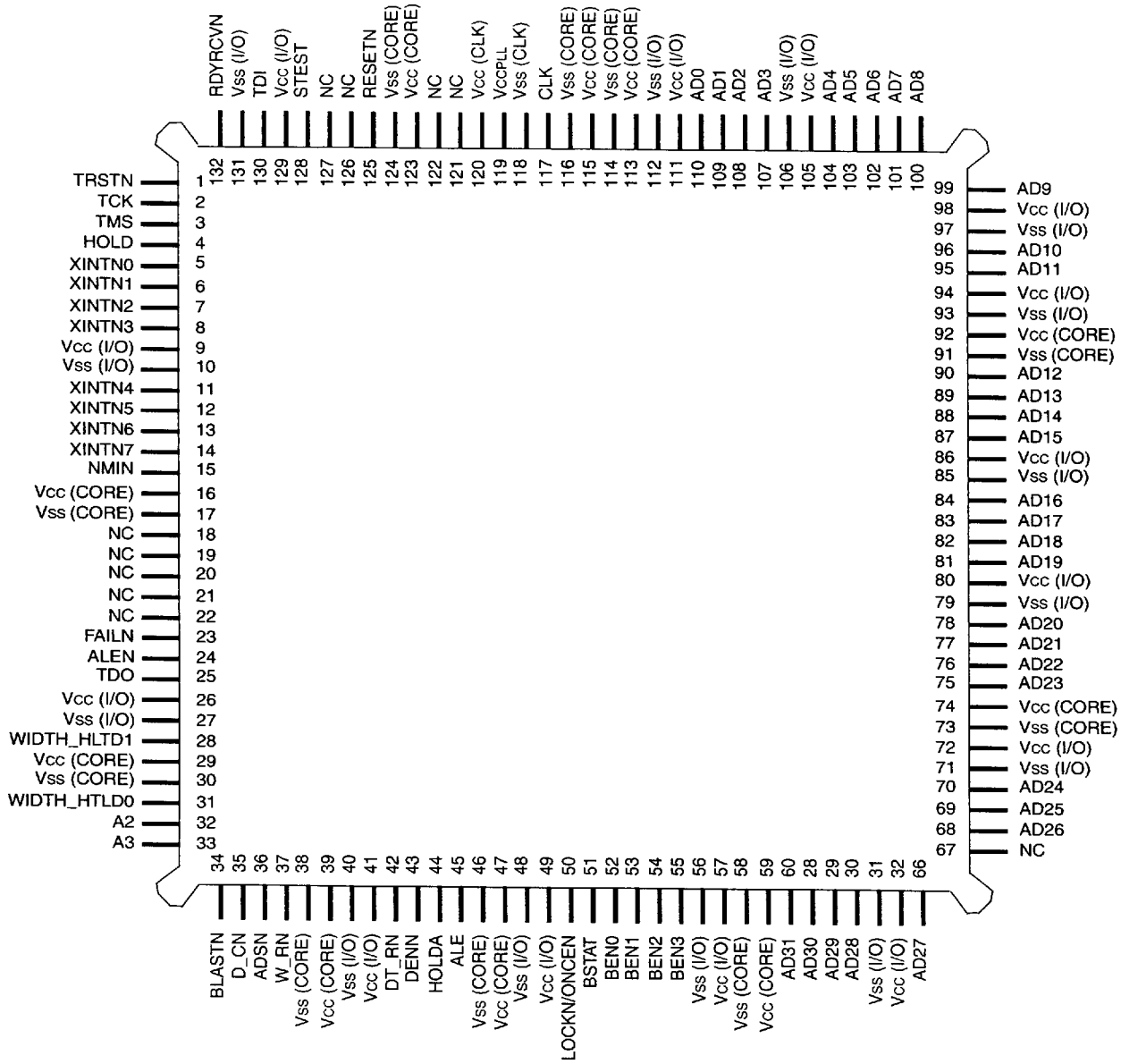

Figure 2. 132-Pin Bumpered Quad Flat Pack (BQFP) Pin Assignments

Signal Information

Table 1. Signal Descriptions — External Bus Signals

Signal	Type	Name/Description
ADI[31:0]	I	**Address/Data Bus.** Carries 32-bit physical addresses and 8-, 16-, or 32-bit data from memory. During an address (T_a) cycle, bits 2—31 contain a physical word address (bits 0—1 indicate SIZE, see below). During a data (T_d cycle), read data is present on one or more contiguous bytes, comprising ADI[31:24], ADI[23:16], ADI[15:8], and ADI[7:0]. SIZE, bits 0—1 of the ADI lines during a T_a cycle, specifies the number of data transfers during the bus transaction. **ADI1 ADI0 Bus Transfers** 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers When the processor enters halt mode, if the previous bus operation was a read, ADI[31:4] are driven with the last address value on the ADI bus; ADI[3:2] are driven with the value of A[3:2] from the last data cycle.
ADO[31:0]	O	**Address/Data Bus.** Carries 32-bit physical addresses and 8-, 16-, or 32-bit data to memory. During an address (T_a) cycle, bits 2—31 contain a physical word address (bits 0—1 indicate SIZE, see below). During a data (T_d) cycle, write data is present on one or more contiguous bytes, comprising ADO[31:24], ADO[23:16], ADO[15:8], and ADO[7:0]. During write operations, unused pins are driven to determinate values. SIZE, bits 0—1 of the ADO lines during a T_a cycle, specifies the number of data transfers during the bus transaction. **ADO1 ADO0 Bus Transfers** 0 0 1 Transfer 0 1 2 Transfers 1 0 3 Transfers 1 1 4 Transfers When the processor enters halt mode, if the previous bus operation was a write, ADO[31:2] are driven with the last data value on the ADO bus.
ADE[3:0]	O	**Address/Data Bus Enable (Active High).** Puts bus in output mode. **Signal Description** ADE3 Enables 31:24 ADE2 Enables 23:16 ADE1 Enables 15:8 ADE0 Enables 7:0
ALE	O	**Address Latch Enable (Active-High).** Indicates the transfer of a physical address. ALE asserts during a T_a cycle and deasserts before the beginning of the T_d state. It is active high and floats to a high-impedance state during a hold cycle.
ALEN	O	**Address Latch Enable Not (Active-Low).** Indicates the transfer of a physical address. ALEN is the inverted version of ALE.
ADSN	O	**Address Strobe Not (Active-Low).** Indicates a valid address and the start of a new bus access. The processor asserts ADSN for the entire T_a cycle. External bus control logic typically samples ADSN at the end of the cycle.

Signal Information (continued)

Table 1. Signal Descriptions — External Bus Signals (continued)

Signal	Type	Name/Description
A[3:2]	O	**Address 3:2.** Forms a partial demultiplexed address bus. For 32-bit memory accesses, the processor asserts address bits A[3:2] during Ta. The partial word address increments with each assertion of RDYRCVN during a burst. For 16-bit memory accesses, the processor asserts address bits A[3:1] during Ta with A1 driven on the BEN1 pin. The partial short word address increments with each assertion of RDYRCVN during a burst. For 8-bit memory accesses, the processor asserts address bits A[3:0] during Ta, with A[1:0] driven on BEN[1:0]. The partial byte address increments with each assertion of RDYRCVN during a burst.
BEN[3:0]	O	**Byte Enables Not (Active-Low).** Selects which of the up to four data bytes on the bus participate in the current bus access. Byte enable encoding is dependent on the bus width of the memory region accessed: 32-bit bus: BEN3 enables data on AD[31:24] BEN2 enables data on AD[23:16] BEN1 enables data on AD[15:8] BEN0 enables data on AD[7:0] 16-bit bus: BEN3 becomes byte high enable (enables data on AD[15:8]) BEN2 is not used (state is high) BEN1 becomes address bit 1 (A1) BEN0 becomes byte low enable (enables data on AD[7:0]) 8-bit bus: BEN3 is not used (state is high) BEN2 is not used (state is high) BEN1 becomes address bit 1 (A1) BEN0 becomes address bit 0 (A0) The processor asserts byte enables, byte-high enable, and byte-low enable during Ta. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during burst. They remain active through the last Td cycle. For accesses to 8- and 16-bit memory, the processor asserts the address bits in conjunction with A[3:2] described above.
WIDTH_HLTD[1:0]	O	**Width/Halted.** These signals denote the physical memory attributes for a bus transaction: **WIDTH_HLTD1** **WIDTH_HLTD0** 0 0 8 bits wide 0 1 16 bits wide 1 0 32 bits wide 1 1 processor halted The processor floats the WIDTH_HLTD pins whenever it relinquishes the bus in response to a HOLD request, regardless of prior operating state.
D_CN	O	**Data/Code Not.** Indicates that a bus access is a data access (1) or an instruction access (0). D_CN as the same timing as W_RN

Signal Information (continued)

Table 1. Signal Descriptions — External Bus Signals (continued)

Signal	Type	Name/Description
W_RN	O	**Write/Read Not.** During a Ta cycle, specifies whether the operation is a write (1) or read (0). It is latched on-chip and remains valid during Td cycles.
DT_RN	O	**Data Transmit/Receive Not.** Indicates the direction of data transfer to and from the address/data bus. It is low during Ta and Tw/Td cycles for a read, and it is high during Ta and Tw/Td cycles for write. DT_RN never changes state when DENN is asserted.
DENN	O	**Data Enable Not (Active-Low).** Indicates data transfer cycles during a bus access. DENN is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. DENN is used with DT_RN to provide control for data transceivers connected to data bus.
BLASTN	O	**Blast Last Not (Active-Low).** Indicates the last transfer in bus access. BLASTN is asserted in the last data transfer of burst and nonburst accesses. BLASTN remains active as long as wait-states are inserted via the RDYRCVN pin. BLASTN becomes inactive after the final data transfer in a bus cycle.
RDYRCVN	I	**Ready-Recover Not (Active-Low).** Indicates that data on AD lines can be sampled or removed. If RDYRCVN is not asserted during a Td cycle, the Td cycle is extended to the next cycle by inserting a wait-state (Tw). The RDYRCVN pin has an alternate function during the recovery (Tr) state. The processor continues to insert additional recovery states until it samples the pin high. This function allows slow external devices longer to float their buffers before the processor begins to drive address again.
LOCKN	O	**Bus Lock Not (Active-Low).** Indicates that an atomic read-modify-write operation is progressing. The LOCKN output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant HOLDA while it is asserting LOCKN. This prevents external agents from accessing memory involved in semaphore operations
ONCEN	I	**ONCE Mode Not (Active-Low).** The processor samples the ONCEN input during reset. If it is asserted low at the end of reset, the processor enters ONCEN mode. In ONCEN mode, the processor stops all clocks and floats all output pins. The pin has a weak internal pull-up that is active during reset to ensure normal operation if the pin is left unconnected.
LOCKNE	O	**Lock Not Enable (Active-High).** Puts LOCKN/ONCEN in LOCKN (output) mode.
HOLD	I	**Hold.** A request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it asserts HOLDA, floats the address/data and control lines, and enters the Th state. When HOLD is deasserted, the processor deasserts HOLDA and enters either the Ti or Ta state, resuming control of the address/data and control lines.
HOLDA	O	**Hold Acknowledge.** Indicates to an external bus master that the processor has relinquished control of the bus. The processor can grant HOLD requests and enter the Th state during reset and while halted as well as during regular operation.
BSTAT	O	**Bus Status.** Indicates that the processor may soon stall unless it has sufficient access to the bus. Arbitration logic can examine this signal to determine when an external bus master should acquire or relinquish the bus.

Signal Information (continued)

Table 2. Signal Descriptions — Processor Control Signals, Test Signals, and Power

Signal	Type	Name/Description
CLK	I	**Clock Input.** Provides the processor's fundamental time base. Both the processor core and the external bus run at the CLK rate. All input and output timing are specified relative to a rising CLK edge.
RESETN	I	**Reset Not (Active-Low).** Initializes the processor and clears its internal logic. During reset, the processor places the address data bus and control output pins in their idle (inactive) states. During reset, the input pins are ignored with the exception of ONCEN, STEST, and HOLD. The RESETN pin has an internal synchronizer. RESETN must be asserted a minimum of 10,000 CLK cycles before powerup with VCC and CLK stable to ensure predictable processor initialization during powerup. On warm reset, RESETN should be asserted for a minimum of 15 cycles.
STEST	I	**Self-Test.** Enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of reset. If STEST is asserted, the processor performs its internal self-test and the external bus confidence test. If STEST is deasserted, the processor performs only the external bus confidence test.
FAILN	O	**Fail Not (Active-Low).** Indicates a failure of the processor's built-in self-test performed during initialization. FAILN is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests. If self-test passes, the processor deasserts FAILN and commences operation from user code. If self-test fails, the processor asserts FAILN and then stops executing.
TCK	I	**Test Clock.** A CPU input that provides the clocking function for *IEEE* 1149.1 boundary-scan testing (JTAG). State information and data are clocked into the processor on the rising edge. Data is clocked out of the processor on the falling edge.
TDI	I	**Test Data Input.** This signal is the serial input for JTAG. TDI is sampled on the rising edge of TCK, during SHIFT-IR and SHIFT-DR states of the test access port.
TDO	O	**Test Data Output.** This signal is the serial output pin for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the test access port. At other times, TDO floats. TDO does not float during ONCE mode.
TRSTN	I	**Test Reset Not.** Asynchronously resets the test access port (TAP) controller function of *IEEE* 1149.1 boundary-scan testing (JTAG). If using the boundary scan feature, connect a pull-down resistor between this pin and ground. If the test access port will not be used, the pin can be tied directly to ground.
TMS	I	**Test Mode Select.** This signal is sampled at the rising edge of TCK to select the operation of the test logic for *IEEE* 1149.1 boundary scan testing.
VCC	—	**Power.** Intended for external connection to a VCC board plane.
VSS	—	**Ground.** Intended for external connection to a VSS board plane.
NC	—	**No Connect.** Do not make any system connections to these leads.

Signal Information (continued)

Table 3. Signal Descriptions — Interrupt Unit Signals

Signal	Type	Name/Description
XINTN[7:0]	I	**External Interrupt Not (Active-Low).** Used to request interrupt service. The signals can be configures in three different modes: **Dedicated Mode:** Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be low level or falling edge sensitive. **Expanded Mode:** All eight pins act as a vectored source. The interrupt signals are level-sensitive in this mode. **Mixed Mode:** The XINTN[7:5] signals act as dedicated sources and the XINTN[4:0] signals act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to 010 internally. Unused external interrupt pin should be connected to VCC.
NMIN	I	**Nonmaskable Interrupt Not (Active-Low).** Causes a nonmaskable interrupt event to occur. NMIN is the highest priority interrupt source and is falling edge triggered. If NMIN is unused, it should be connected to VCC.

Netlist Order

Inputs: ADI[31:0], RDYRCVN, ONCEN, HOLD, CLK, RESETN, STEST, TCK, TDI, TRSTN, TMS, XINTN[7:0], NMIN

Outputs: ADO[31:0], ADE[3:0], ALE, ALEN, ADSN, A[3:2], BEN[3:0], WIDTH_HLTD[1:0], D_CN, W_RN, DT_RN, DENN, BLASTN, LOCKN, HOLDA, BSTAT, FAILN, TDO

For additional information, contact your Microelectronics Group Account Manager or the following:
U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
Tel. (65) 778 8833, FAX (65) 777 7495
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
For data requests in Europe:
MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148
For technical inquiries in Europe:
CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 1344 865 900** (Bracknell UK),
FRANCE: **(33) 1 47 67 47 67** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)

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