SONET/SDH/ATM OC-48 1:8 RECEIVER S3042

FEATURES

- Micro-power Bipolar technology
- Complies with Bellcore and ITU-T specifications
- Supports 2.488 Gbps (OC-48)
- 8-bit LVDS data path
- Compact 100 TQFP/TEP package
- Diagnostic loopback mode
- Line loopback
- LVPECL Signal detect input
- Low jitter serial interface
- Single 3.3V supply

APPLICATIONS

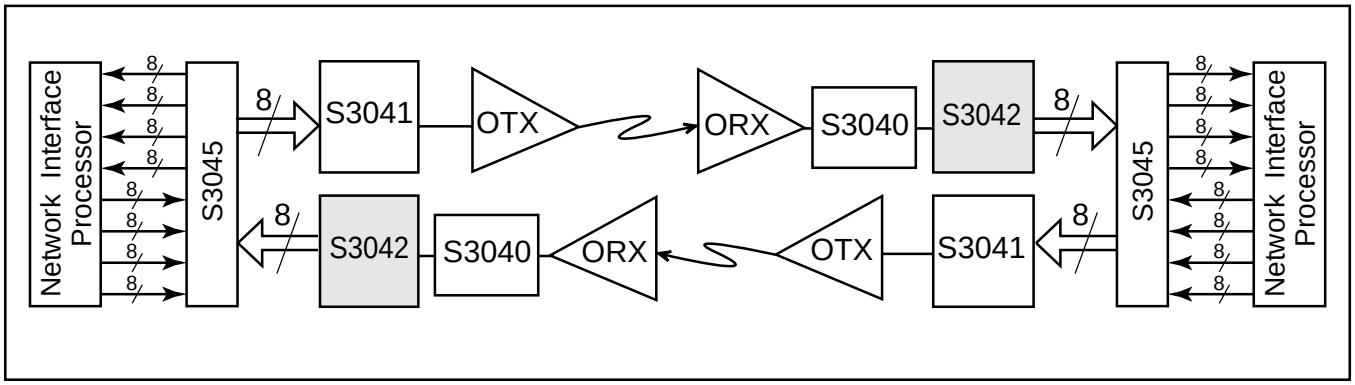
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexers
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3042 SONET/SDH receiver chip is a fully integrated deserialization SONET OC-48 (2.488 Gbps) interface device. The chip performs all necessary serial-to-parallel and framing functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications. Figure 1 shows a typical network application.

The low jitter serial interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3042 is packaged in a 100 TQFP/TEP, offering designers a small package outline.

Figure 1. System Block Diagram



S3042 OVERVIEW

The S3042 receiver implements SONET/SDH deserialization and frame detection functions. The block diagram in Figure 2 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip includes serial-to-parallel conversion and system timing. The system timing circuitry consists of management of the datastream, framing, and clock distribution throughout the front end.

The sequence of operations of the S3042 is as follows:

Receiver Operations:

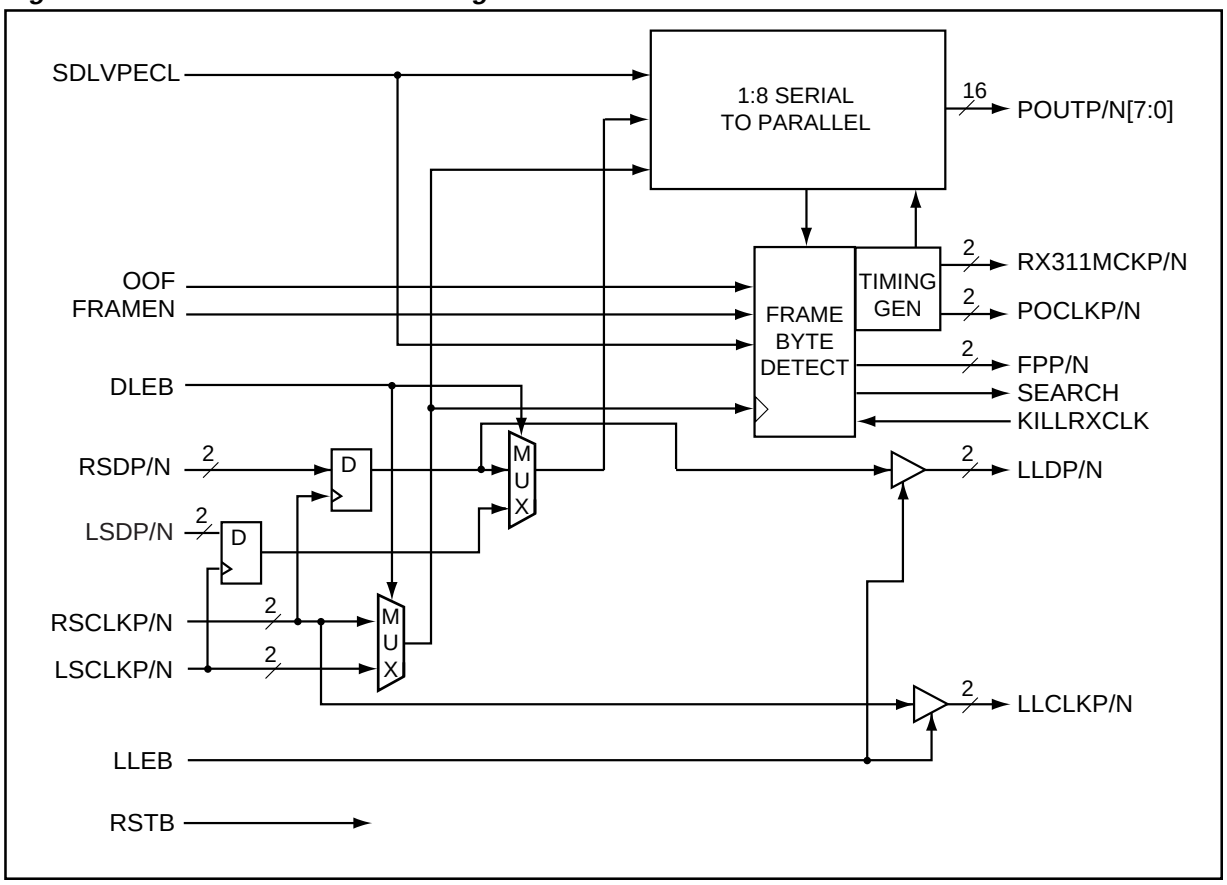
1. Serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 9.

Suggested Interface Devices

AMCC	S3040	Clock Recovery Device
AMCC	S3045	OC-48 to OC-12 Mux/Demux
AMCC	S3041	OC-48 Mux

Figure 2. S3042 Functional Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 3 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3042 chip supports OC-48 rate (2.488 Gbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-48 consists of 144 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 144 overhead and 4176 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 4.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 3. SONET Structure

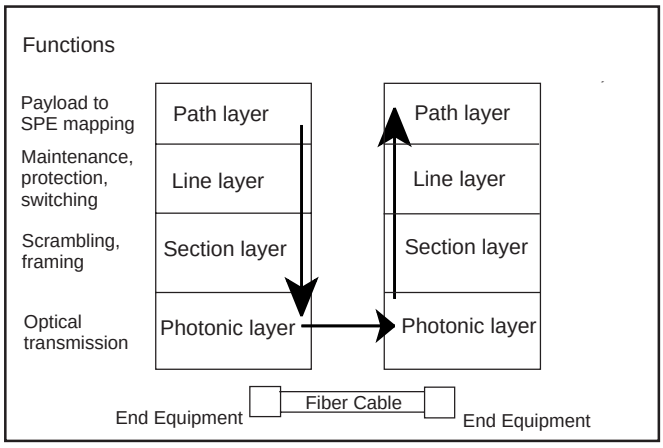
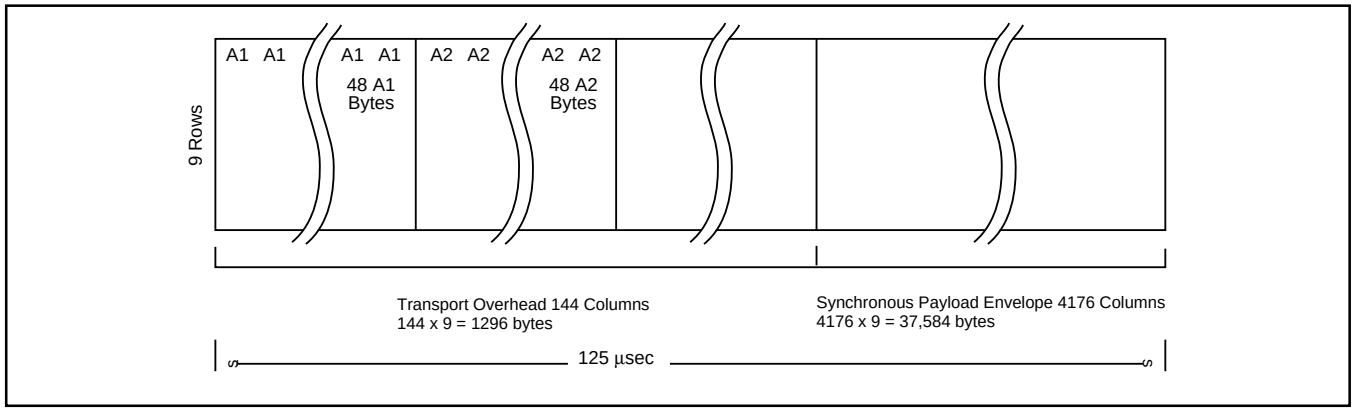


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 4. STS–48/OC–48 Frame Format



RECEIVER OPERATION

The S3042 receiver chip provides the first stage of digital processing of a receive SONET STS-48 bit-serial stream. It converts the bit-serial 2.488 Gbps data stream into a 311 Mbyte/sec byte-serial data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A Line Loopback (receiver to transmitter) is also provided. Both line and local loopback modes can be active at the same time.

Frame and Byte Boundary Detection

The Frame and Byte Boundary Detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by one A2 byte. Framing pattern detection is enabled by the Out-of-Frame (OOF) input. Detection is enabled by a rising edge on OOF when FRAMEN is active. It is disabled when a framing pattern is detected. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or looped transmitter data). During this time, the parallel data bus (POUT [7:0]) will not contain valid data. The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). The frame boundary is reported on the Frame Pulse (FP) output when any 32-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output. Frame detection can be immediately disabled by bringing FRAMEN inactive.

The probability that random data in an STS-48 stream will generate the 32-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 μs, even for extremely high bit error rates.

Serial-to-Parallel Converter

The Serial-to-Parallel Converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is low, a loopback from the transmitter (S3041) to the receiver (S3042) at the serial data rate can be set up for diagnostic purposes. The differential serial output data and clock from the transmitter (S3041) (LSD/LSCLK) is routed to the receiver (S3042) (LSD/LSCLK) in place of the normal data stream.

Line Loopback

The line loopback circuitry consists of alternate clock and data output drivers. For the S3042, enabling line loopback enables the LLD/LLCLK outputs. When the line loopback enable input (LLEB) is inactive, the LLD/LLCLK outputs are disabled. When LLEB is active, data and clock from the primary inputs (RSD/RSCLK) are transmitted on LLD/LLCLK, allowing a receive-to-transmit loopback to be established at the serial data rate. The S3042 LLD/LLCLK outputs should be connected to the S3041 LLD/LLCLK inputs.

Table 2 . Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Internally Biased Diff. LVPECL	I	71 70	Receive Serial Data. Serial data streams normally connected to an optical receiver module. These inputs are clocked by the rising RSCLK inputs. The RSD will be frame aligned and demultiplexed to an 8-bit parallel output <7:0>.
RSCLKP RSCLKN	Internally Biased Diff. LVPECL	I	66 65	Receive Serial Clock. Recovered clock signal that is synchronous with the RSD inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions.
OOF	LVTTL	I	55	Out of Frame. Indicator used to enable framing pattern detection logic in the S3042. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figure 10.)
SDLVPECL	LVPECL	I	52	LVPECL Signal Detect. Active high. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVPECL is inactive, the data on the Serial Data In (RSDP/N) pins will be internally forced to a constant zero. When SDLVPECL is active, data on the RSDP/N pins will be processed normally.
DLEB	LVTTL	I	46	Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is inactive, the S3042 device uses the primary data (RSD) and clock (RSCLK) inputs. When active, the S3042 device uses the diagnostic loopback data (LSD) and clock (LSCLK) from the transmitter.
RSTB	LVTTL	I	45	Master Reset. Reset input for the device. Active Low. During reset, POCLK and RX311MCK do not toggle.
LLEB	LVTTL	I	47	Line Loopback Enable. Active Low. Selects Line Loopback. When LLEB is active, the S3042 will enable the data on the LLD/LLCLK outputs.
LSDP LSDN	Externally Biased Diff. LVPECL	I	85 86	Loopback Serial Data. Inputs normally provided from a companion S3041 device. Used to implement a diagnostic loopback.
LSCLKP LSCLKN	Externally Biased Diff. LVPECL	I	76 77	Loopback Serial Clock. Inputs normally provided from a companion S3041 device. Used to implement a diagnostic loopback.
KILLRXCLK	LVTTL	I	53	Kill Receive Clock Input. For normal operation set KILLRXCLK "High." When this input is low, it will force RX311MCK and POCLK outputs to a logic "0" state.
FRAMEN	LVTTL	I	54	Frame Enable Input. For normal operation set FRAMEN High. This enables the frame detector circuit to detect A1 A2 alignment and lock to word boundary. When this input is Low, it will disable the frame detector circuit and it will lock on the last byte alignment state.

Table 3. Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
POUTN7 POUTP7 POUTN6 POUTP6 POUTN5 POUTP5 POUTN4 POUTP4 POUTN3 POUTP3 POUTN2 POUTP2 POUTN1 POUTP1 POUTN0 POUTP0	LVDS	O	14 15 16 17 18 19 20 21 28 29 30 31 32 33 34 35	Parallel Output. Parallel data bus, a 311 Mbps word, aligned to the parallel output clock (POCLK). POUT<7> is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT<0> is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT<7:0> is updated on the falling edge of POCLK.
LLDP LLDN	Diff. LSCML	O	99 100	Line Loopback Data. A retimed version of the incoming data stream [RSD]. Enabled by LLEB.
LLCLKP LLCLKN	Diff. LSCML	O	90 91	Line Loopback Clock. A buffered version of the RSCLK input. Enabled by LLEB.
FPP FPN	LVDS	O	37 36	Frame Pulse. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle during the third A2 byte when a 32-bit sequence matching the framing pattern is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high during the third A2 byte when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.
POCLKP POCLKN	LVDS	O	13 12	Parallel Output Clock. A 311MHz nominally 50% duty cycle, byte rate output clock that is aligned to POUT<7:0> byte serial output data. POUT<7:0> and FP are updated on the falling edge of POCLK.
RX311MCKP RX311MCKN	LVDS	O	39 38	Receive Free Running 311MHz clock output. This clock is generated by dividing the RSCLK signal by eight.
SEARCH	LVTTL	O	44	A1 A2 Frame Search Output. A High on this output pin indicates the frame detection circuit is activated and it is searching for a new A1 A2 byte alignment. This output will be High during the entire period of A1 A2 frame search. Once a new alignment is found, this signal will remain High for a minimum of one 311MHz clock period beyond the third A2 byte before it will be set to Low.

Table 4. Common Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
COREGND	GND		6, 7, 58, 59, 61, 63, 88, 89	Core Ground
COREVCC	+3.3V		4, 5, 60, 62, 64, 87	Core VCC
PECLVCC	+3.3V		69, 74, 75, 78, 79, 82, 92, 95, 96	PECL VCC
PECLGND	GND		67, 68, 72, 73, 80, 81, 83, 84, 93, 94, 97, 98	PECL Ground
TTLVCC	+3.3V		56 57	TTL VCC
TTLGND	GND		49 50	TTL Ground
LVDSGND	GND		10, 11, 24, 25, 26, 27, 40, 41	LVDS Ground
LVDSVCC	+3.3V		8, 9, 22, 23, 42, 43	LVDS VCC
NC			1, 2, 3, 48, 51	Not Connected

Figure 5. S3042 Pinout

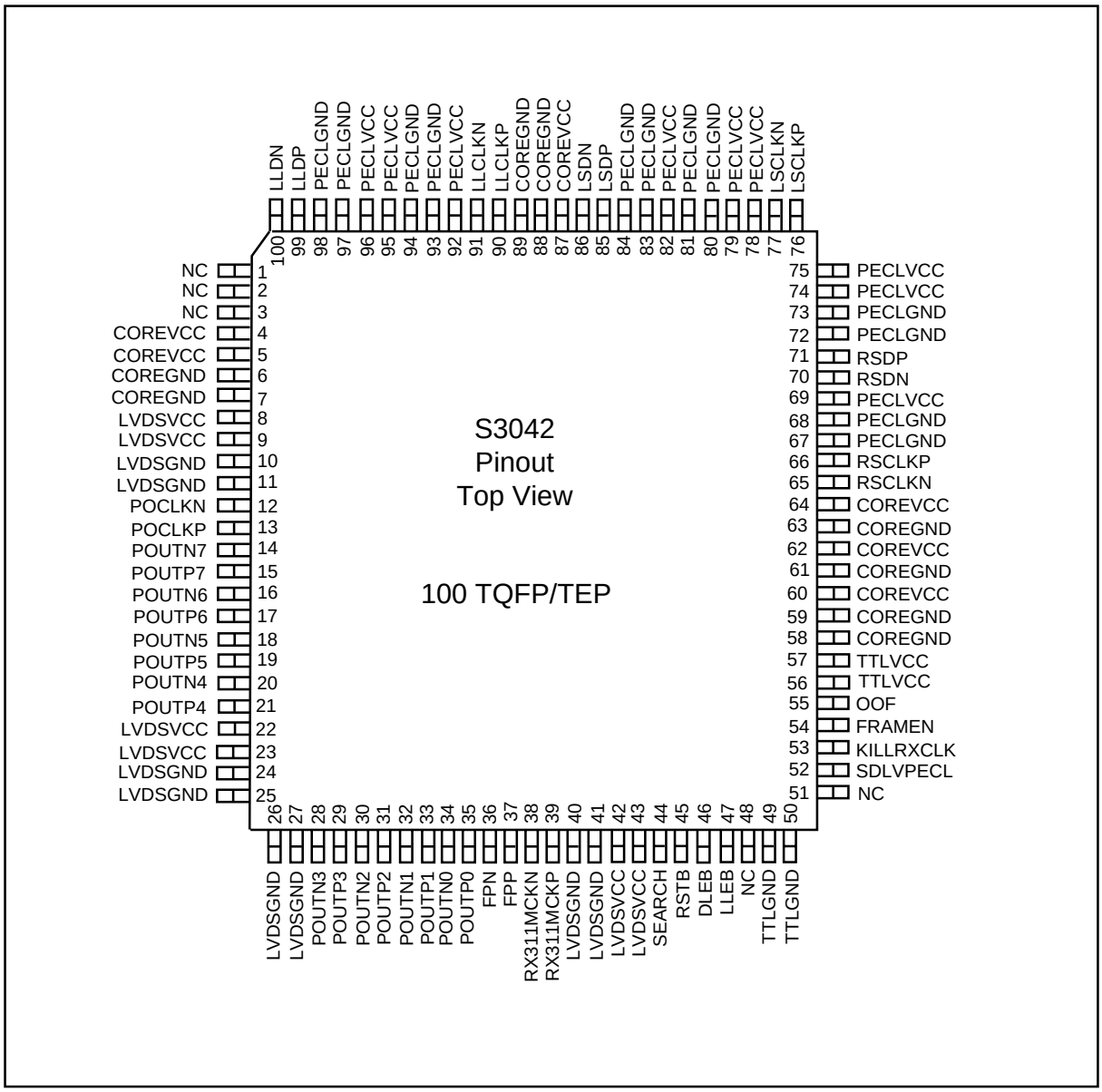
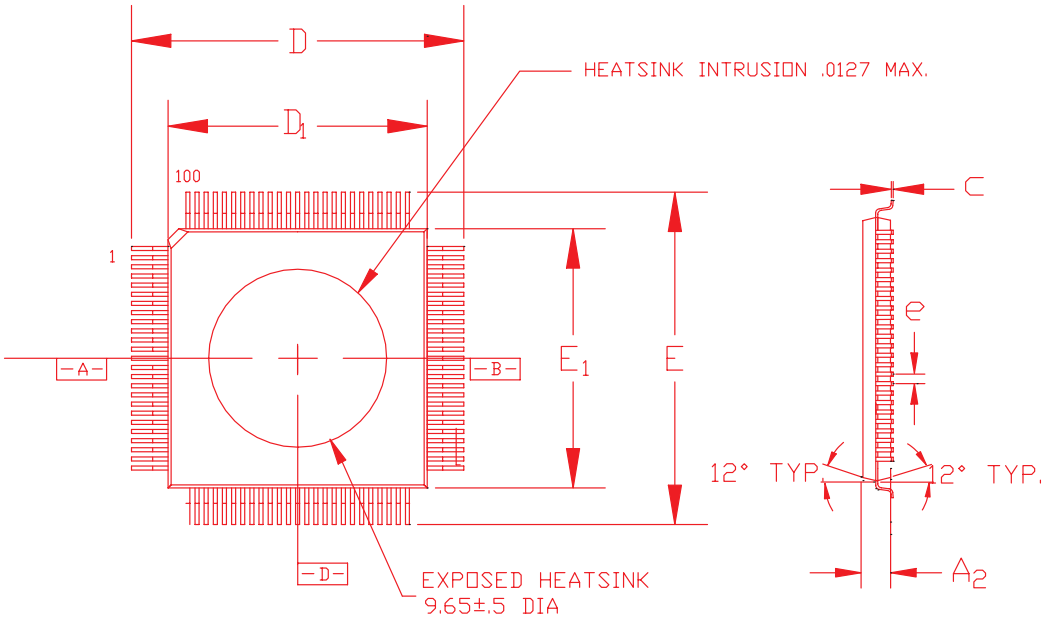
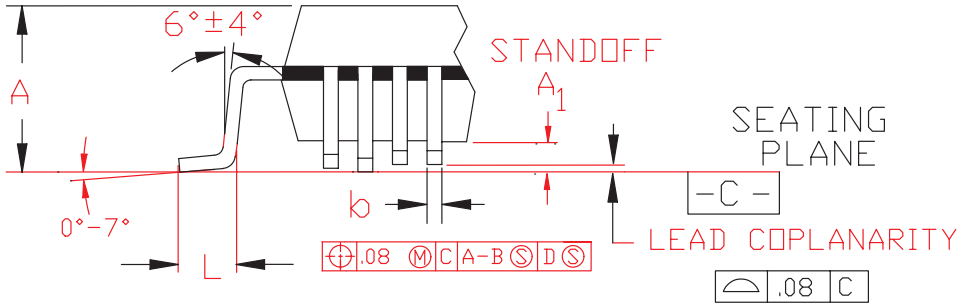


Figure 6. 100 TQFP/TEP Package



TOP VIEW



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN		0.05	1.35	15.80	13.95	15.80	13.95	0.50	0.17	0.50 BSC.	
NOM			1.40	16.00	14.00	16.00	14.00	0.60	0.22		
MAX	1.60	0.15	1.45	16.20	14.05	16.20	14.05	0.75	0.27		0.17

Thermal Management

Device	Max Power	Θja
S3042	1.11 W	33° C/W

Table 5. Differential Low Swing CML Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Low Swing CML Output LOW Voltage	V_{CC} -0.50		V_{CC} -0.25	V	100Ω line-to-line.
V_{OH}	Low Swing CML Output HIGH Voltage	V_{CC} -0.20		V_{CC} -0.05	V	100Ω line-to-line.
$\Delta V_{OUTDIFF}$	Low Swing CML Serial Output Differential Voltage Swing	360		800	mV	100Ω line-to-line. See Figure 13.
$\Delta V_{OUTSINGLE}$	Low Swing CML Serial Output Single-ended Voltage Swing	180		400	mV	100Ω line-to-line. See Figure 13.

Table 6. Internally Biased LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 7. Externally Biased LVPECL Input DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{BIAS}	LVPECL DC Bias Voltage	V_{CC} -1.2		V_{CC} -0.8	V	Inputs open.
V_{IL}	LVPECL Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.35	V	
V_{IH}	LVPECL Input HIGH Voltage	V_{CC} -1.20		V_{CC} -0.05	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1200	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Single-ended Input Voltage Swing	150		600	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 8. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with Respect to GND	-0.5		+4.0	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
ESD Sensitivity[1]	Under 500			V

1. Human body model.

Table 9 Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-40		85	˚C
Voltage on V_{CC} with Respect to GND	3.13	3.3	3.47	V
Voltage on any LVPECL Input Pin	V_{CC} -2		V_{CC}	V

Table 10. Power Consumption

Parameter	Min	Typ	Max	Units
ICC[1]		200	260	mA

1. Add 60 mA for line loopback active.

Table 11. LVTTL Input/Output DC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	2.0		TTL V_{CC}	V	TTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	TTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.2			V	V_{IH} = Min. V_{IL} = Max. I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{IH} = Min. V_{IL} = Max. I_{oL} = 4 mA

Table 12. LVDS Input/Output Characteristics[1]

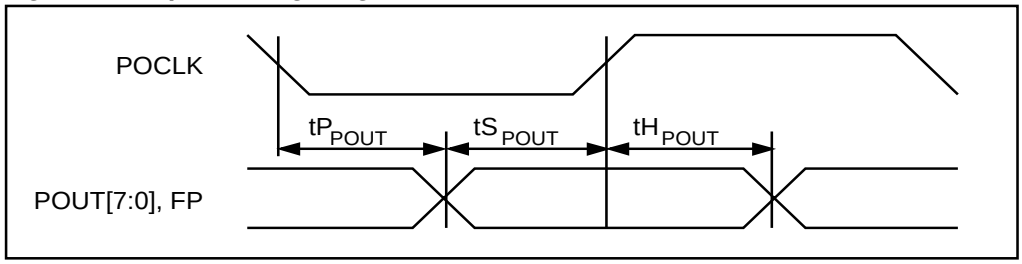
Symbol	Description	Min	Typ	Max	Unit	Conditions
V_{KH}	High I/O Clamp Voltage	0.15		1.5	V	I_I = Io = +100µA $V_{LVDSVCC}$ = 0V
V_{KL}	Low I/O Clamp Voltage	-1.5		-0.15	V	I_I = Io = -100µA $V_{LVDSVCC}$ = 0V
V_{OH}	Output High Voltage	1.00		1.80	V	V_{IH} = Min V_{IL} = Max
V_{OL}	Output Low Voltage	0.700		1.40	V	V_{IH} = Min V_{IL} = Max
$V_{OUTDIFF}$[2]	Output Differential Voltage	460	740	900	mV	V_{IH} = Max V_{IL} = Min
$V_{OUTSINGLE}$	Output Single-ended Voltage	230	370	450	mV	V_{IH} = Max V_{IL} = Min

1. Output loading is 275Ω to GND and 100Ω line-to-line.
2. See Figure 13.

Table 13. AC Receiver Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Duty Cycle	40	60	%
tP_{POUT}	POCLK Low to POUT [7:0] Valid Prop. Delay	-500	+500	ps
tS_{POUT}	POUT[7:0] and FP Set-up Time w.r.t. POCLK	1		ns
tH_{POUT}	POUT[7:0] and FP Hold Time w.r.t. POCLK	1		ns
tS_{RSD}	RSD/LSD Set-up Time w.r.t. RSCLK/LSCLK	75		ps
tH_{RSD}	RSD/LSD Hold Time w.r.t. RSCLK/LSCLK	75		ps
	LLCLK Duty Cycle	40	60	%
tP_{LLD}	LLCLK Low to LLD Valid Propagation Delay	-100	100	ps
	RSCLK/LSCLK Duty Cycle	45	55	%
	Low Swing CML Output Rise/Fall Time 20 to 80% 50Ω to VCC Load		150	ps
tS_{LLD}	LLD Setup Time w.r.t. LLCLK	100		ps
tH_{LLD}	LLD Hold Time w.r.t. LLCLK	100		ps

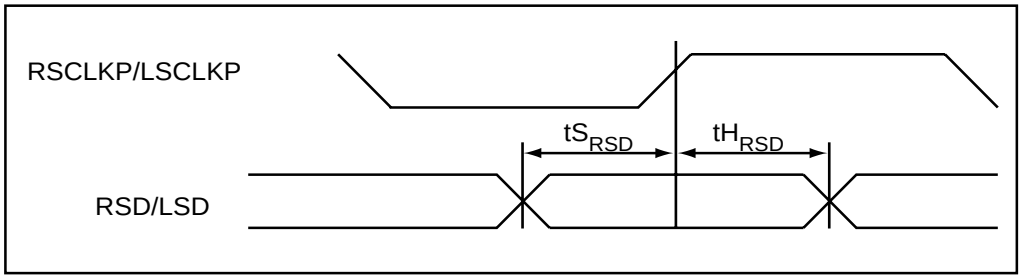
Figure 7. Output Timing Diagram



Notes on LVDS Output Timing:

1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the output.

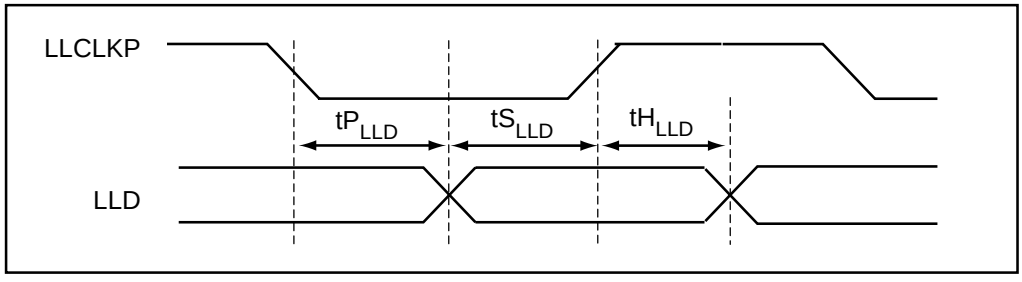
Figure 8. Receiver Input Timing Diagram



Notes on High-Speed LVPECL Input Timing:

1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Figure 9. LLD Output Timing



1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the output.

RECEIVER FRAMING

Figure 10 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF. The byte alignment is made during the A1 data sequence, resulting in correct byte alignment on the outgoing data bus (POUT[7:0]). Frame boundary is recognized upon receipt of the first A2 byte, and is reported via the frame pulse being set high for one POCLK cycle concurrent with the third A2 byte.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP pulse.

Figure 11 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP pulse.

Figure 12 shows the frame and byte boundary detection activation by a rising edge of FRAMEN, and deactivated by the FRAMEN input.

Figure 12 also shows the frame and byte boundary detection activation by a rising edge on FRAMEN, and deactivation by the first FP pulse.

Figure 10. Frame and Byte Detection

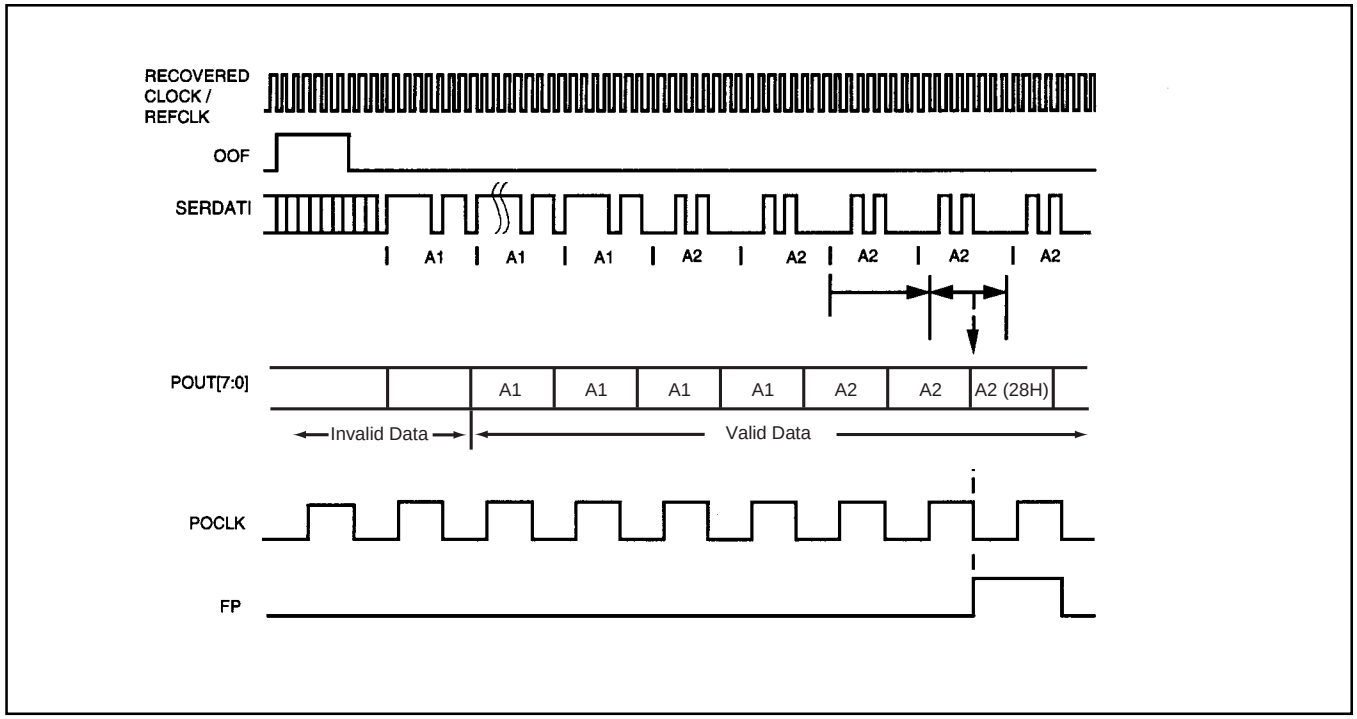


Figure 11. OOF Timing (FRAMEN = 1)

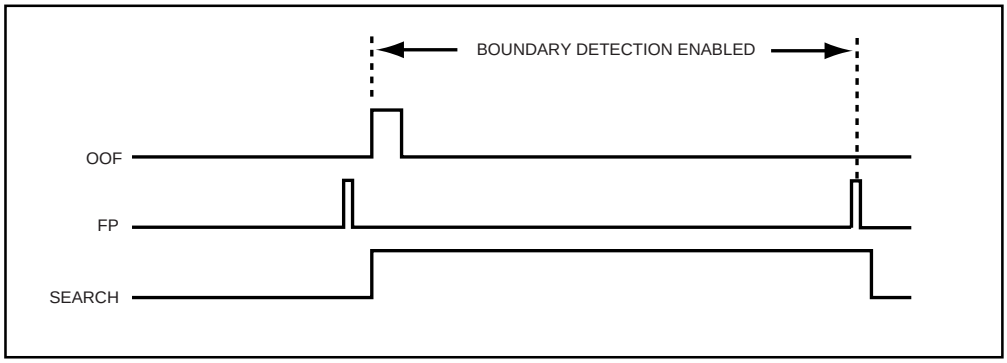


Figure 12. FRAMEN Timing (OOF = 1)

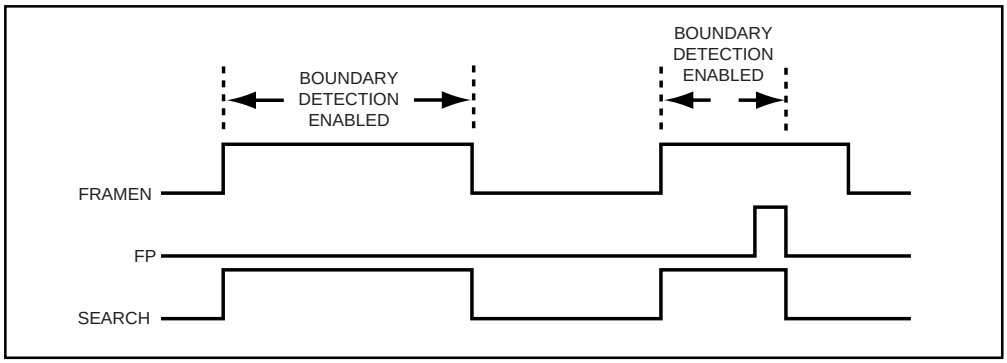


Figure 13. Differential Voltage Measurement

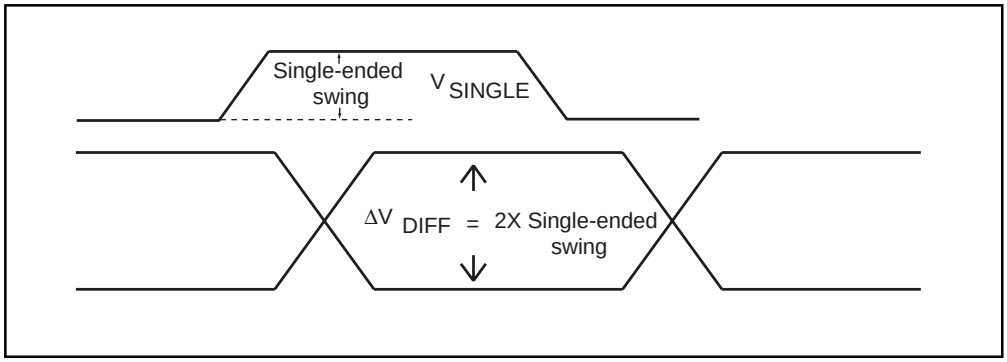


Figure 14. +5V Differential PECL Driver to S3042 Input AC Coupled Termination

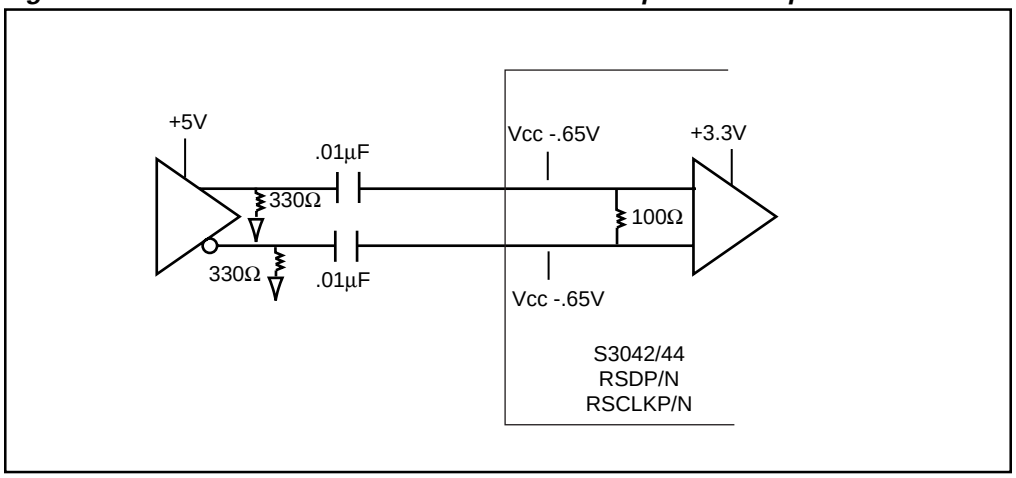


Figure 15. S3040 to S3042/S3044 Terminations

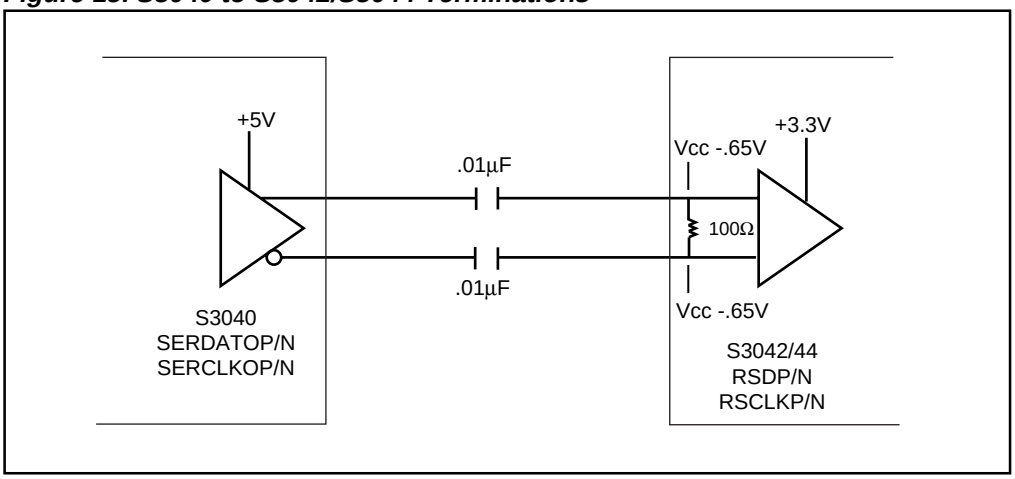


Figure 16. S3041 to S3042 for Diagnostic Loopback

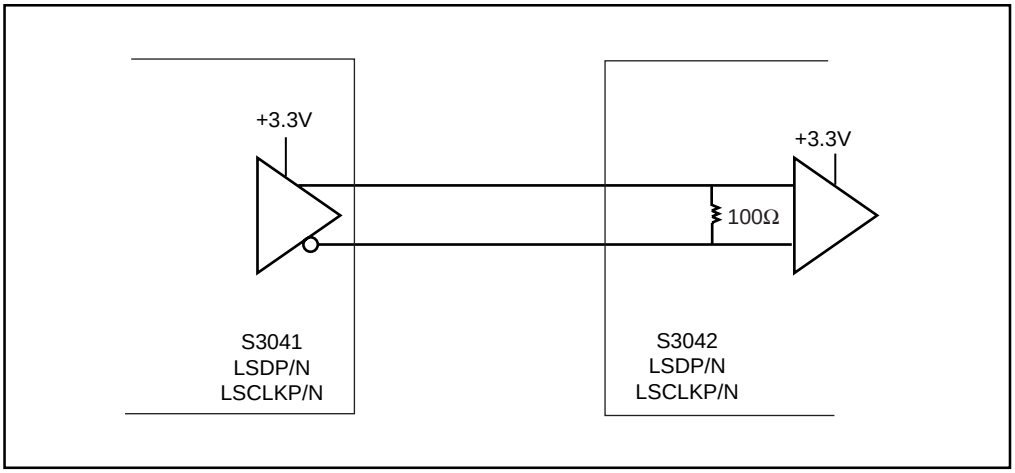


Figure 17. S3042 LVDS Driver to S3045 LVDS Driver

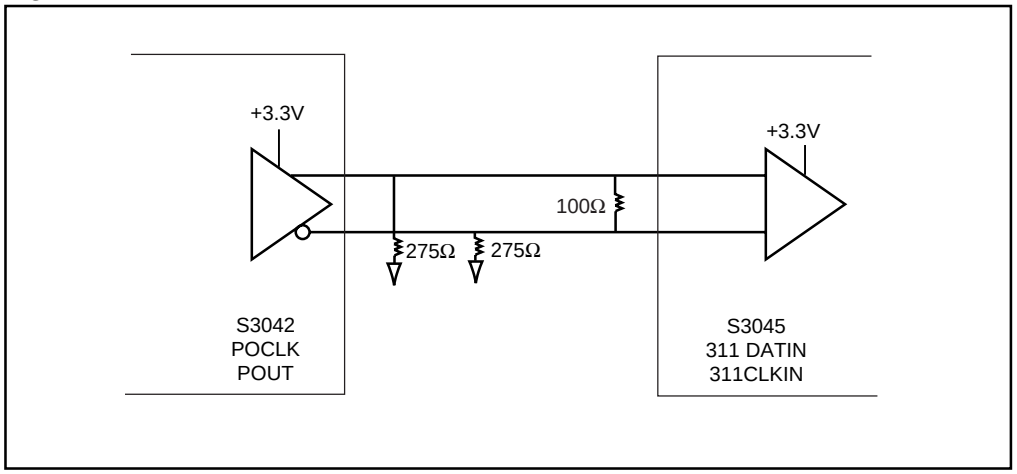
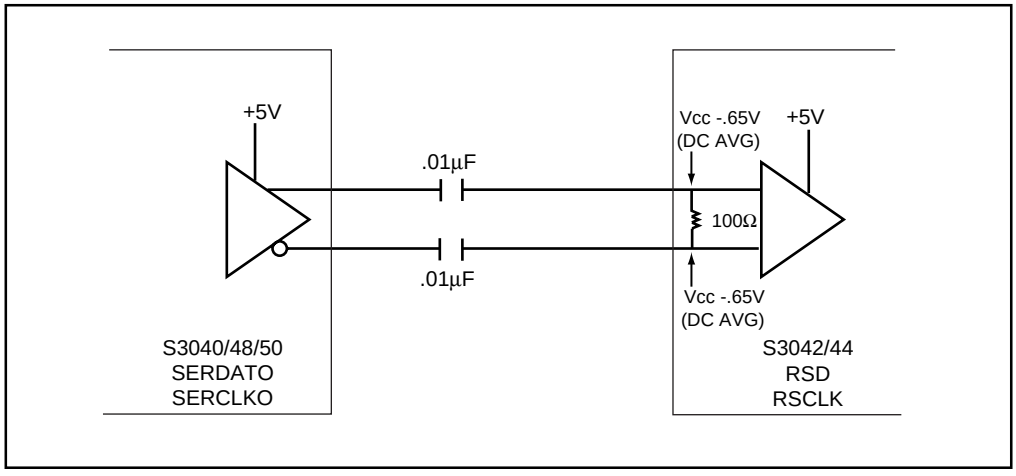
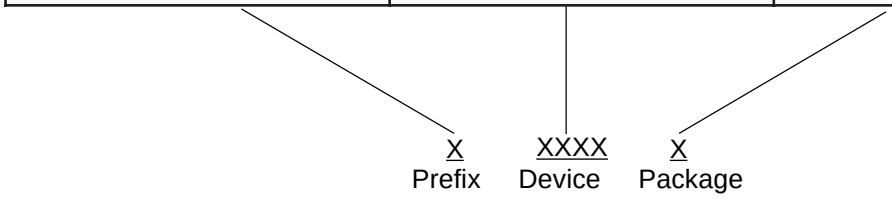


Figure 18. S3040/48/50 +5V PECL Output to CML Input AC Coupled Termination



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3042	A – 100 TQFP/TEP



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