M32C/80 Series

[CAN] Effects of PLL jitters on CAN communication

Introduction

This document describes the phase correction mechanism of the PLL frequency synthesizer (hereafter referred to as the PLL) used in the M32C/80 series microcomputers and the effects of PLL jitters on CAN communication.

Target Device

M32C/81, 83,84,85,86 groups

Contents

1. Phase timing of the PLL frequency synthesizer

The PLL in the M32C/80 series has its phases corrected every reference clock cycle. Therefore, in no case will PLL jitters accumulate along with the passage of time.

Figure 1 shows a block diagram of the PLL. Figure 2 shows an example timing with which the PLL in the M32C/80 series is corrected for phases. In the example in Figure 2, the reference clock is derived from XIN by dividing it by 2, and the programmable counter is set to divide-by-16, so that XIN is multiplied by 4.

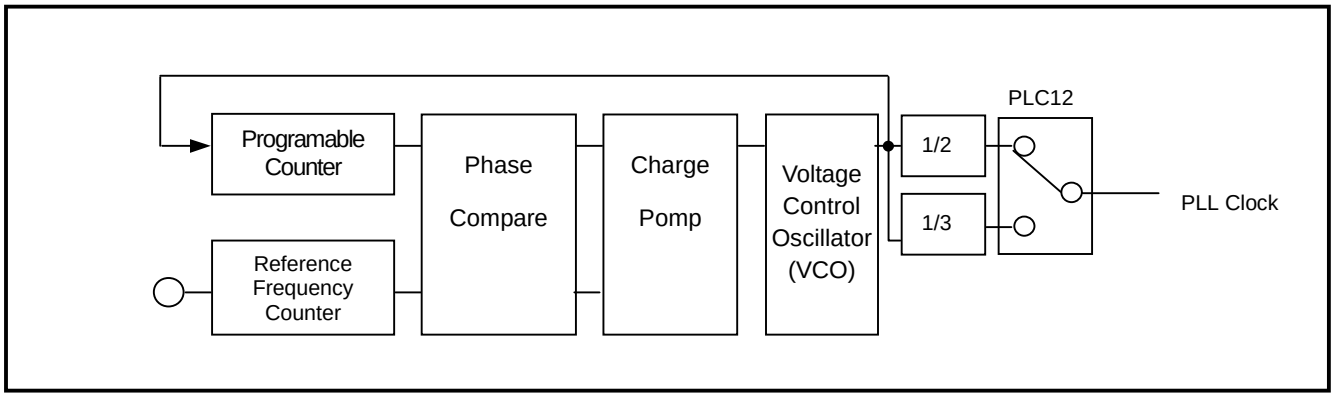
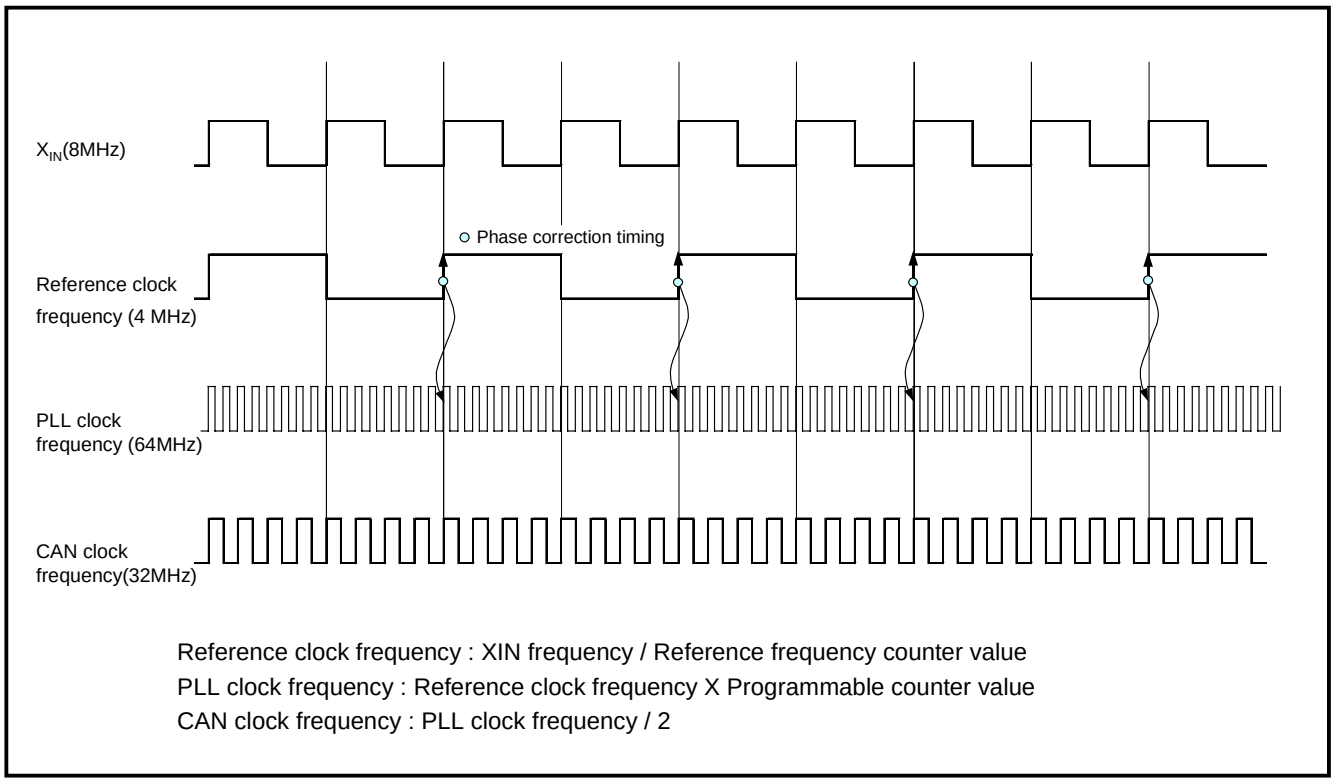


Figure 1 PLL block diagram



Reference clock frequency : XIN frequency / Reference frequency counter value
PLL clock frequency : Reference clock frequency X Programmable counter value
CAN clock frequency : PLL clock frequency / 2

Figure 2 Phase correction timing

2. Effects of PLL jitters on CAN communication

A worst-case situation where CAN communication is most affected by an out-of-sync condition (i.e., the longest possible period for which communication will not be resynchronized) occurs when 5 consecutive dominant bits are followed by 5 consecutive recessive bits. If the falling edge of XIN occurs within the resynchronization width (Resynchronization Jump Width, hereafter referred to as SJW), CAN communication will not be affected.

Figure 3 shows how CAN communication is resynchronized when 5 consecutive dominant bits are followed by 5 consecutive recessive bits and the timing with which the PLL is corrected for phases.

Because the PLL in the M32C/80 series has its phases corrected every reference clock cycle, PLL jitters do not accumulate along with the passage of time.

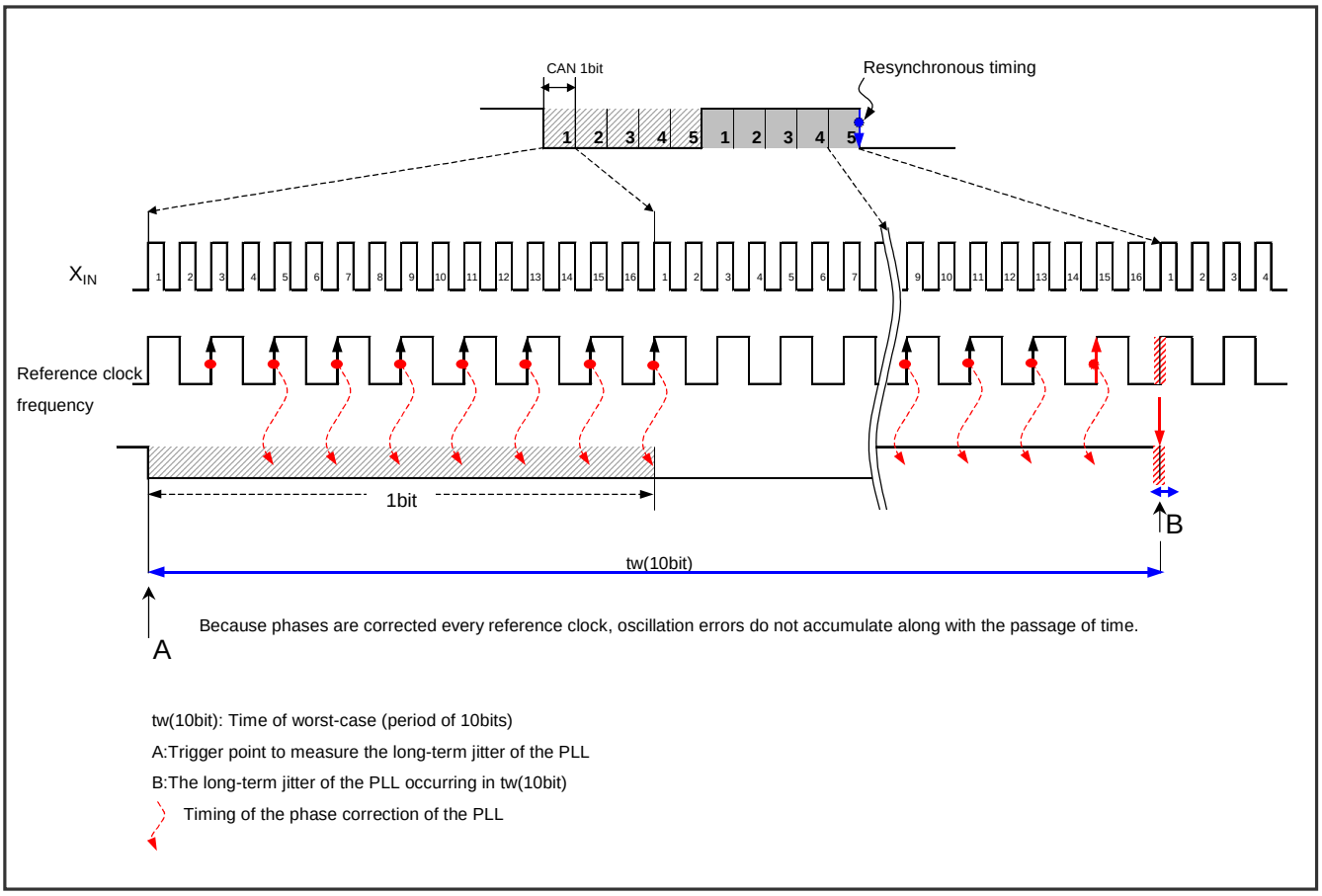


Figure 3 Relation of resynchronization on CAN communication and PLL phase correction

Next, we measured the long-term jitter of the PLL by using the M32C/80 series microcomputer to calculate an out-of-sync time due to clock errors that include the long-term jitter of the PLL.

When measuring the long-term jitter, we aimed to obtain the maximum value (worst value) of the long-term jitter by changing samples and measurement conditions before making a measurement. Then, by adding errors inherent in the measurement equipment and jitter fluctuations due to measurement time to the maximum value (worst value) of the measured data, we calculated the long-term jitter in tw(10bit). As a result, it was found that the long-term jitter of the PLL occurring in tw(10bit) was 25 ns.

Based on this measurement result, we calculated the maximum value (worst value) of an out-of-sync time occurring in tw(10bit). In CAN communication performed at a baud rate of 500 kbps, it was found to be 85 ns. The calculation method is shown below. Because this maximum value (worst value) is smaller than SJW (1 Tq) = 125 ns, it can safely be said that the long-term jitter of the PLL does not affect CAN communication.

[Calculation method]

(1) Conditions
- XIN = 8 MHz
- PLL clock frequency = 64 MHz
- CAN clock frequency = 32 MHz
- CAN baud rate = 500 kbps (1 Tq = 125 ns)
- SJW = 1 Tq
- ΔfXIN: XIN clock error = 0.3%
- ΔTPLL: long-term jitter of PLL occurring in tw(10bit) = 25 ns

(2) Equation to calculate an out-of-sync time (ΔT) that occurs in tw(10bit) due to clock errors including PLL jitter

ΔT = out-of-sync time occurring in tw(10bit) due to XIN clock errors [ns] + long-term jitter of PLL occurring in tw(10bit) [ns]

$|\Delta T| \leq 10\text{bit} \times (\text{Nominal Time}) \times \Delta fXIN \div 100 + \Delta TPLL$

[Calculation result]

$|\Delta T| \leq 10\text{bit} \times 2000[\text{ns}] \times 0.3[\%] \div 100 + 25[\text{ns}] = 85[\text{ns}]$

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Nov.01.03	—	First edition issued

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