



# AK8817

## NTSC/PAL Digital Video Encoder

### General Description

The AK8817 is a Digital Video Encoder for Portable and Mobile application. ITU-R BT.601 level compatible Y, Cb, and Cr signals which correspond to 27MHz or square pixel are encoded into either NTSC or PAL compatible composite video signal. Interface is made in HSYNC-, VSYNC- synchronized slave-mode operation or ITU-R.Bt656. AK8817 has 75ohm driver with LPF.

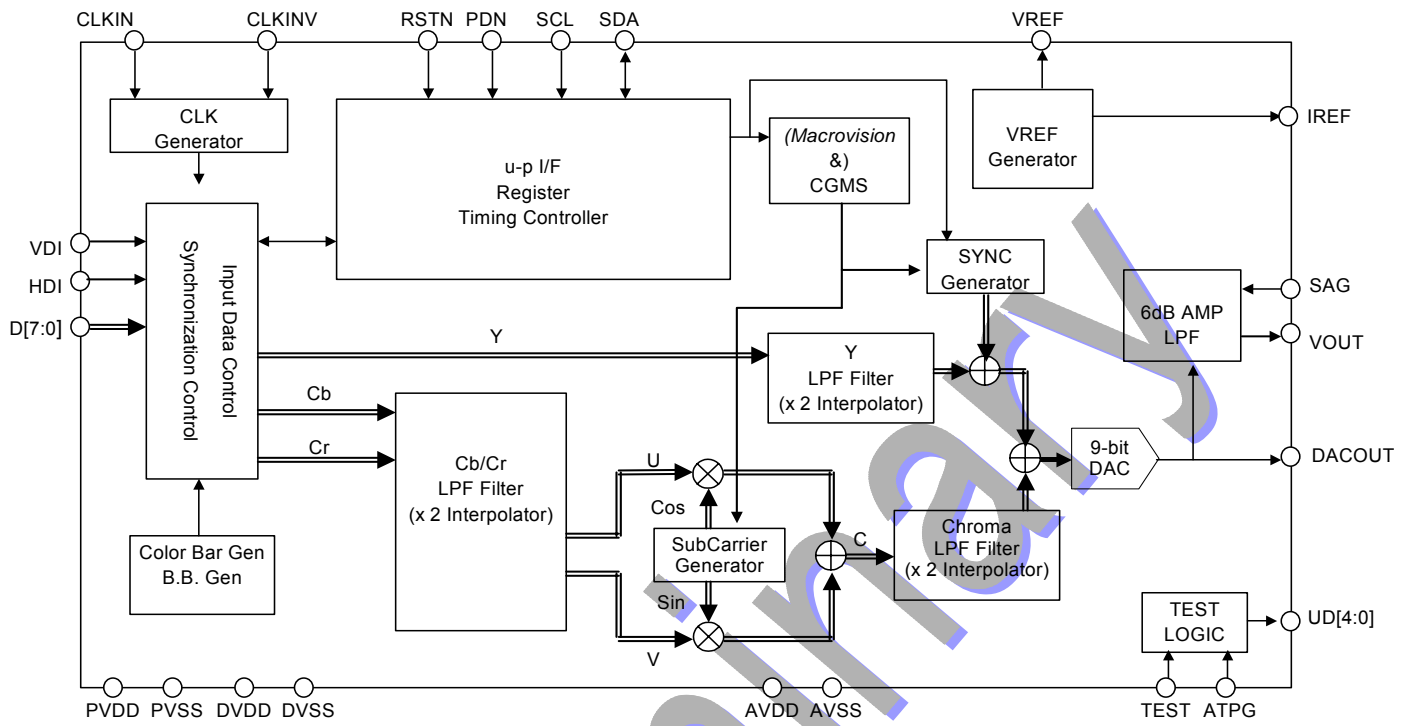
It is possible to encode the VBID(CGMS-A) and WSS signal on the output video signal.

Host Control interface is I2C Bus I/F.

### Features

- NTSC-M, PAL-B, D, G, H, I Composite Video encoding
- Y:Cb:Cr 4:2:2
- H/V Slave Operation / ITU-R.BT656 Interface
- Y filtering: 2 x over-sampling
- C filtering: 4 x over-sampling
- 9bit DAC
- Setup
- VBID ( CGMS-A ) Compatible
- WSS Compatible
- Operation Clock rate : 27MHz or Square-pixel Clock rate(NTSC:24.5454MHz/PAL29.50MHz)
- Video Amp with LPF
- On-chip Color Bar Output
- Black Burst Output
- Power Supply (AVDD, DVDD) 2.7V - 3.3V
- I/F Power Supply (PVDD) 1.6V - 3.3V
- Power Down mode
- Monolithic CMOS
- 41pin FBGA(4mm x 4mm) (Pb Free)

**Block Diagram**

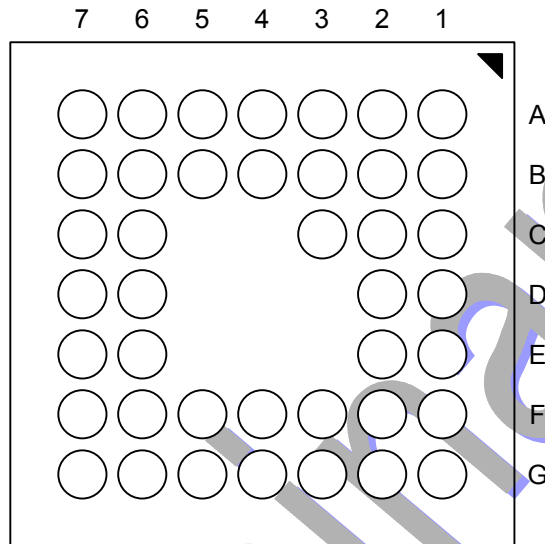


Preliminary

**Ordering Guide**

AK8817VG 41pin FBGA

**Pin Assignment**



Bottom View

|   | 1      | 2      | 3     | 4    | 5    | 6    | 7    |
|---|--------|--------|-------|------|------|------|------|
| A | NC     | DACOUT | SAG   | VOUT | DVDD | RSTN | NC   |
| B | AVDD   | AVSS   | BVSS  | DVSS | PDN  | SCL  | ATPG |
| C | VREF   | IREF   | INDEX |      |      | HDI  | SDA  |
| D | UD3    | UD4    |       |      |      | PVSS | VDI  |
| E | UD1    | UD2    |       |      |      | D0   | PVDD |
| F | CLKINV | UD0    | DVSS  | D7   | D5   | D3   | D1   |
| G | NC     | CLKIN  | DVDD  | D6   | D4   | D2   | TEST |

TOP View

|                                   |
|-----------------------------------|
| <b>Pin Functional Description</b> |
|-----------------------------------|

| Pin#   | Pin Name | I/O | Functional Outline  |
|--------|----------|-----|---|
| G2     | CLKIN    | I   | Clock input pin.<br>Input a clock which is synchronized with data.<br>When to input 601 data : 27 MHz.<br>When to input square pixel data : 24.5454 MHz ( NTSC ) / 29.50 MHz ( PAL )                                      |
| F1     | CLKINV   | I   | Internal clock is inverted (internal operation timing edge is inverted.)<br>Connect to either DVDD or DGND.   |
| B5     | PDN      | I   | Power Down Pin. After returning from PD mode to normal operation, RESET Sequence should be done to AK8817.<br>"L " (GND level): Power-down<br>"H " : normal operation   |
| A6     | RSTN     | I   | Reset input pin. In order to initialize the device , an initialization must be made in accordance with the reset sequence.<br>"L " : reset<br>"H " : normal operation<br>Hi-Z input is acceptable to this pin at PDN = L. |
| C7     | SDA      | I   | I2C data pin.<br>This pin is pulled-up to PVDD.<br>Hi-Z input is possible when PDN is at low.<br>SDA input is not accepted during the reset sequence operation.   |
| B6     | SCL      | I   | I2C clock input pin<br>An input level of lower-than-PVDD should be input.<br>Hi-Z input is possible when PDN is at low.<br>SCL input is not accepted during the reset sequence operation.                                 |
| F4     | D7       | I   | Data Video Signal input pin (MSB).<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| G4     | D6       | I   | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| F5     | D5       | I   | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| G5     | D4       | I   | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| F6     | D3       | I   | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| G6     | D2       | I   | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| F7     | D1       | I   | Data Video Signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| E6     | D0       | I   | Data Video Signal input pin (LSB).<br>Hi-Z input is acceptable to this pin at PDN = L.  |
| C6     | HDI      | I   | Horizontal SYNC signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.   |
| D7     | VDI      | I   | Vertical SYNC signal input pin.<br>Hi-Z input is acceptable to this pin at PDN = L.   |
| C1     | VREF     | O   | On-chip VREF output pin.<br>AVSS level is output on this pin at PDN = L.<br>Connect this pin to Analog Ground via a 0.1 uF or larger capacitor.   |
| C2     | IREF     | O   | IREF output pin. Connect this pin to Analog ground via a 12k ohm resistor ( better than +/- 1% accuracy ).  |
| A2     | DACOUT   | O   | DAC output pin. Connect this pin to Analog ground via a 390 ohm resistor ( better than +/- 1% accuracy ).   |
| A4     | VOUT     | O   | Video output pin.   |
| A3     | SAG      | O   | SAG Compensation Input pin  |
| B1     | AVDD     | P   | Analog power supply pin.  |
| B2     | AVSS     | G   | Analog ground pin.  |
| A5, G3 | DVDD     | P   | Digital power supply pin (digital core power supply).   |
| B4, F3 | DVSS     | G   | Digital ground pin (digital core ground).   |
| E7     | PVDD     | P   | Power supply pin for chip pad.  |
| D6     | PVSS     | G   | Ground pin for PVDD.  |
| B3     | BVSS     | G   | Substrate ground pin.<br>Connect this pin to Analog ground  |

|            |      |     |   |
|------------|------|-----|---|
| G7         | TEST | I   | For normal operation, connect to ground.          |
| B7         | ATPG | I   | For normal operation, connect to ground.          |
| D2         | UD4  | O   | Test output pin. For normal operation, left open. |
| D1         | UD3  | O   | Test output pin. For normal operation, left open. |
| E2         | UD2  | O   | Test output pin. For normal operation, left open. |
| E1         | UD1  | I/O | Test I/O pin. For normal operation, left open.    |
| F2         | UD0  | I/O | Test I/O pin. For normal operation, left open.    |
| C3         | N.C. | -   | Index pin. For normal operation, left open.       |
| A1, A7, G1 | N.C. | -   | For normal operation, left open.                  |

Analog Output pin status

| MODE / PIN name            | IREF   | VREF   | DACOUT                 | VOUT                        |
|----------------------------|--------|--------|------------------------|-----------------------------|
| PDN = L                    | Hi-Z   | Hi-Z   | Hi-Z                   | Hi-Z                        |
| PDN=H, DAC=L<br>VIDEOAMP=L | Output | Output | Hi-Z<br>DAC Power Down | Hi-Z<br>VIDEOAMP Power Down |
| PDN=H, DAC=H<br>VIDEOAMP=L | Output | Output | Output                 | VIDEOAMP Power Down         |
| PDN=H, DAC=H<br>VIDEOAMP=H | Output | Output | Output                 | Output                      |

Preliminary

|                                   |
|-----------------------------------|
| <b>Electrical Characteristics</b> |
|-----------------------------------|

## (1) Absolute Maximum Ratings

| Parameter                           | Min  | Max       | Units | Note  |
|-------------------------------------|------|-----------|-------|---|
| Supply voltage<br>DVDD, AVDD, PVDD  | -0.3 | 4.5       | V     |   |
| Digital Input pin voltage<br>(VinP) | -0.3 | PVDD +0.3 | V     | D[7:0], HDI, VDI,<br>RSTN, PDN,<br>CLKIN,<br>CLKINV,SCL,<br>SDA |
| Input pin current (Iin)             | -10  | 10        | mA    | Exclude Power<br>supply pin.                                    |
| Storage temperature                 | -40  | 125       | °C    |   |

(Note1)

Power supply voltages are values where each ground pin ( DVSS = AVSS = PVSS ) is at 0 V( voltage reference ).

All power supply ground pins DVSS, AVSS and PVSS should be at same potential.

## (2) Recommended Operating Conditions

| Parameter                      | Min | Typ. | Max  | Units | Conditions  |
|--------------------------------|-----|------|------|-------|-------------|
| Supply voltage *<br>AVDD,DVDD  | 2.7 | 3.0  | 3.3  | V     | AVDD = DVDD |
| Interface power supply<br>PVDD | 1.6 | 1.8  | DVDD | V     |             |
| Operating temperature<br>(Ta)  | -30 |      | 85   | °C    |             |

\* Power supply voltages are values where each ground pin ( PVSS = AVSS = DVSS ) is at 0 V( voltage reference ).

All power supply ground pins DVSS, AVSS and PVSS should be at same potential.

## (3) DC Characteristics

< Operating voltage: DVDD 2.7V~3.3V / PVDD 1.6 V~DVDD, loading condition 15 pF, temperature -30~+85°C >

| Parameter                     | Symbol | Min     | Typ | Max     | Units | Conditions      |
|-------------------------------|--------|---------|-----|---------|-------|-----------------|
| Digital input H voltage (VIH) | VIH    | 0.8PVDD |     |         | V     | PVDD=1.6 - DVDD |
| Digital input L voltage (VIL) | VIL    |         |     | 0.2PVDD | V     | PVDD=1.6 - DVDD |
| Digital input leak current    | IL     |         |     | +/-10   | uA    |                 |
| I2C (SDA) L output            | VOLC   |         |     | 0.4     | V     | IOLC = 3mA      |

( Note )

Digital output pins refer to D[7:0], HDI, VDI, PDN, RSTN, SCL, SDA,CLKIN and CLKINV pin outputs in general term.

(4) Analog Characteristics

< AVDD = 3.0 V, temperature 25 °C >

| Parameter                                | Symbol | Min     | Typ     | Max    | Units                                 |
|--|--------|---------|---------|--------|---------------------------------------|
| DAC resolution                           |        | 9       |         | bit    |                                       |
| DAC integral non-linearity ( error )     |        | +/- 0.6 | +/- 2.0 | LSB    |                                       |
| DAC differential non-linearity ( error ) |        | +/- 0.4 | +/- 1.0 | LSB    |                                       |
| DAC output full scale voltage            | 1.18   | 1.28    | 1.38    | V      | Note1)                                |
| DAC output offset voltage                |        |         | 5.0     | mV     | Note2)                                |
| Video Amp Output Gain                    | 5.0    | 6.0     | 7.0     | dB     | Amp Input Level 1Vpp                  |
| Video Amp Full scale Level               |        | 2.0     |         | Vpp    | Note3)                                |
| Video Amp THD                            | -45    | -51     |         | dB     | 100kHz - 5.5MHz Note4)                |
| Video Amp S/N                            |        | 54      |         | dB     | 100kHz - 5.5MHz Note4)                |
| LPF Ripple                               | -1     | +/- 0.5 | +1      | dB     | 100kHz - 5.5MHz<br>0dB = 100kHz input |
| LPF Stop Band Level                      | 20     | 30      |         | dB     | 27MHz<br>0dB = 100kHz input           |
| LPF Group Delay                          |        | 10      | 100     | ns     | GD3MHz - GD6MHz                       |
| On-chip reference voltage (VREF)         | 1.17   | 1.23    | 1.30    | V      |                                       |
| Reference voltage drift                  |        | -50     |         | ppm/°C |                                       |

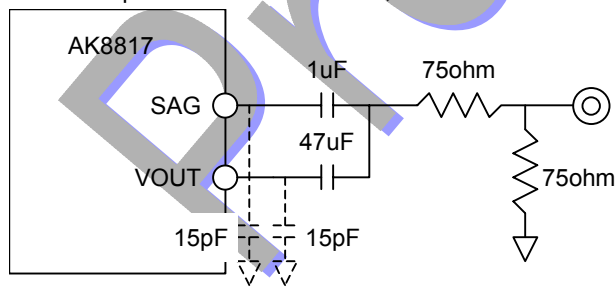
Note1) Values are when a 390 ohm output load, a 12k ohm IREF pin resistor and on-chip VREF are used. Full scale output current is calculated as  $I_{out} = \text{full scale output voltage (typ. 1.28 V)} / 390 \text{ ohm} = \text{typ. 3.28 mA}$ .  
 Note2) A voltage referenced to VSS when a decimal zero voltage is input to DAC.  
 Note3) VOUT Output Level Output Load Resistor: 150ohm, Load Capacitor: 15pF Internal Color Bar output  
 Note4) Output signal from DAC to which Input data corresponded 1Vpp. This signal is input to AMP.  
 Load resistor is 150ohm and Load capacitor is 15pF as shown below figure at (5) Current Consumption.

(5) Current consumption

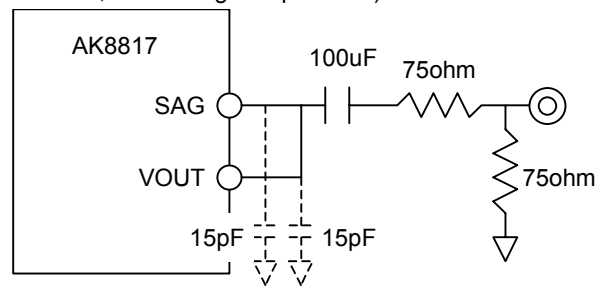
< Operating voltage : DVDD = AVDD = PVDD = 3.0 V, Ta = +25 °C >

| Parameter                        | Symbol | Min | Typ | Max | Units  |
|----------------------------------|--------|-----|-----|-----|--------|
| Total power consumption          |        | 27  | 35  | mA  | Note1) |
| Power-down current 1             |        | 10  | 30  | uA  | Note2) |
| Digital part operating current 1 |        | 13  |     | mA  | Note3) |
| Analog part operating current 1  |        | 14  |     | mA  | Note4) |
| Analog part operating current 2  |        | 5.5 |     | mA  | Note5) |
| Analog part operating current 3  |        | 0.8 |     | mA  | Note6) |

Note1) operation at 27 MHz, NTSC mode on-chip 75% color bar output is enabled and Video Amp output is " on " ( no external output loads are connected , other than those recommended, connecting-components ).



SAG Compensation ON



SAG Compensation OFF

Note2) measuring conditions :

input / output settings after power-down sequence are, PDN pin is at GND level, CLKOUT and SDO output are at high level ( power supply voltage ) with no external connection, input voltage on those input pins is 1/2 level of power supply which are set to accept Hi-Z input at power-down, and TEST = ATPG = GND ( or left open ).

Power supplies are AVDD = DVSS = PVDD.

Each ground pin ( DVSS, AVSS, PVSS ) is always 0 V ( voltage reference ).

Note3) Operation at 27 MHz, NTSC mode on-chip 75% color bar output is enabled.

Note4) DAC ON, Video Amp On SAG Compensation On

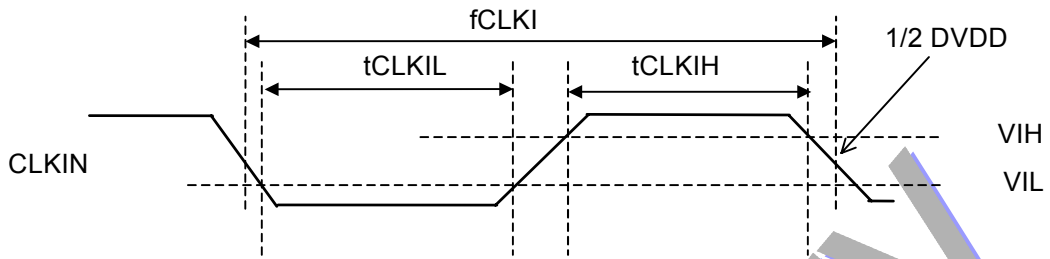
Note5) DAC ON, Video Amp Off (SAG Compensation Off)

Note6) DAC Off, Video Amp Off (SAG Compensation Off)

**AC Timing**

< DVDD 2.7 V ~ 3.3 V / PVDD 1.6 V ~ DVDD, Ta at -30 ~ +85 °C > loading condition : CL = 15 pF

(1) CLK



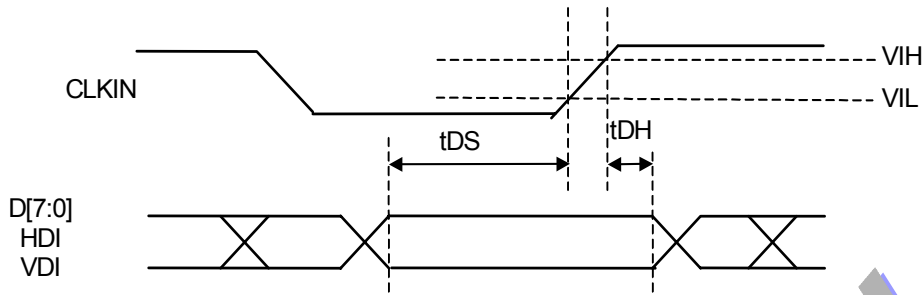
| Parameter      | Symbol | Min. | Typ.    | Max | Unit | Conditions         |
|----------------|--------|------|---------|-----|------|--------------------|
| CLKIN          | fCLKI  |      | 24.5454 |     | MHz  | PIXRT=1<br>NTSC    |
|                |        |      | 27      |     |      | PIXRT=0<br>NTSC/PA |
|                |        |      | 29.50   |     |      | PIXRT=1<br>PAL     |
| CLK duty ratio | pCLKID | 40   |         | 60  | %    |                    |
| CLK Accuracy   |        |      |         | 100 | ppm  |                    |

tCLKIL, tCLKIH : minimum pulse width 12 nS ( tr/tf10%-90%Level Rising/Falling time ≤ 2nS)

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(2) Pixel Data Input Timing



| Parameter       | Symbol | Min. | Typ. | Max | Unit | Conditions   |
|-----------------|--------|------|------|-----|------|--------------|
| Data Setup Time | tDS    | 5    |      |     | nsec | CLKINV = Low |
| Data Hold Time  | tDH    | 8    |      |     | nsec | CLKINV = Low |

When CLKINV = High, similar tDS and tDH are specified at the falling edge of CLKOUT.

(3) HSYNC pulse width

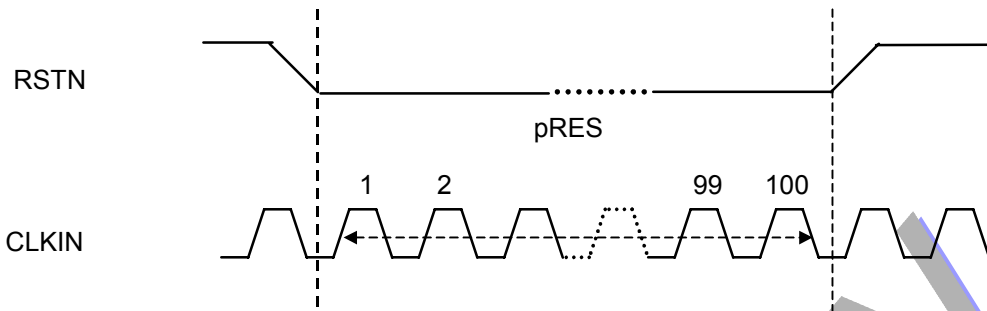


| Parameter       | Symbol | Min. | Typ. | Max | Unit | Conditions           |
|-----------------|--------|------|------|-----|------|----------------------|
| HDI Pulse Width | pHSW   | 15   | 116  |     | CLKs | NTSC<br>(24.5454MHz) |
|                 |        | 15   | 128  |     |      | 27MHz                |
|                 |        | 15   | 139  |     |      | PAL<br>(29.50MHz)    |

\* typical values are calculated by converting the HSYNC pulse width of Analog Video specification into number of system clock pulses.

(4) Reset

(4-1) Reset Timing

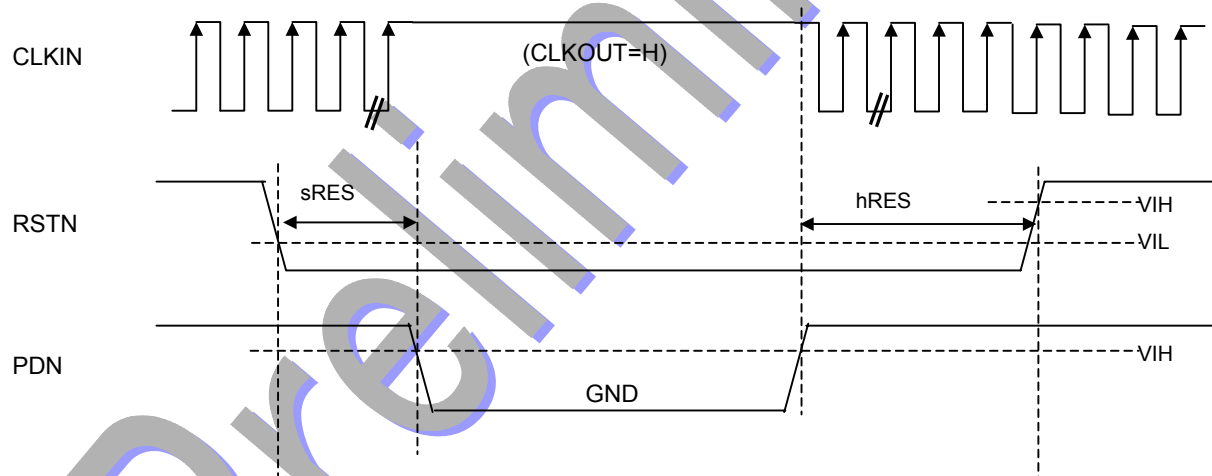


| Parameter        | Symbol | Min. | Typ. | Max | Unit |
|------------------|--------|------|------|-----|------|
| RSTN Pulse Width | pRES   | 100  |      |     | CLKs |

(4-2) Power Down Sequence / Reset Sequence

Before PDN setting ( PDN to low ), Reset must be enabled for a duration of longer-than-100 clock time.

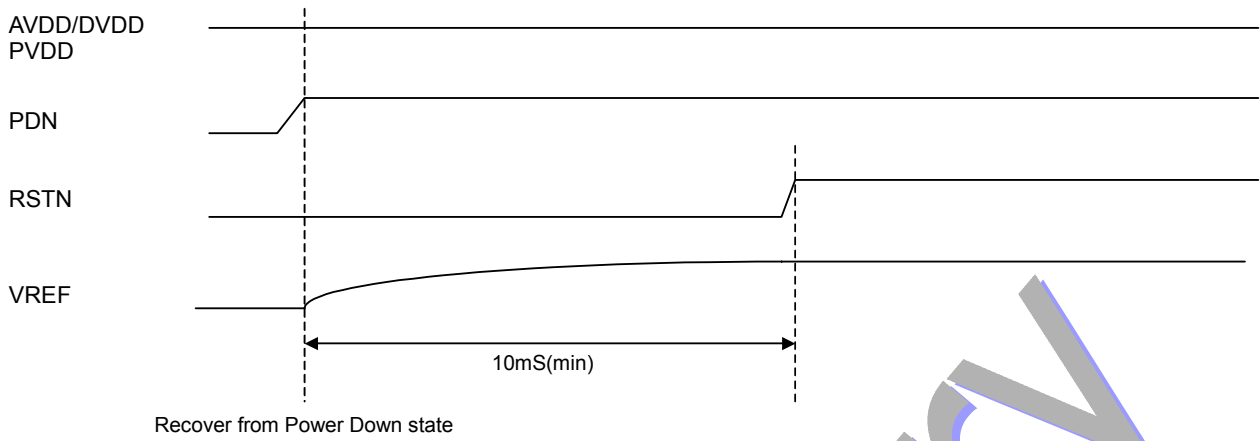
After PDN release ( PDN to high ), Reset must be enabled for 10 mS or longer till analog part reference voltage & current are stabilized.



| Parameter                             | Symbol | Min. | Typ. | Max | Unit |
|---------------------------------------|--------|------|------|-----|------|
| RSTN Pulse Width                      | sRES   | 100  |      |     | CLKs |
| Time from PDN to high to RSTN to high | hRES   | 10   |      |     | msec |
| SCL low duration before RSTN to rise  | tSCLL  | 50   |      |     | nsec |

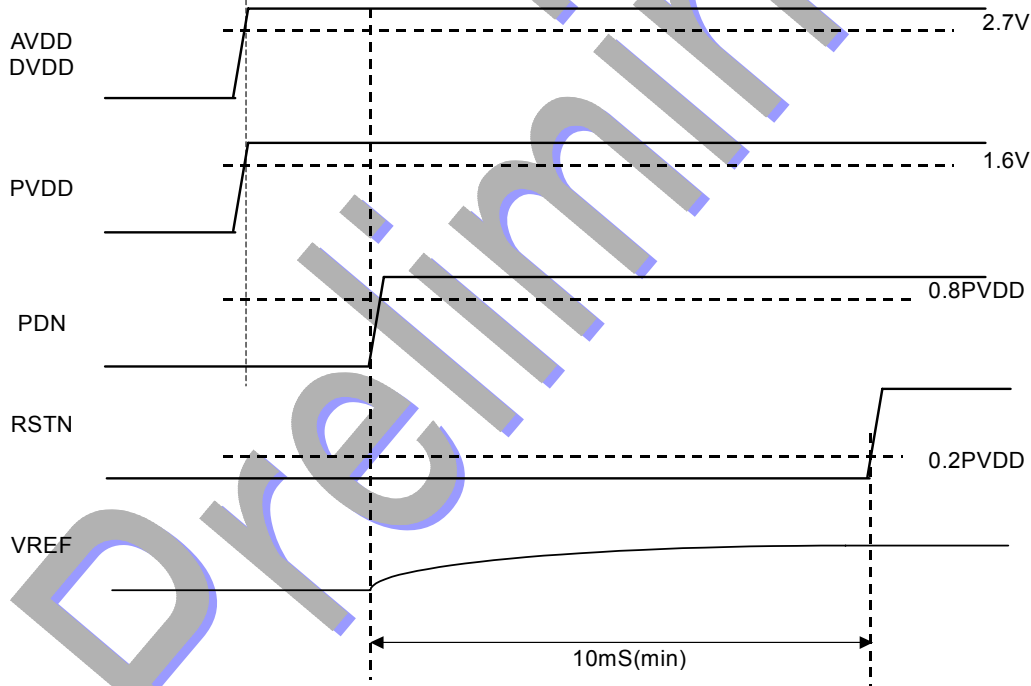
At power-down, all control signals must be surely connected to either the selected power supply or ground level, and not to VIH / VIL levels.

(4-3) Power Down Sequence/Power up sequence



(4-4) Power On Reset

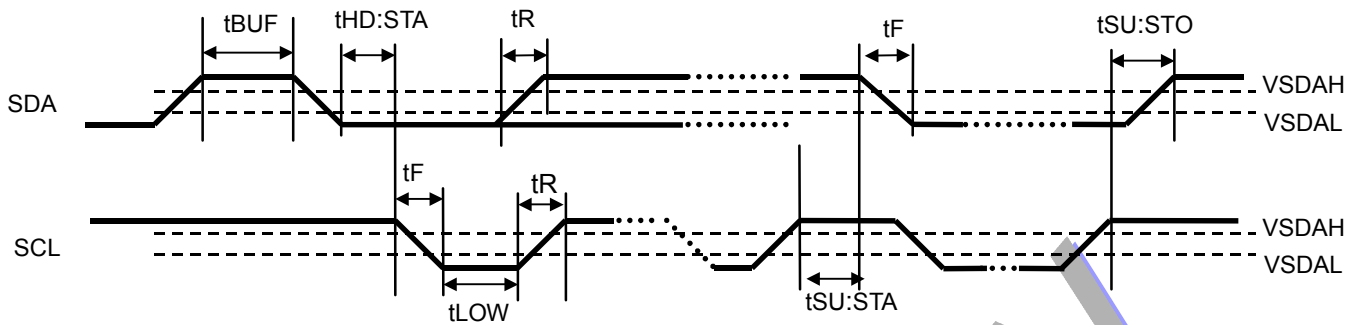
After Power up, It is necessary to make reset sequence until Analog Reference voltage(VREF) becomes stable. PVDD/DVDD/AVDD should be power up at same time or 1st PVDD power up and AVDD/DVDD makes up.



| item               | Symbol   | Min | Typ | Max | Unit | Note |
|--------------------|----------|-----|-----|-----|------|------|
| RESETN Pulse width | pRES_PON | 10  |     |     | msec |      |

Remark: Reset sequence requires clock input.

(5) I2C Bus Input/Output Timing < Ta = -30 ~ +85 °C >

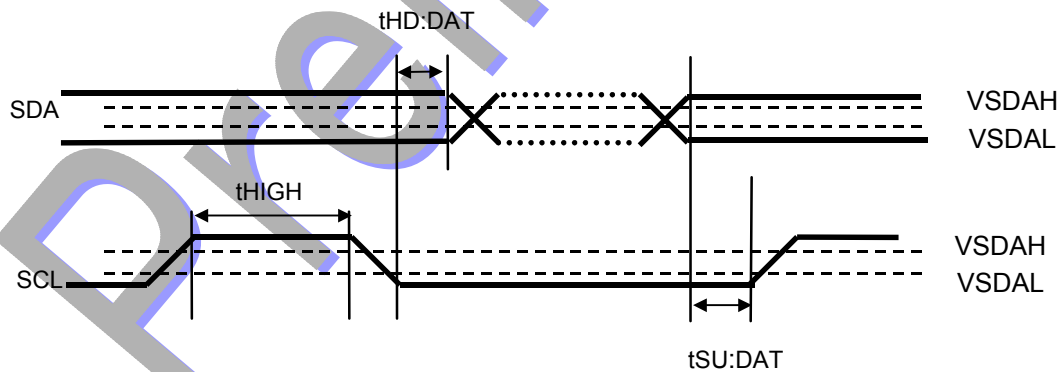


(5-1) Timing 1  
 VSDAH: 0.8PVDD  
 VSDAL : 0.2PVDD

| Parameter                   | Symbol       | Min. | Max. | Unit |
|-----------------------------|--------------|------|------|------|
| Bus Free Time               | $t_{BUF}$    | 1.3  |      | usec |
| Hold Time (Start Condition) | $t_{HD:STA}$ | 0.6  |      | usec |
| Clock Pulse Low Time        | $t_{LOW}$    | 1.3  |      | usec |
| Input Signal Rise Time      | $t_R$        |      | 300  | nsec |
| Input Signal Fall Time      | $t_F$        |      | 300  | nsec |
| Setup Time(Start Condition) | $t_{SU:STA}$ | 0.6  |      | usec |
| Setup Time(Stop Condition)  | $t_{SU:STO}$ | 0.6  |      | usec |

The above I2C bus related timing is specified by the I2C Bus Specification, and it is not limited by the device performance. For details, please refer to the I2C Bus Specification.

(5-2) Timing 2



VSDAH: 0.8PVDD  
 VSDAL : 0.2PVDD

| Parameter             | Symbol       | Min.        | Max.        | Unit |
|-----------------------|--------------|-------------|-------------|------|
| Data Setup Time       | $t_{SU:DAT}$ | 100 (note1) |             | nsec |
| Data Hold Time        | $t_{HD:DAT}$ | 0.0         | 0.9 (note2) | usec |
| Clock Pulse High Time | $t_{HIGH}$   | 0.6         |             | usec |

note 1 : when to use I2C Bus Standard mode,  $t_{SU:DAT} > 250$  ns must be met.

note 2 : when the AK8817 is used in such bus interface where  $t_{LOW}$  is not extended ( at minimum specification of  $t_{LOW}$  ), this condition must be met.

**Device Control Interface**

The AK8817 is controlled via I2C Bus Control Interface.

**[ I2C SLAVE Address ]**

2C Slave Address is **0x40**

**[ I2C Control Sequence ]**

(1) Write Sequence

When the Slave Address of the AK8817 Write mode is received at the first byte, Sub Address at the second byte and Data at the third and succeeding bytes are received.

There are 2 operations in Write Sequence - a sequence to write at every single byte, and a sequential write operation to write multiple bytes successively.

(a) 1 Byte Write Sequence

|   |               |   |      |             |      |        |      |     |
|---|---------------|---|------|-------------|------|--------|------|-----|
| S | Slave Address | w | A    | Sub Address | A    | Data   | A    | Stp |
|   | 8-bits        |   | 1bit | 8-bits      | 1bit | 8-bits | 1bit |     |

(b) Multiple Bytes ( m-bytes ) Write Sequence ( Sequential Write Operation )

|   |               |   |      |                 |      |         |      |           |      |     |           |      |     |
|---|---------------|---|------|-----------------|------|---------|------|-----------|------|-----|-----------|------|-----|
| S | Slave Address | w | A    | Sub Address (n) | A    | Data(n) | A    | Data(n+1) | A    | ... | Data(n+m) | A    | stp |
|   | 8-bits        |   | 1bit | 8-bits          | 1bit | 8-bits  | 1bit | 8-bits    | 1bit |     | 8-bits    | 1bit |     |

(2) Read Sequence

When the Slave Address of the AK8817 Read mode is received, Data at the second and succeeding bytes are transmitted.

|   |               |   |   |                 |   |    |               |   |   |        |   |        |   |        |   |     |        |   |     |
|---|---------------|---|---|-----------------|---|----|---------------|---|---|--------|---|--------|---|--------|---|-----|--------|---|-----|
| S | Slave Address | r | A | Sub Address (n) | A | rS | Slave Address | F | A | Data1  | A | Data2  | A | Data3  | A | ... | Data n | A | stp |
|   | 8-bits        |   | 1 | 8-bits          | 1 |    | 8-bits        |   | 1 | 8-bits | 1 | 8-bits | 1 | 8-bits | 1 |     | 8-bits | 1 |     |

Abbreviated terms listed above mean :

- S, rS : Start Condition
- A : Acknowledge ( SDA Low )
- A- : Not Acknowledge ( SDA High )
- stp : Stop Condition
- R/W 1 : Read 0 : Write

- : to be controlled by the Master Device. Micro-computer interface is output normally .
- : to be controlled by the Slave Device. To be output by the AK8817.

## Video Encoder Functional Outline

### (1) Reset

#### (1-1) Reset of Serial Interface part ( asynchronous reset )

Reset is made by setting RSTN pin to low.

#### (1-2) Reset of other than Serial Interface blocks

Reset is made by keeping RSTN pin low for a longer than 100 clock time, in normal operation.

#### (1-3) at Power-On-Reset ( including power-down release case )

Follow the power-on-reset sequence.

At the completion of each initialization, all internal registers are set to default values ( refer to Register Map ). Right after the reset, Video output of the AK8817 is put into Hi-Z condition.

### (2) Power-Down

It is possible to put the device into power-down mode by setting the AK8817 power-down pin to GND.

Transition to power-down mode should be followed by the power-down sequence. As for the recover from the power-down mode, it should be followed by the power-down release sequence.

### (3) Master Clock

A following clock should be input as a Master clock.

In Encoder Mode operation ( a synchronized clock with input data is required )

|              | When ITU-R BT.601 data is input<br>( PIXRT-bit = 0 ) | When Square Pixel data is input<br>( PIXRT-bit = 1 ) |
|--------------|--|--|
| NTSC Encoder | 27MHz  | 24.5454MHz   |
| PAL Encoder  | 27MHz  | 29.50MHz   |

### (4) Video Signal Interface

Video input signal ( data ) should be synchronized in either of the following methods :

- \* Slave mode operation where synchronization is made with HSYNC ( HDI ) / VSYNC ( VDI ).
- \* ITU-R BT. 656 I / F ( EAV decode ) (only 27MHz operation)

### (5) Pixel Data

Input data to the AK8817 is YCbCr ( 4:2:2 ).

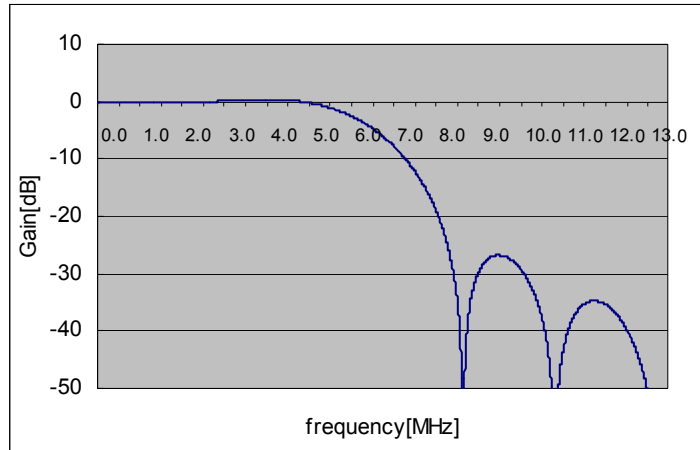
Data with Y : 16 ~ 235 and CbCr : 16 ~ 240 should be input.

### (6) Video Signal Conversion

Video Re-Composition module converts the multiplexed data ( ITU-R BT.601 Level Y, Cb, Cr ) into interlaced NTSC-M and PAL-B, D, G, H, I data. Video encoding setting is done by "Control 1 Register ".

(7) Luminance Signal Filter ( Luma Filter )

Luminance signal is output via LPF ( see x2 Luma Filter in the block diagram ).



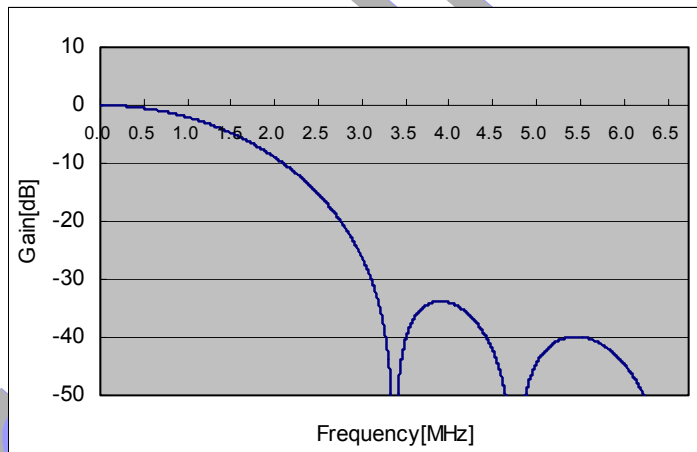
(8) Chroma Signal Filter ( Chroma Filter )

Chroma input signal components ( Cb, Cr ) prior to the modulation go through a 1.3 MHz Band Limiting Filter ( see 4:2:2 to 4:4:4 x2 interpolator in the block diagram ).

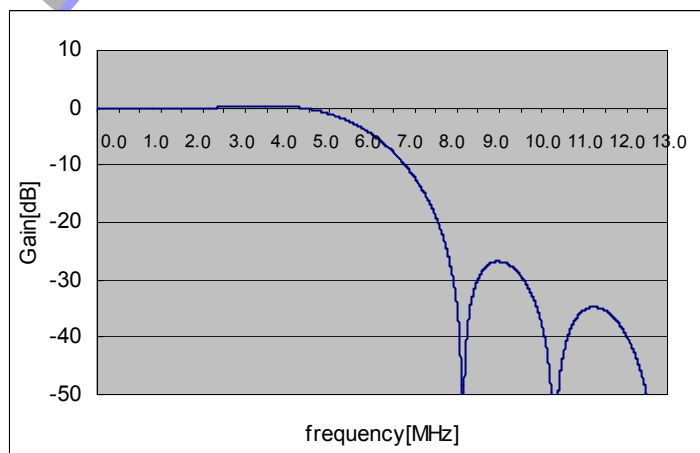
Chroma signal which is modulated by the sub-carrier is output via a low pass filter ( Chroma LPF in the block diagram ).

Frequency response of each filter is shown below.

4:2:2 to 4:4:4 Interpolator Filter



x 2 Interpolator Filter



## (9) Color Burst Signal

Burst signal is generated by a 32 bit digital frequency synthesizer.  
Color Burst Frequency is selected by mode setting of NTSC / PAL.

| Standard      | Subcarrier Freq (MHz) | Video Process 1 VMOD-bit |
|---------------|-----------------------|--------------------------|
| NTSC-M        | 3.57954545            | 0                        |
| PAL-B,D,G,H,I | 4.43361875            | 1                        |

Burst Signal Table

## (10) Sub - Carrier Reset

A function to reset sub-carrier by Color Frame sequence.  
Reset function can be turned "OFF " by setting SCR-bit of Control 1 Register.  
Default value is set to enable Sub-carrier reset.

| SCR  | 0   | 1                             |
|------|---|-------------------------------|
| NTSC | Sub-carrier phase is reset in every 2 Frames ( 4 Fields ) | Sub-carrier reset is not done |
| PAL  | Sub-carrier phase is reset in every 4 Frames ( 8 Fields ) | Sub-carrier reset is not done |

## (11) Setup processing

Setup processing can be performed on Video signal by Control 2 Register Setup-bit.  
Following processing is made on Luminance signal ( Y signal ) and Chroma signal ( C signal ) by the Setup processing.

$Y \text{ Setup} = Y \times 0.925 + 7.5 \text{ IRE}$  where Y setup is the Luminance signal after Setup processing.

$C \text{ Setup} = C \times 0.925$  where C Setup is the Chroma signal after Setup processing.

## (12) Video DAC

The AK8817 has a 9 Bit resolution, current-drive DAC as a video DAC which runs at 29.5 / 24.5454 MHz or 27.00MHz clock frequency.

This DAC is designed to output 1.28 V o-p at full scale under the following conditions loading resistance of 390 ohms, VREF at 1.23 V and IREF pin resistor of 12k ohms.

[ VREF ] pin should be connected to ground via a 0.1 uF or larger capacitor.

DAC output can be turned "ON" or "OFF" by register setting and current consumption can be lowered.

When the output is turned off, it is put into high impedance condition.

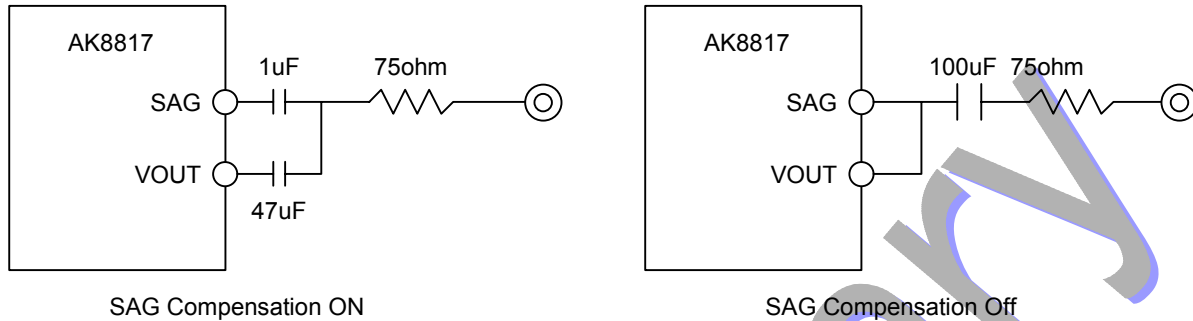


(13) Video Amp

AK8817 has Video amp that can drive 150ohm with Low pass filter. It can also possible to compensate SAG distortion. To compensate SAG external capacitor is 47uF and 1uF as shown following figure. Recommendation voltage when SAG compensation circuit is used is 3V or more.

VOUT pin and SAG pin should be shorten when SAG Compensation is not used. Output pin should make AC coupling. SAG Compensation circuit can be set on or off with setting register.

In case of not using internal Video amp (Only DAC use case), Video Amp becomes power down. In this case SAG and VOUT should be Open.



| VAMPMD[1:0] | Operation                            | Conditions   |
|-------------|--------------------------------------|--|
| 00          | Video Amp OFF + SAG Compensation OFF | Only DAC output                                    |
| 01          | Video AMP ON + SAG Compensation ON   | Recommendation Voltage of DVDD/AVDD is 3v or more. |
| 10          | Video Amp ON + No SAG Compensation   | SAG pin and VOUT should be shorten.                |
| 11          | Reserved                             |  |

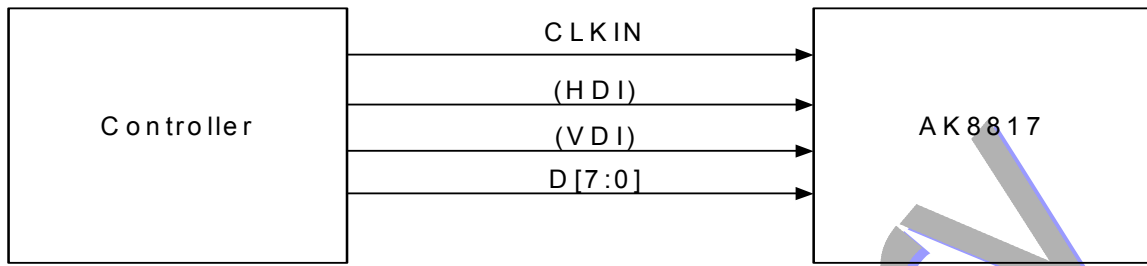
(14) Video Data Interface Timing

Data is captured by a clock which is fed on CLKIN pin.

The Video Encoder receives a clock from a controller ( refer to the following diagram ).

In Slave mode operation, Synchronization is made with HDI / VDI.

In ITU-R BT.656 mode operation, HDI / VDI are not required.



Preliminary

(14-2) Video Interface mode

The AK8817 synchronizes with input signal by the following, 2 interface modes.

- (a) Slave-mode interface where synchronization is made with externally-fed synchronization signals HDI / VDI (HDI / VDI interface)
- (b) ITU-R BT.656 Interface mode ( 656 interface )

interface mode setting is controlled by [REC656]-bit of Control 2 Register.

| REC656-bit | Operation                   |
|------------|-----------------------------|
| 0          | HDI / VDI Slave mode        |
| 1          | ITU-R BT.656 Interface mode |

(a-1) Timing signal ( HDI / VDI ) VS Data input relation

Horizontal Synchronization ( in-line Pixel Sync ) is made with HDI synchronization timing signal.

Vertical Synchronization ( in-line Frame Line Sync ) is made with VDI synchronization timing signal.

Recognition of Video Field ( Odd Field or Even Field ) is made by VDI input signal which is referenced with HDI.

In normal operation, the AK8817 checks changes of HDI and VDI at the clock edge ( CLK synchronization ) which becomes a data capture reference position.

At a pixel position where HDI is judged to become " Low ", it is recognized as 0<sub>H</sub> (zero th position ).

Cb0 data position depends on input data rate ( ITU-R BT.601 or Square Pixel data ).

Cb0 Data

|              | At ITU-R BT.601 Data input | At Square Pixel data input |
|--------------|----------------------------|----------------------------|
| NTSC Encoder | 244 <sup>th</sup> data     | 236 <sup>th</sup> data     |
| PAL Encoder  | 264 <sup>th</sup> data     | 310 <sup>th</sup> data     |

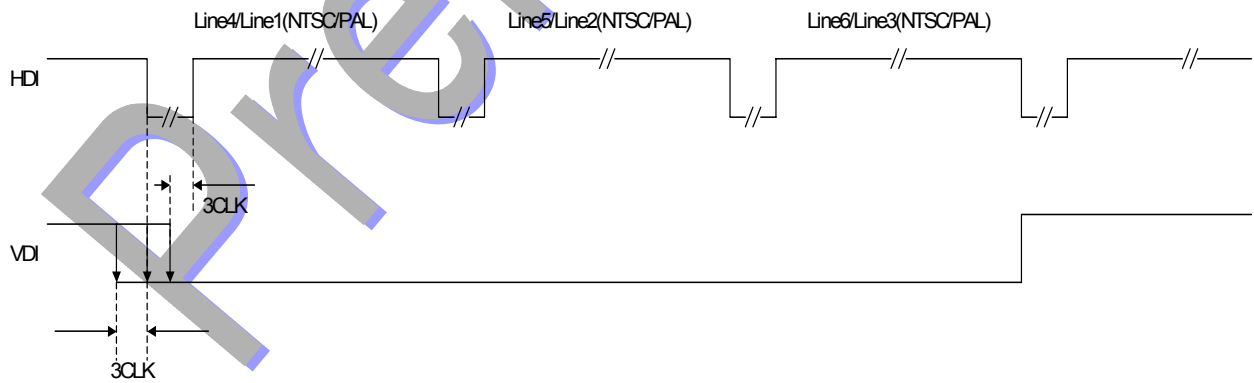
Video Field is recognized by the VDI relation with HDI.

Field recognition is made as follows :

The AK8817 distinguishes at every Field if it is Odd Field ( 1<sup>st</sup> Field ) or not. Even Field Sync signal is not usually input.

1 ) Recognition timing of Odd Field is decided by those timing signal relations which are fed on HDI and VDI pins.

When the VDI falling pulse is input on VDI input pin during the time from 3 clocks prior to the falling edge of HDI timing pulse which is fed on HDI input till 3 clocks prior to the rising edge of HDI timing pulse, the Line is recognized to be Line 4.



2 ) Whenever Horizontal / Vertical SYNC signal inputs are not fed as expected in the Video Specifications, in term of timing and # of pulses ( kept at " High " level ), the AK8817 continues to self-run the operation which is based on the Sync signals, fed just before.

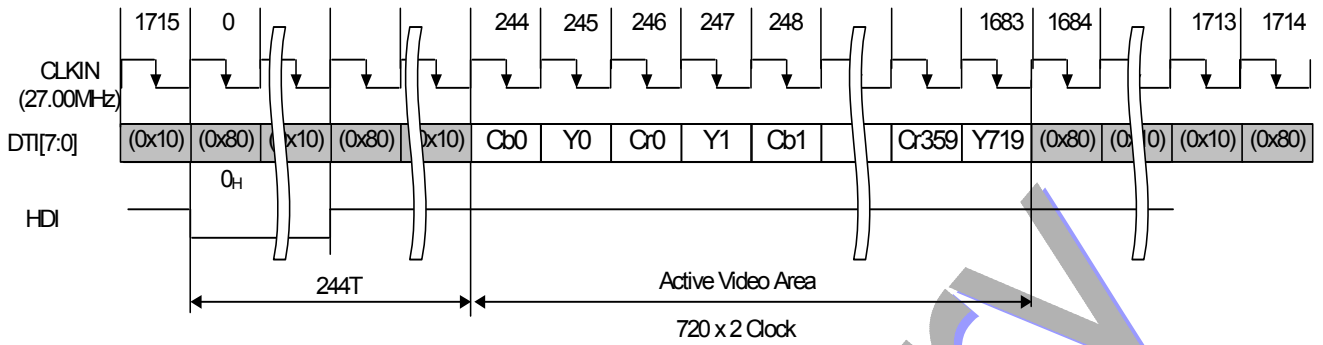
But it is recommended to feed Sync signals as specified every time in order to prevent erroneous operation.

3 ) VD pulse input at other than Odd Field synchronization is ignored ( Synchronization is made with Odd Field only ).

(a-2) Horizontal Synchronization ( Pixel Data synchronization within a Line )

(a-2-1) at ITU-R BT. 601 data input case

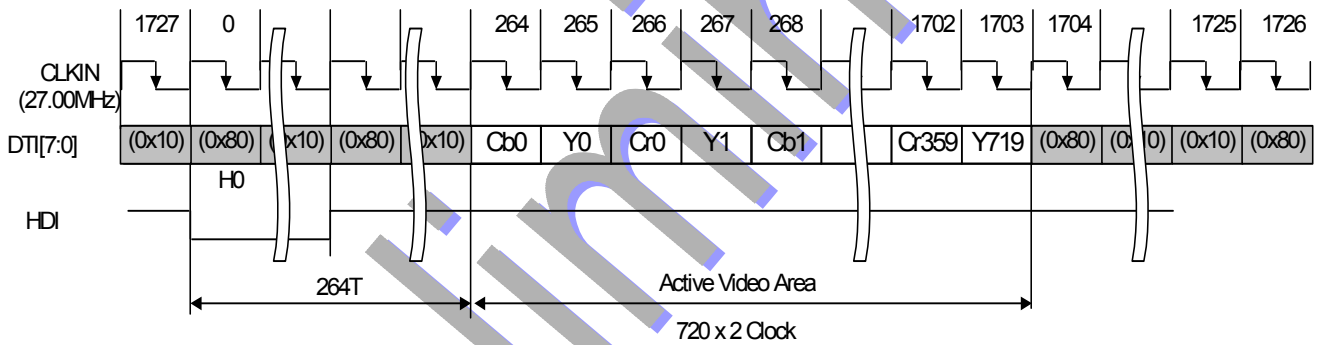
(a-2-1-1) NTSC



\*) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817 takes input data at the falling edge of each CLKIN if CLKEDGE-bit = 1.(CLKINV = 1.)

\*) as an input data other than during active video period, Black level ( C / Y = 0x80 / 0x10 ) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

(a-2-1-2) PAL

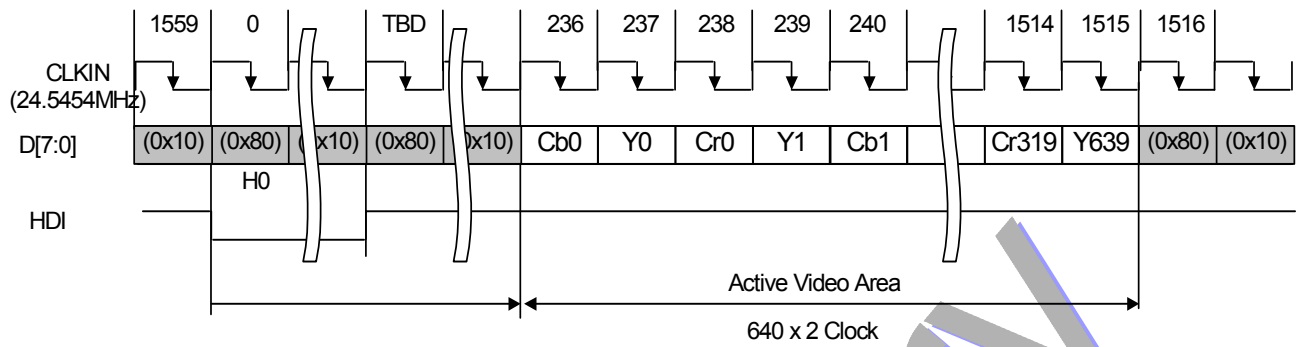


\*) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817 takes input data at the falling edge of each CLKIN if CLKEDGE-bit = 1. ( CLKINV = 1.)

\*) as an input data other than during active video period, Black level ( C / Y = 0x80 / 0x10 ) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

(a-2-2) at Square Pixel Rate input case

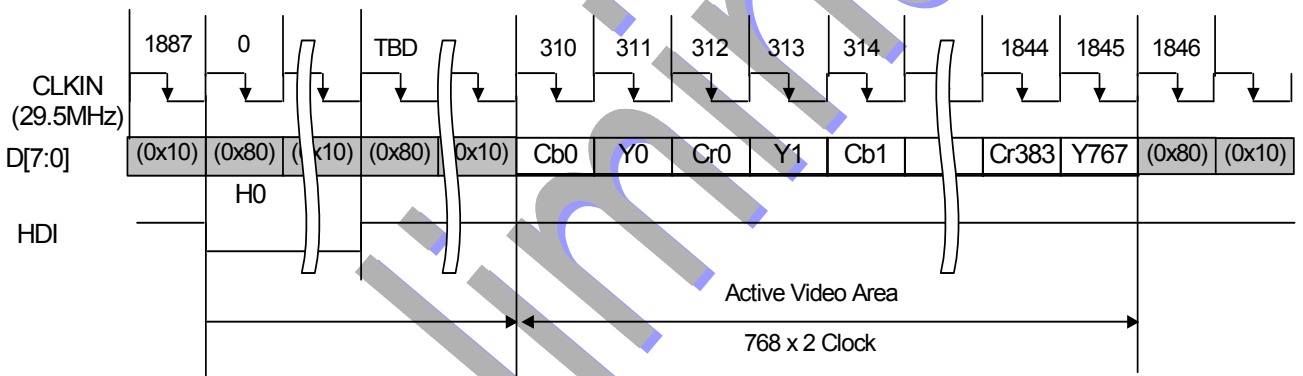
(a-2-2-1) NTSC



\* ) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817 takes input data at the falling edge of each CLKIN if CLKINV = 1.

\* ) as an input data other than during active video period, Black level ( C / Y = 0x80 / 0x10 ) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

(a-2-2-2) PAL



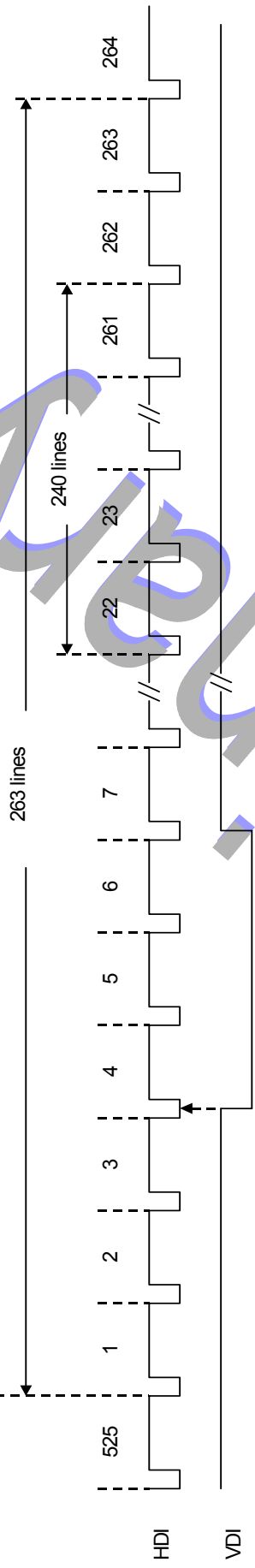
\* ) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817 takes input data at the falling edge of each CLKIN if CLKINV-bit = 1. (CLKINV = 1.)

\* ) as an input data other than during active video period, Black level ( C / Y = 0x80 / 0x10 ) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

( a-3 ) HDI and VDI relation in each Frame

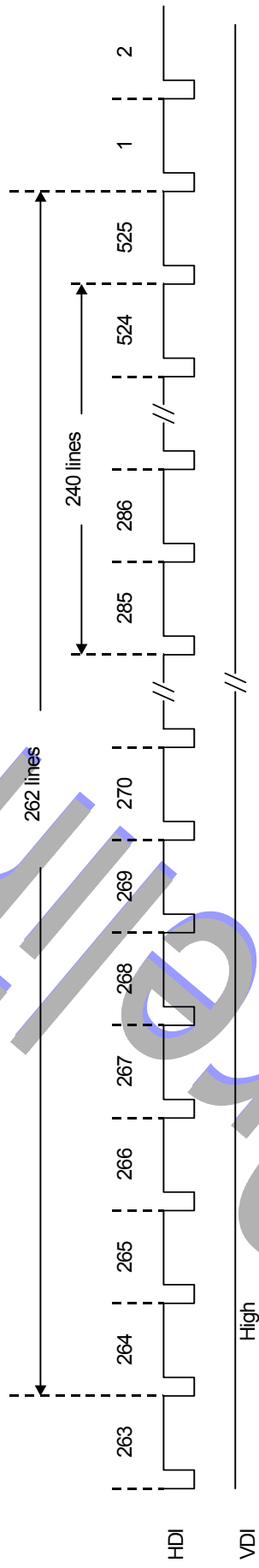
( a-3-1 ) NTSC ( Frame ) 525 Line 480 active lines

The First Field ( ODD )



\* ) VDI negative-going should be fed during the time from 3 clocks prior to negative-going of HDI at L4 till 3 clocks prior to positive-going of HDI. VDI positive-going can occur at arbitrary location, but keep VDI low for 3 line duration time as a rough idea.

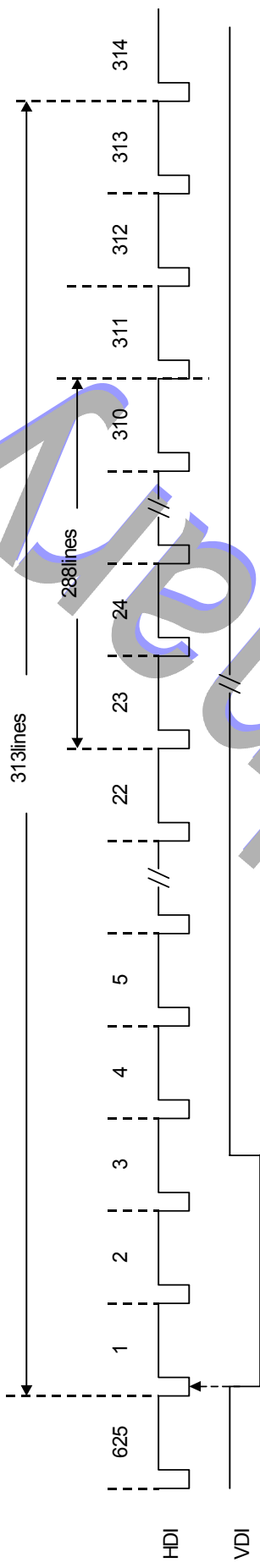
The Second Field ( EVEN )



\* ) VDI negative-going is not required for the Second Field. It is required for the First Field only ( VDI fed during the Second Field is ignored ).

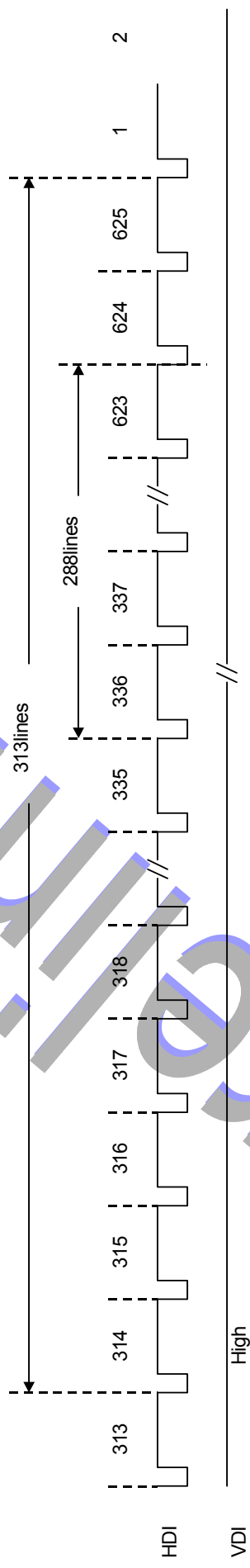
( a-3-2 ) PAL ( Frame ) 625 Line 576 active lines

The First Field ( ODD )



\* ) VDI negative-going should be fed during the time from 3 clocks prior to negative-going of HDI at L1 till 3 clocks prior to positive-going of HDI. VDI positive-going can occur at arbitrary location, but as a rough idea, keep VDI low for 2.5, or 2 or 3 line- duration time. Data fed at Line 23 is not output on Video output

The Second Field (EVEN)



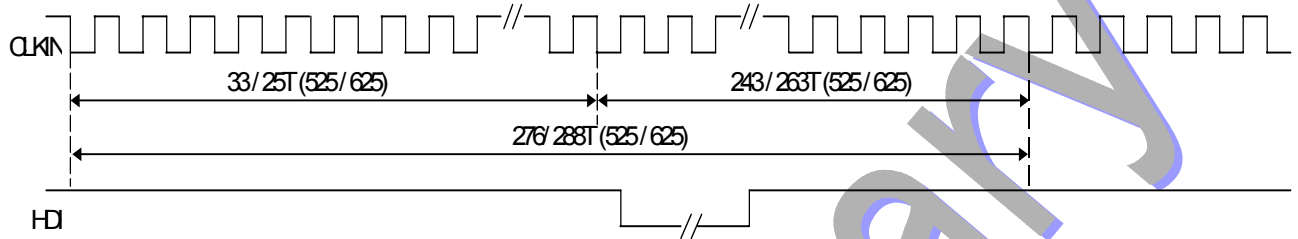
\* ) VDI negative-going is not required for the Second Field. It is required for the First Field only ( VDI fed during the Second Field is ignored ). Data fed at Line 623 is not output.

( b-1 ) ITU-R BT.656 Interface mode

The AK8817 makes a synchronization with an incoming signal by decoding EAV in the signal when ITU-R BT.656 encoded signal is input.

EAV code is located at the following position in the Video stream ( this mode of operation is not supported in the Square Pixel clock operation ).

|                    | EAV |     |     |     |     |     |     |     | SAV |  |     |     |     |  |  |     |     |     |     |     |    |   |    |   |    |
|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|-----|-----|-----|--|--|-----|-----|-----|-----|-----|----|---|----|---|----|
| Y/Cb/Cr            | Cb  | Y   | Cr  | Y   | Cb  | Y   | Cr  | Y   |     |  | Cb  | Y   | Cr  |  |  | Y   | Cb  | Y   | Cr  | Y   | Cb | Y | Cr | Y | Cb |
| Data#<br>525system | 360 | 720 | 360 | 721 | 361 | 722 | 361 | 723 |     |  | 368 | 736 | 368 |  |  | 865 | 428 | 866 | 428 | 867 | 0  | 0 | 0  | 1 | 1  |
| Data#<br>625system | 360 | 720 | 360 | 721 | 361 | 722 | 361 | 723 |     |  | 366 | 732 | 366 |  |  | 861 | 431 | 862 | 431 | 863 | 0  | 0 | 0  | 1 | 1  |



Preliminary



( 1 ) EAV Synchronization

an EAV code which is encoded on input signal is decoded, and the device makes synchronization with its timing. EAV / SAV codes are as follows.

Those codes succeeding 0xFF- 0x00- 0x00 which are fed as input data in 8-bit form become EAV / SAV codes. EAV / SAV codes have following meanings, starting with MSB.

| Bit Number |       | MSB |   |   |   |    |    |    |    | LSB |  |
|------------|-------|-----|---|---|---|----|----|----|----|-----|--|
| WORD       | VALUE | 7   | 6 | 5 | 4 | 3  | 2  | 1  | 0  |     |  |
| 0          | 0xFF  | 1   | 1 | 1 | 1 | 1  | 1  | 1  | 1  |     |  |
| 1          | 0x00  | 0   | 0 | 0 | 0 | 0  | 0  | 0  | 0  |     |  |
| 2          | 0x00  | 0   | 0 | 0 | 0 | 0  | 0  | 0  | 0  |     |  |
| 3          | 0xxx  | 1   | F | V | H | P3 | P2 | P1 | P0 |     |  |

here,

F = 0 : Field 1  
 = 1 : Field 2

V = 0 : other than Filed Blanking (V-Blanking)  
 = 1 : Filed Blanking (V-Blanking)

H = 0 : SAV  
 = 1 : EAV

P3, P2, P1, P0 : Protection Bit

Protection Bit and F / V / H relation is shown in the following table.

| F | V | H | P3 | P2 | P1 | P0 |
|---|---|---|----|----|----|----|
| 0 | 0 | 0 | 0  | 0  | 0  | 0  |
| 0 | 0 | 1 | 1  | 1  | 0  | 1  |
| 0 | 1 | 0 | 1  | 0  | 1  | 1  |
| 0 | 1 | 1 | 0  | 1  | 1  | 0  |
| 1 | 0 | 0 | 0  | 1  | 1  | 1  |
| 1 | 0 | 1 | 1  | 0  | 1  | 0  |
| 1 | 1 | 0 | 1  | 1  | 0  | 0  |
| 1 | 1 | 1 | 0  | 0  | 0  | 1  |

At NTSC data input case

| Cb  | Y   | Cr  | Y   | Cb  | Y   | Cr  | Y   | ..... | Cb  | Y   | Cr  | Y   | Cb | Y | Cr | Y |
|-----|-----|-----|-----|-----|-----|-----|-----|-------|-----|-----|-----|-----|----|---|----|---|
| 359 | 718 | 359 | 719 | 360 | 720 | 360 | 721 | ..... | 428 | 856 | 428 | 857 | 0  | 0 | 0  | 1 |
| EAV |     |     |     |     |     |     |     |       | SAV |     |     |     |    |   |    |   |

At PAL data input case

| Cb  | Y   | Cr  | Y   | Cb  | Y   | Cr  | Y   | ..... | Cb  | Y   | Cr  | Y   | Cb | Y | Cr | Y |
|-----|-----|-----|-----|-----|-----|-----|-----|-------|-----|-----|-----|-----|----|---|----|---|
| 359 | 718 | 359 | 719 | 360 | 720 | 360 | 721 | ..... | 431 | 862 | 431 | 863 | 0  | 0 | 0  | 1 |
| EAV |     |     |     |     |     |     |     |       | SAV |     |     |     |    |   |    |   |

( 1-1 ) EAV / SAV Code and Line Synchronization

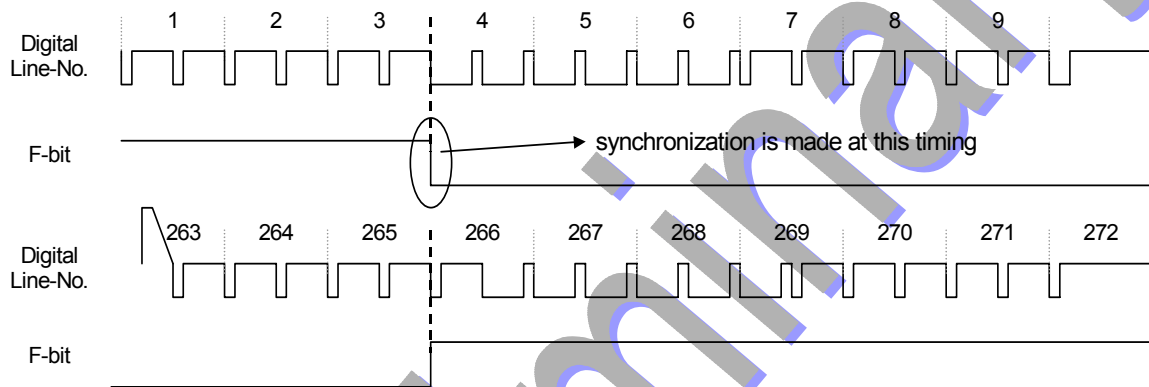
The AK8817 makes Vertical synchronization ( Line synchronization ) when F-bit in EAV makes transition from " 1 " to " 0 " .

F-bit of EAV / SAV and Line relation is as follows

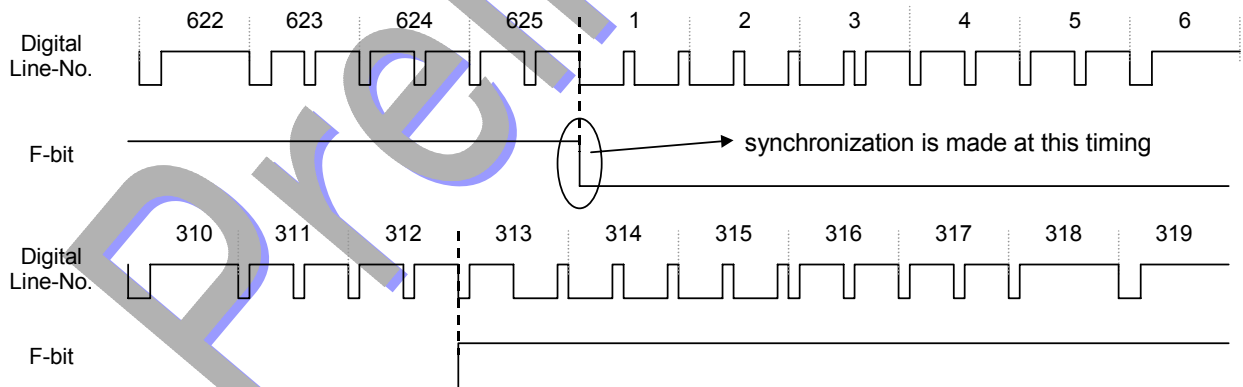
| F-bit | NTSC                               | PAL               |
|-------|------------------------------------|-------------------|
| 0     | Line4 – Line265                    | Line1 – Line312   |
| 1     | Line266 – Line525<br>Line1 – Line3 | Line313 – Line625 |

For reference, V-bit of EAV / SAV and Line relation is also shown below.

| Field   | V-bit       | NTSC              | PAL                        |
|---------|-------------|-------------------|----------------------------|
| Field 1 | Start (V=1) | Line1 – Line19    | Line624 – Line625 – Line22 |
|         | End (V=0)   | Line20 – Line263  | Line23 – Line310           |
| Field 2 | Start (V=1) | Line264 – Line282 | Line311 – Line335          |
|         | End (V=0)   | Line283 – Line525 | Line336 – Line623          |



Line Synchronization by EAV at NTSC input case



Line Synchronization by EAV at PAL input

(15) On-chip Color Bar

The AK8817 can output Color Bar signal.

Color Bar signal to be generated has 100 % amplitude and 75 % Saturation levels.

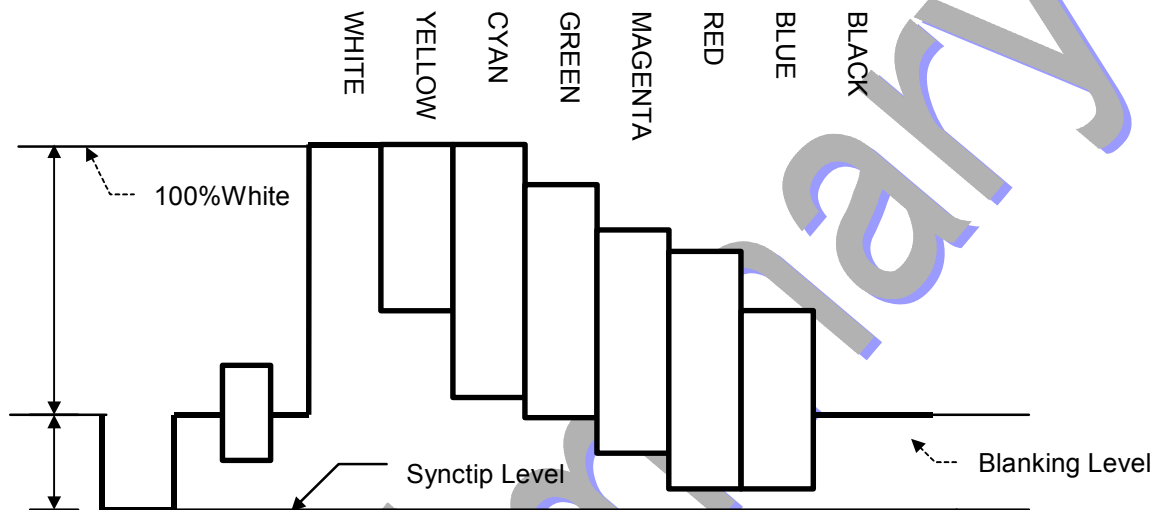
Color Bar signal is output by setting register.

When to output Color Bar signal, there are 2 modes of operation – one is external Sync timing mode for normal operation, and the other is internal self-operation mode.

In internal self-operating mode, required timing is internally generated automatically. Namely, it is no need to input synchronization timing from outside of the chip.

Operation mode setting is done by Control 1 Register .

When BBG-bit is set, BBG-bit is prioritized ( Black Burst is output ).



The following values are code for ITU-R. BT601

|    | WHITE | YELLOW | CYAN | GREEN | MAGENTA | RED | BLUE | BLACK |
|----|-------|--------|------|-------|---------|-----|------|-------|
| Cb | 128   | 44     | 156  | 72    | 184     | 100 | 212  | 128   |
| Y  | 235   | 162    | 131  | 112   | 84      | 65  | 35   | 16    |
| Cr | 128   | 142    | 44   | 58    | 198     | 212 | 114  | 128   |

(16) Black Burst Signal generation function

The AK8817 can output Black Burst signal ( Black level output ).

When to output Black Burst signal, there are 2 modes of operation – one is external Sync timing mode for normal operation , and the other is internal self-operation mode.

In internal self-operation mode, required timing is internally generated automatically. Namely, it is no need to input synchronization timing from outside of the chip.

When BBG-bit of [ Control 1 Register ] is set to “1”, same operation is processed as in the case where fixed-16 Y signal and

fixed-128 Cb / Cr signal outputs are input.

Operation mode setting is done by Control 1 Register setting.

(17) Video ID

The AK8817 supports to encode the Video ID ( EIAJ CPR-1204 ) which distinguishes the aspect ratio etc..

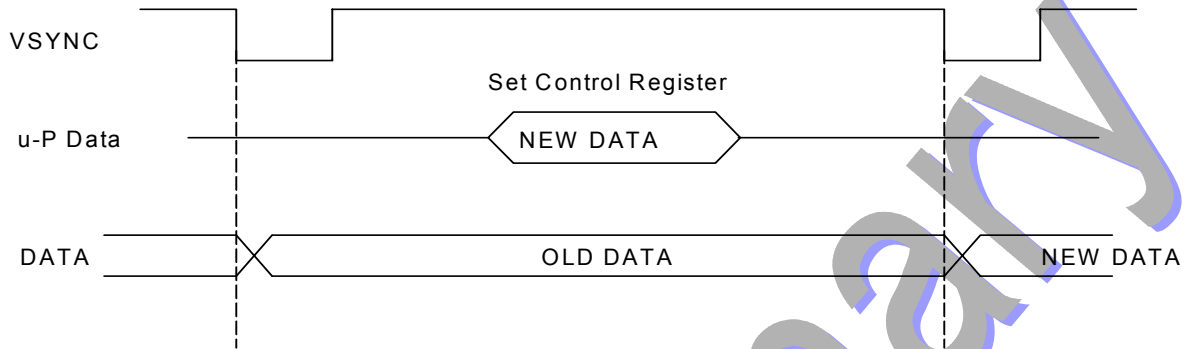
This is also used as CGMS ( Copy Generation Management System ).

Turning "ON/OFF" of this function is made by setting both VMOD-bit = 0 and VBID-bit = 1 of { Control 1 Register (0x00) }.

And data to be set is written into { VBID / WSS Data1 & 2 Registers ( 0x02,0x03 )}.

Video ID information is the highest order of priority information among VBI information

VBID Data Update timing



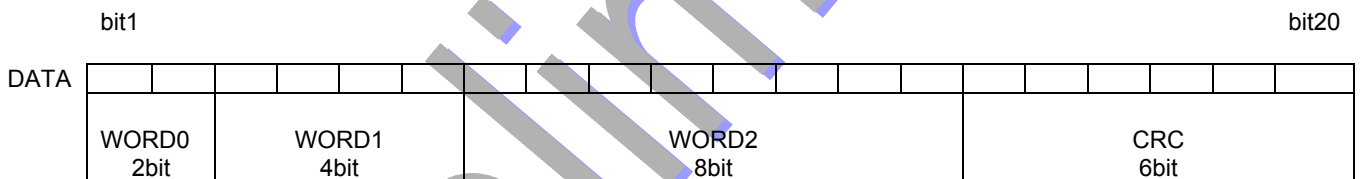
VBID Code assignment

20 bit data is configured with WORD0 = 2 bit, WORD1 = 4 bit, WORD2 = 8 bit and CRC = 6 bit.

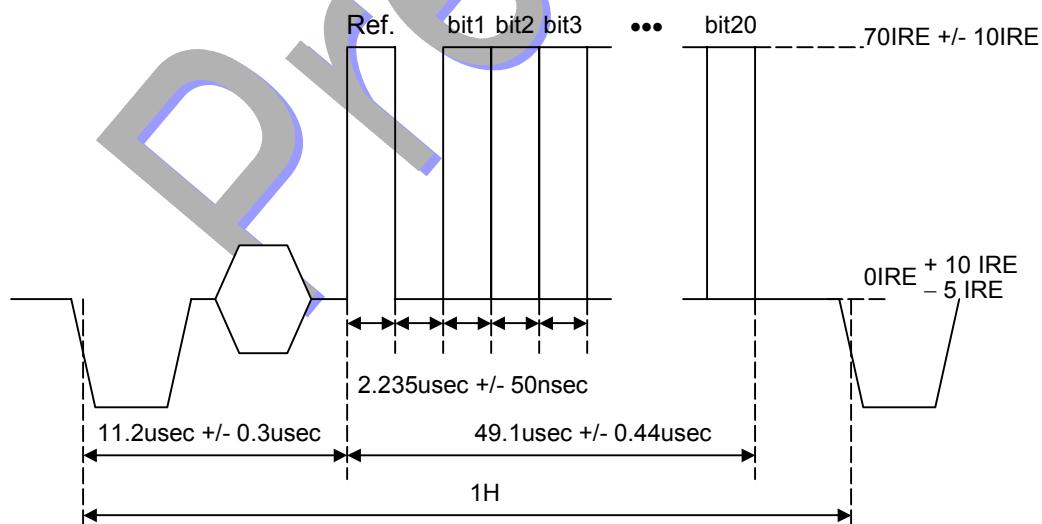
CRC is automatically calculated and added by the AK8817.

Default values of CRC polynomial expression  $X^6 + X + 1$  are all ones.

-data configuration



VBID Waveform

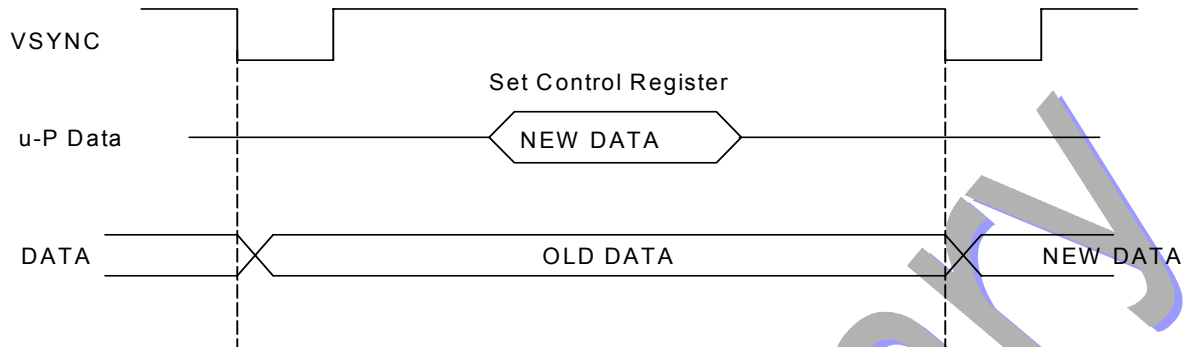


|             |               |
|-------------|---------------|
|             | 525/60 System |
| Amplitude   | 70IRE         |
| Encode Line | 20/283        |

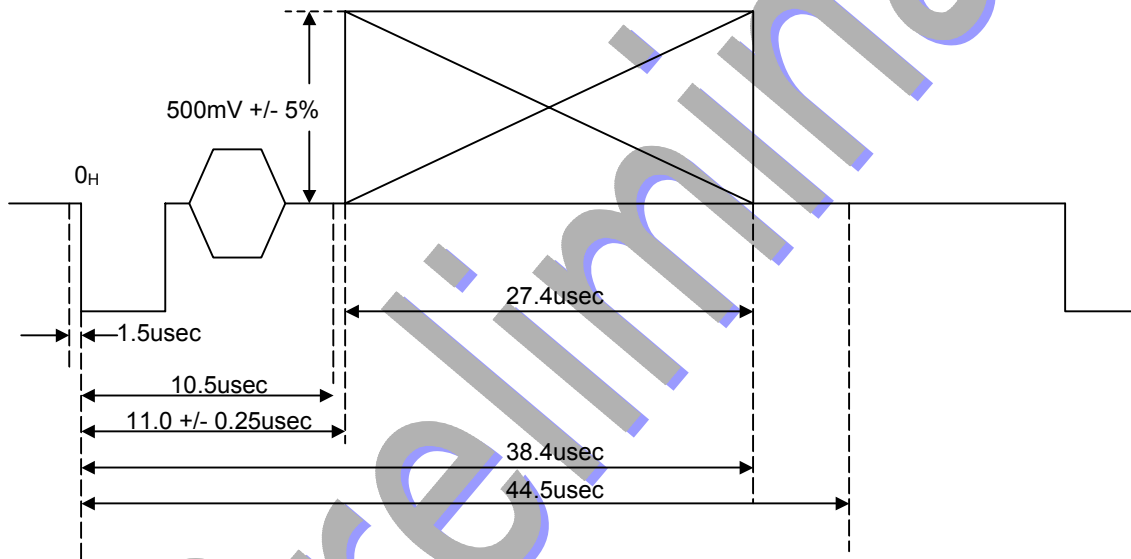
( 17 ) WSS function

The AK8817 supports to encode the WSS ( ITU-R. BT.1119 ) which distinguishes the aspect ratio and sets CGMS-A etc.. Turning "ON/OFF" of this function is made by setting both VMOD-bit = 1 and WSS-bit = 1 of { Control 1 Register ( 0x00 ) }. And data to be set is written into { VBID / WSS Data1 & 2 Registers ( 0x02, 0x03 )}.

WSS Data Update timing



WSS Waveform



Encode line : former half of Line 23 ( Blank output during latter half )

Coding : Bi-phase modulation coding

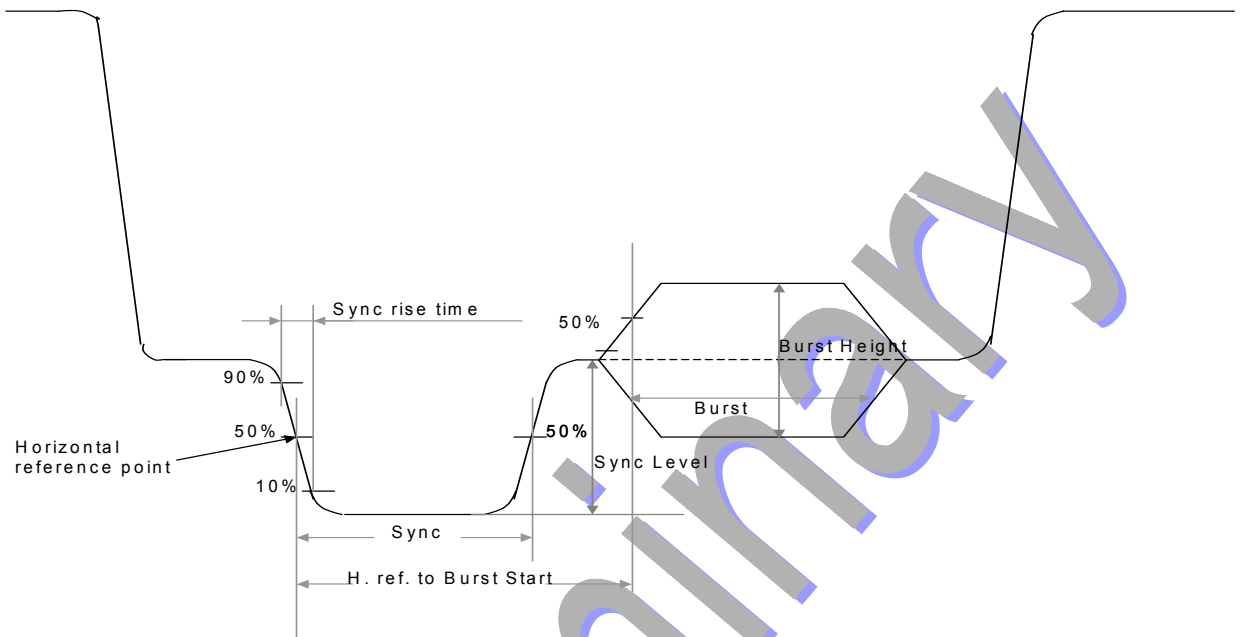
Clock : 5 MHz ( Ts = 200 nS )

Encoding details as follows

| Run-in      | Start code  | Group 1 Aspect ratio                | Group 2 Enhanced Services           | Group 3 Subtitles                  | Group4 Reserved                      |
|-------------|-------------|-------------------------------------|-------------------------------------|------------------------------------|--------------------------------------|
| 29 elements | 24 elements | 24 elements                         | 24 elements                         | 18 elements                        | 18 elements                          |
|             |             | Bit numbering<br>0 1 2 3<br>LSB MSB | Bit numbering<br>4 5 6 7<br>LSB MSB | Bit numbering<br>8 9 10<br>LSB MSB | Bit numbering<br>11 12 13<br>LSB MSB |
|             |             | 0 : 000111<br>1 : 111000            | 0 : 000111<br>1 : 111000            | 0 : 000111<br>1 : 111000           | 0 : 000111<br>1 : 111000             |
| 0x1F1C71C7  | 0x1E3C1F    |                                     |                                     |                                    |                                      |

**SYNC Signal waveform, Burst Waveform generator**

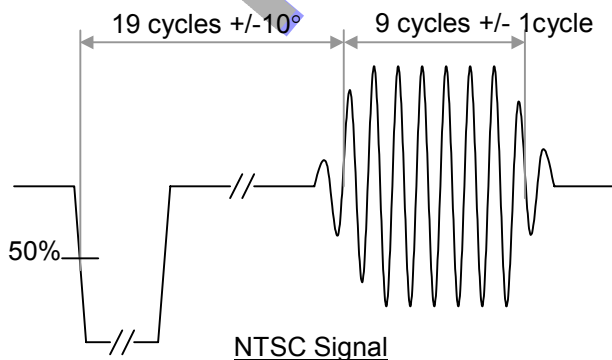
(1) NTSC-J



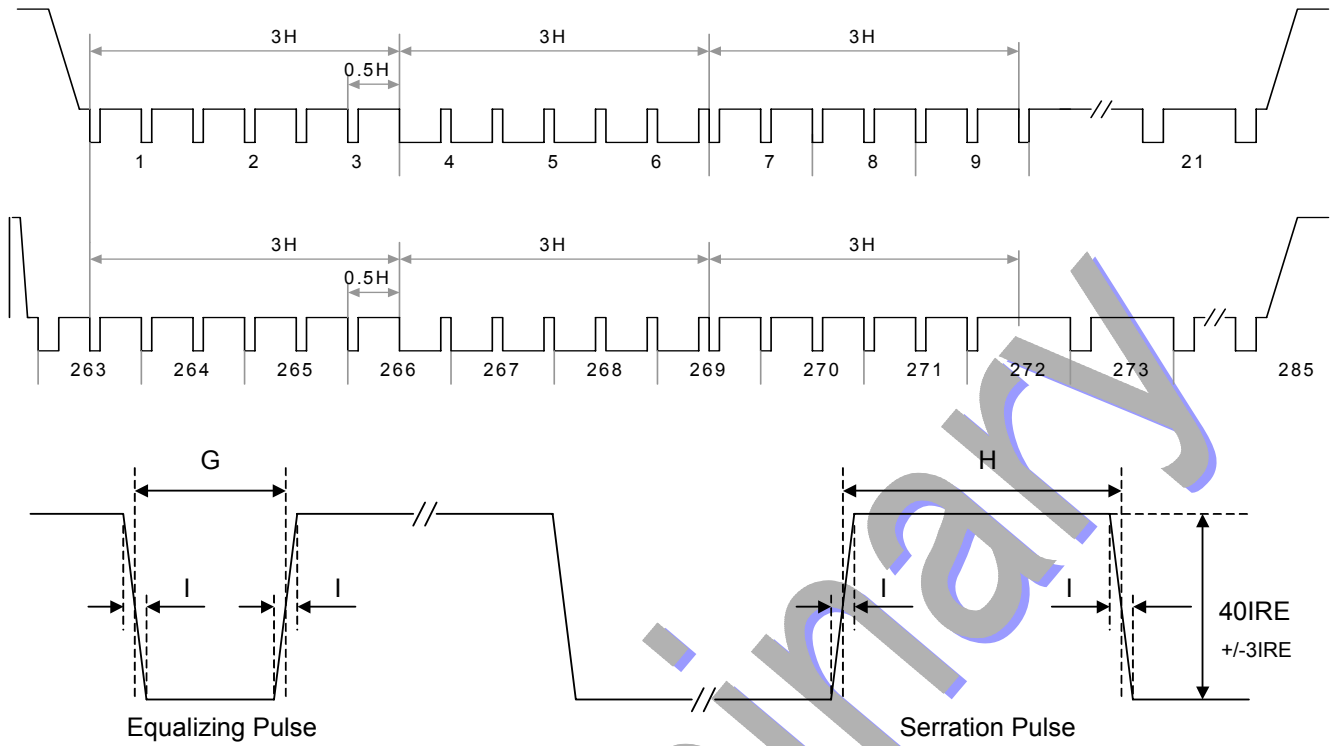
|   | measurement point | value  | Consumer Quality tolerance | units  |
|---|-------------------|--------|----------------------------|--------|
| Total line period(derived)                |                   | 63.556 |                            | usec   |
| Sync Level                                |                   | 40     | +/- 3                      | IRE    |
| Sync rise time                            | 10% - 90%         | 140    | Max 250                    | nsec   |
| Horizontal Sync width                     | 50%               | 4.7    | +/- 0.1                    | usec   |
| Horizontal reference point to burst start | 50%               | 19     | defined by SC/H            | cycles |
| Burst *                                   | 50%               | 9      | +/- 1                      | cycles |
| Burst Height **                           |                   | 40     | +/- 3                      | IRE    |

\* there is a case where tolerance of Sync rise time is added to Sync width tolerance.

\* Measurement of Burst time length is made between the Burst start point which is defined as the zero-cross point, preceding the first half-cycle of the sub-carrier where Burst amplitude becomes higher than 50 % level and the Burst end point, defined in the same manner.



(2) Vertical Sync Signal timing ( NTSC )

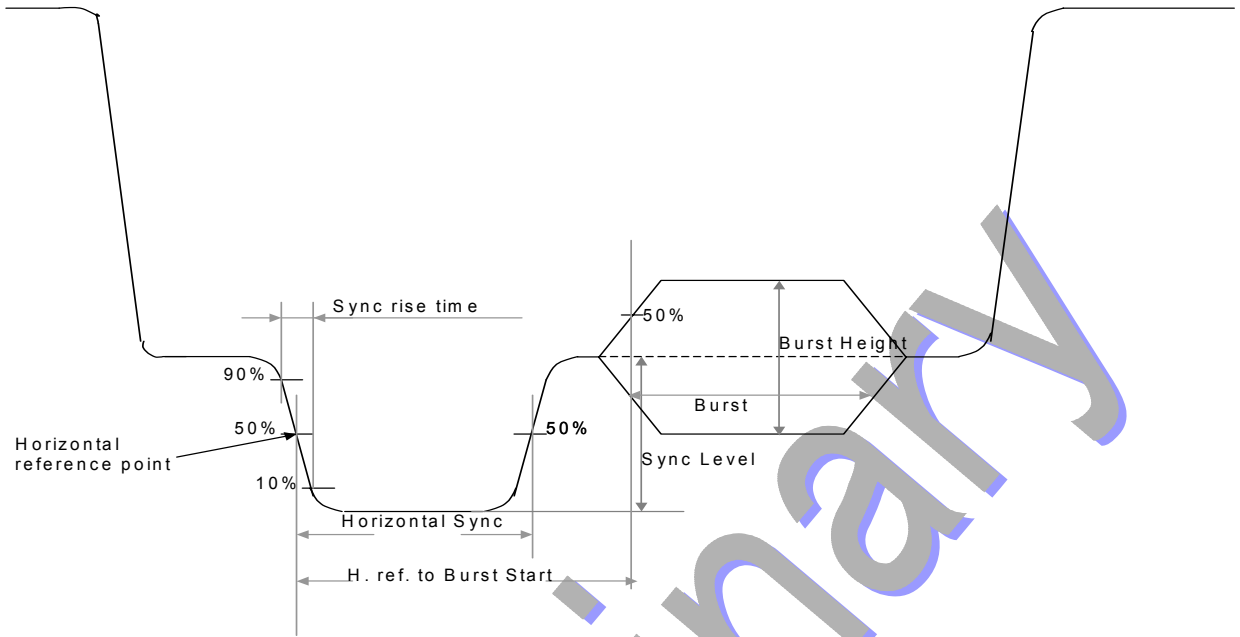


Equalizing Pulse and Serration Pulse

| Symbol |                                | Measurement point | Value | Recommended tolerance | units |
|--------|--------------------------------|-------------------|-------|-----------------------|-------|
| G      | Pre-equalizing pulse width     | 50%               | 2.3   | +/- 0.1               | usec  |
| H      | Vertical serration pulse width | 50%               | 4.7   | +/- 0.2               | usec  |
| G      | Post-equalizing pulse width    | 50%               | 2.3   | +/- 0.1               | usec  |
| I      | Sync rise time                 |                   | 140   | Max 250               | nsec  |

\* there is a case where tolerance of Sync rise time is added to Pulse width tolerance.

(3) PAL-B,D,G,H,I



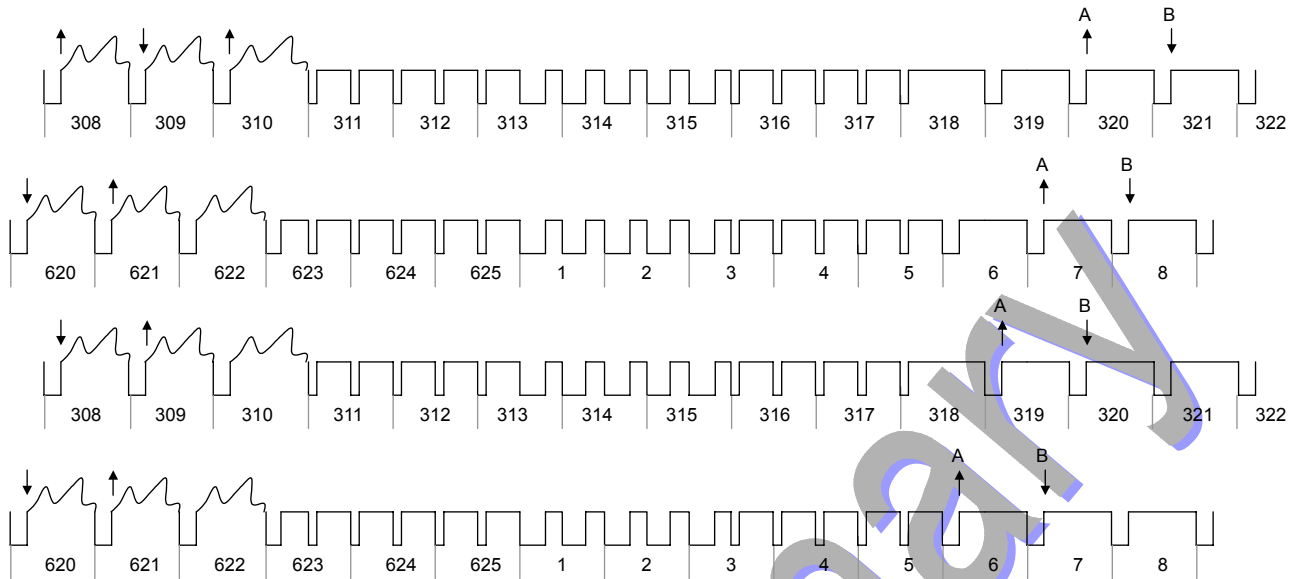
|   | measurement point | value | Consumer Quality tolerance | units  |
|---|-------------------|-------|----------------------------|--------|
| Total line period(derived)                |                   | 64.0  |                            | usec   |
| Sync Level                                |                   | 300   | +/- 20                     | mV     |
| Sync rise time                            | 10% - 90%         | 0.2   | Max 0.3                    | usec   |
| Horizontal Sync width                     | 50%               | 4.7   | +/- 0.2                    | usec   |
| Horizontal reference point to burst start | 50%               | 5.6   | +/- 0.1                    | usec   |
| Burst *                                   | 50%               | 10    | +/- 1                      | cycles |
| Burst Height **                           |                   | 300   | +/- 30                     | mV     |

\* there is case where tolerance of Sync rise time is added to Sync width tolerance.



(4) Vertical Sync Signal timing and Burst Phase

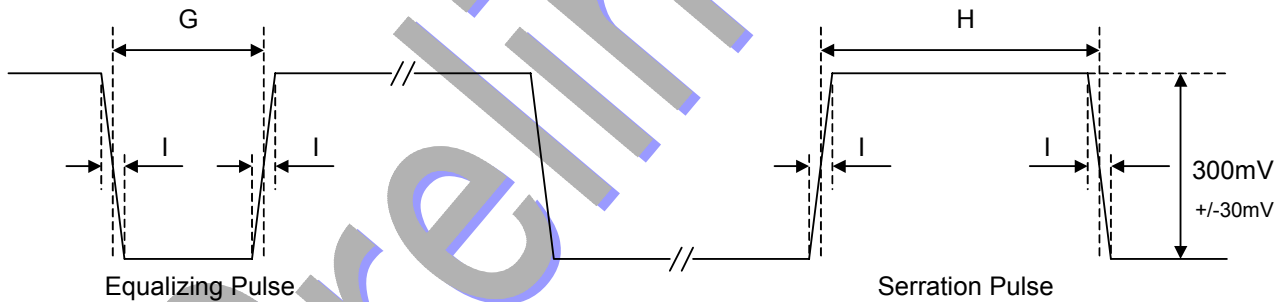
PAL-B,D,G,H,I



A : Phase of Burst : nominal Value + 135°  
 B : Phase of Burst : nominal Value - 135°

Since Burst frequency and Line frequency are not practically in integer-multiple relation, specified phase value is not exactly 135 degrees.

Diagram below shows phase direction.



Equalizing Pulse and Serration Pulse

| Symbol |                                | Measurement point | Value | Recommended tolerance | units |
|--------|--------------------------------|-------------------|-------|-----------------------|-------|
| G      | Pre-equalizing pulse width     | 50%               | 2.35  | +/- 0.1               | usec  |
| H      | Vertical serration pulse width | 50%               | 4.7   | +/- 0.2               | usec  |
| G      | Post-equalizing pulse width    | 50%               | 2.35  | +/- 0.1               | usec  |
| I      | Sync rise time                 |                   | 200   | Max 300               | nsec  |

\* there is a case where tolerance of Sync rise time is added to Pulse width tolerance.

**Register Map**

| Address | Register                         | Default | R/W | Function  |
|---------|----------------------------------|---------|-----|---|
| 0x00    | Control 1 Register               | 0x00    | R/W | Mode set Register   |
| 0x01    | Control 2 Register               | 0x00    | R/W | Mode set Register   |
| 0x02    | VBID/WSS Data 1 Register         | 0x00    | R/W | VBID data is set, WSS data is set                               |
| 0x03    | VBID/WSS Data 2 Register         | 0x00    | R/W | VBID data is set, WSS data is set                               |
| 0x04    | Input Control Register           | 0x00    | R/W | Input control register for out-of-standard quality input signal |
| 0x05    | Device ID & Revision ID Register | 0x17    | R   | Register for Device ID and Revision ID                          |
|         |                                  |         |     |   |

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**Control 1 Register (R/W) [Address 0x00]****Sub Address 0x00****Default Value 0x00**

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| DAC           | BBG   | CBG   | MASMD | WSS   | VBID  | SCR   | VMOD  |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Control 1 Register Definition**

| BIT   | Register Name |                           | R/W | Definition   |
|-------|---------------|---------------------------|-----|--|
| bit 0 | VMOD          | Video Mode bit            | R/W | 0: NTSC<br>1: PAL  |
| bit 1 | SCR           | Sub-Carrier Reset bit     | R/W | 0 : Sub-Carrier Reset<br>1 : Sub-Carrier Reset off   |
| bit 2 | VBID          | VBID Set bit              | R/W | 0 : VBID OFF<br>1 : VBID ON  |
| bit 3 | WSS           | WSS Set bit               | R/W | 0 : WSS OFF<br>1 : WSS ON  |
| bit 4 | MASMD         | Master Mode bit           | R/W | Master Mode bit to set Sync mode when Color Bar signal and Black Burst signal are generated<br>0 : operation by an external Sync timing<br>1 : operation by an internal self-operating mode ( master mode )<br>note ) Master mode bit is still valid in normal data input, but output video is not synchronized. |
| bit 5 | CBG           | Color Bar Generator bit   | R/W | 0: OFF<br>1: ON<br>when BBG is set, BBG is prioritized.  |
| bit 6 | BBG           | Black Burst Generator bit | R/W | 0 : OFF<br>1 : ON  |
| bit 7 | DAC           | DAC Set bit               | R/W | 0 : DAC OFF<br>1 : DAC ON  |

**Control 2 Register (R/W) [Address 0x01]**

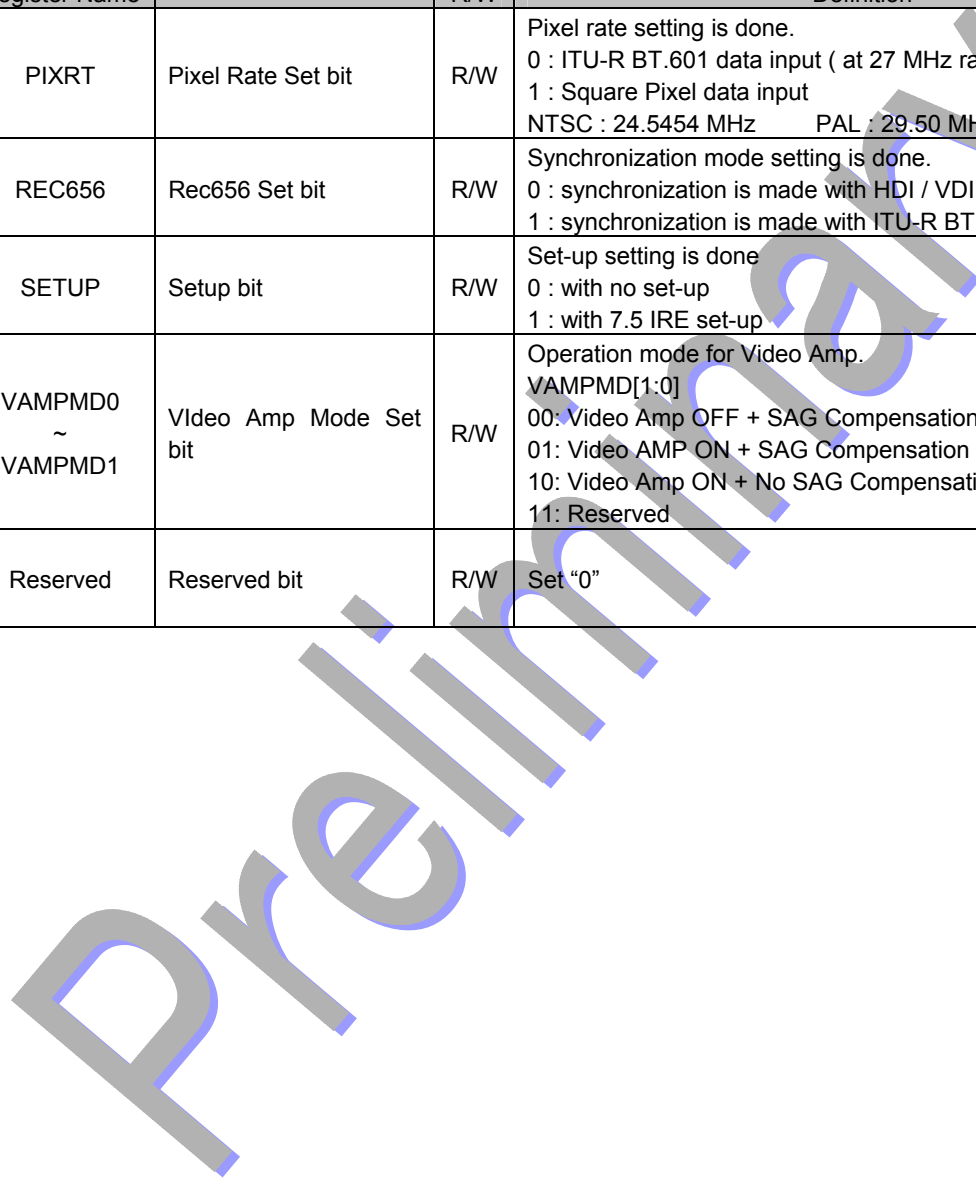
**Sub Address 0x01**

**Default Value 0x00**

| bit 7         | bit 6    | bit 5    | bit 4   | bit 3   | bit 2 | bit 1  | bit 0 |
|---------------|----------|----------|---------|---------|-------|--------|-------|
| Reserved      | Reserved | Reserved | VAMPMD1 | VAMPMD0 | SETUP | REC656 | PIXRT |
| Default Value |          |          |         |         |       |        |       |
| 0             | 0        | 0        | 0       | 0       | 0     | 0      | 0     |

**Control 2 Register Definition**

| BIT                 | Register Name           |                        | R/W | Definition   |
|---------------------|-------------------------|------------------------|-----|--|
| bit 0               | PIXRT                   | Pixel Rate Set bit     | R/W | Pixel rate setting is done.<br>0 : ITU-R BT.601 data input ( at 27 MHz rate )<br>1 : Square Pixel data input<br>NTSC : 24.5454 MHz      PAL : 29.50 MHz                                      |
| bit 1               | REC656                  | Rec656 Set bit         | R/W | Synchronization mode setting is done.<br>0 : synchronization is made with HDI / VDI input.<br>1 : synchronization is made with ITU-R BT.656 data input                                       |
| bit 2               | SETUP                   | Setup bit              | R/W | Set-up setting is done<br>0 : with no set-up<br>1 : with 7.5 IRE set-up  |
| bit 3<br>~<br>bit 4 | VAMPMD0<br>~<br>VAMPMD1 | Video Amp Mode Set bit | R/W | Operation mode for Video Amp.<br>VAMPMD[1:0]<br>00: Video Amp OFF + SAG Compensation OFF<br>01: Video AMP ON + SAG Compensation ON<br>10: Video Amp ON + No SAG Compensation<br>11: Reserved |
| bit 5<br>~<br>bit 7 | Reserved                | Reserved bit           | R/W | Set "0"  |



**VBID/WSS 1 Register (R/W) [Address 0x02]**  
**VBID/WSS 2 Register (R/W) [Address 0x03]**

Video ID and WSS data setting are made. A common data register is used for both video ID and WSS data.

When VBID bit of mode register is set in NTSC mode, data is for VBID data ,and when WSS bit of Control 1 Register is set in

PAL mode, data is for WSS data.

When VBID-bit is “1” and VMOD-bit is “0” in Control 1 Register , the following bits are assigned.

**Sub Address 0x02** **default Value 0x00**

| bit 7         | bit 6 | bit 5 | bit 4  | bit 3  | bit 2  | bit 1  | bit 0  |
|---------------|-------|-------|--------|--------|--------|--------|--------|
| VBID7         | VBID8 | VBID9 | VBID10 | VBID11 | VBID12 | VBID13 | VBID14 |
| Default Value |       |       |        |        |        |        |        |
| 0             | 0     | 0     | 0      | 0      | 0      | 0      | 0      |

**Sub Address 0x03** **default Value 0x00**

| bit 7         | bit 6    | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|----------|-------|-------|-------|-------|-------|-------|
| Reserved      | Reserved | VBID1 | VBID2 | VBID3 | VBID4 | VBID5 | VBID6 |
| Default Value |          |       |       |       |       |       |       |
| 0             | 0        | 0     | 0     | 0     | 0     | 0     | 0     |

Note ) “0” should be written into reserved bits.

VBID1 ---- VBID14 above correspond to the bit 1 ---- bit 14 which are described at { VBID Data Code Assignment } in { ( 14 ) Video ID } section.

A 6-bit CRC code from bit 15 ~ bit 20 is automatically added by the AK8817.

Data is retained till data is updated to a new one.

Following bits are assigned when WSS-bit is “1” and VMOD-bit is “1” in Control 1 Register .

**Sub Address 0x02** **default Value 0x00**

| bit 7         | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| G2-7          | G2-6  | G2-5  | G2-4  | G1-3  | G1-2  | G1-1  | G1-0  |
| Default Value |       |       |       |       |       |       |       |
| 0             | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

**Sub Address 0x03** **default Value 0x00**

| bit 7         | bit 6    | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------------|----------|-------|-------|-------|-------|-------|-------|
| Reserved      | Reserved | G4-13 | G4-12 | G4-11 | G3-10 | G3-9  | G3-8  |
| Default Value |          |       |       |       |       |       |       |
| 0             | 0        | 0     | 0     | 0     | 0     | 0     | 0     |

Note ) WSS data is written with 0x01 first, then 0x02 in this order.

When the 2<sup>nd</sup> byte ( 0x02 ) of WSS data is written, the AK8817 interprets that data is updated to a new one and then encodes it to the next video line ( Line 23 ).

Data is retained till data is updated to a new one.

**Input Control Register (R/W) [Address 0x04]**

This is an out-of-standard quality input signal control register.

**Sub Address 0x04****default Value 0x00**

| bit 7    | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| Reserved | CBCR  | VD2   | VD1   | VD0   | HD2   | HD1   | HD0   |
| 0        | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

Adjustment of Sync input timing is made.

| BIT                 | Register Name   |                 | R/W | Definition   |
|---------------------|-----------------|-----------------|-----|--|
| bit 0<br>~<br>bit 2 | HD0<br>~<br>HD2 | HDI Input Delay | R/W | HDI signal input is delayed by the set value.<br>HD [ 2:0 ] system clock count delay ( + 0 ~ + 7 CLK delay ) |
| bit 3<br>~<br>bit 5 | VD0<br>~<br>VD2 | VDI Input Delay | R/W | VDI signal input is delayed by the set value.<br>VD [ 2:0 ] system clock count delay ( + 0 ~ + 7 CLK delay ) |
| bit 6               | CBCR            | Exchange CbCr   | R/W | Cb, Cr timing data are interchanged at CBCR = 1.   |
| bit 7               | Reserved        | Reserved        | R/W | Reserved   |

Preliminary

**Device ID and Revision ID Register (R) [Address 0x05]**

Register to show Device ID & Revision of the AK8817.

Device ID for AK8817 is 0x17(decimal)

Initial Version of the Revision ID is 0x00.

Revision number is modified only when a control software needs to be modified.

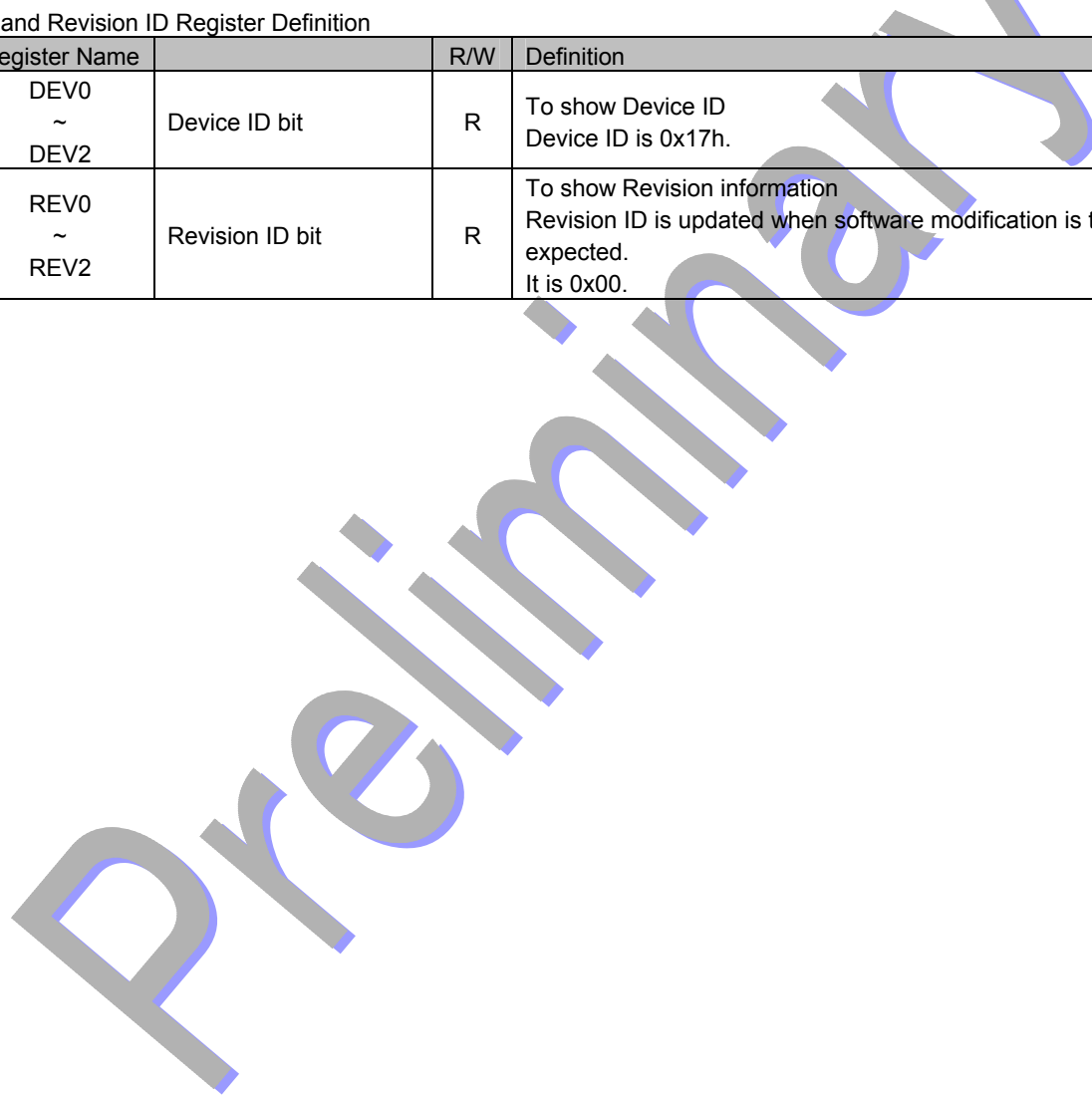
**Sub Address 0x5**

**default Value 0x17**

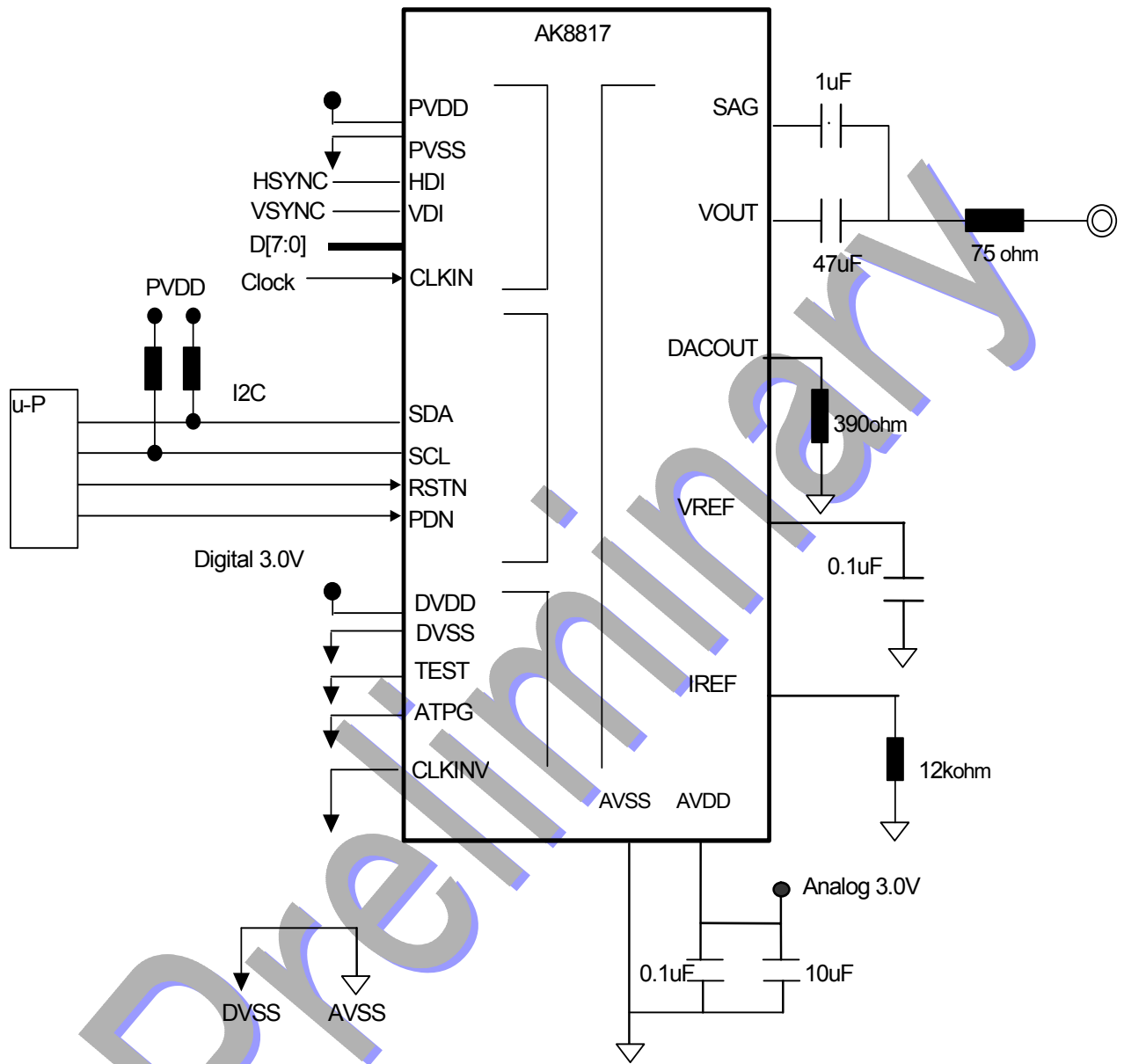
| bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Rev1  | REV0  | DEV5  | DEV4  | DEV3  | DEV2  | DEV1  | DEV0  |
| 0     | 0     | 0     | 1     | 0     | 1     | 1     | 1     |

Device ID and Revision ID Register Definition

| BIT                 | Register Name     |                 | R/W | Definition  |
|---------------------|-------------------|-----------------|-----|---|
| bit 0<br>~<br>bit 5 | DEV0<br>~<br>DEV2 | Device ID bit   | R   | To show Device ID<br>Device ID is 0x17h.  |
| bit 6<br>~<br>bit 7 | REV0<br>~<br>REV2 | Revision ID bit | R   | To show Revision information<br>Revision ID is updated when software modification is to be expected.<br>It is 0x00. |



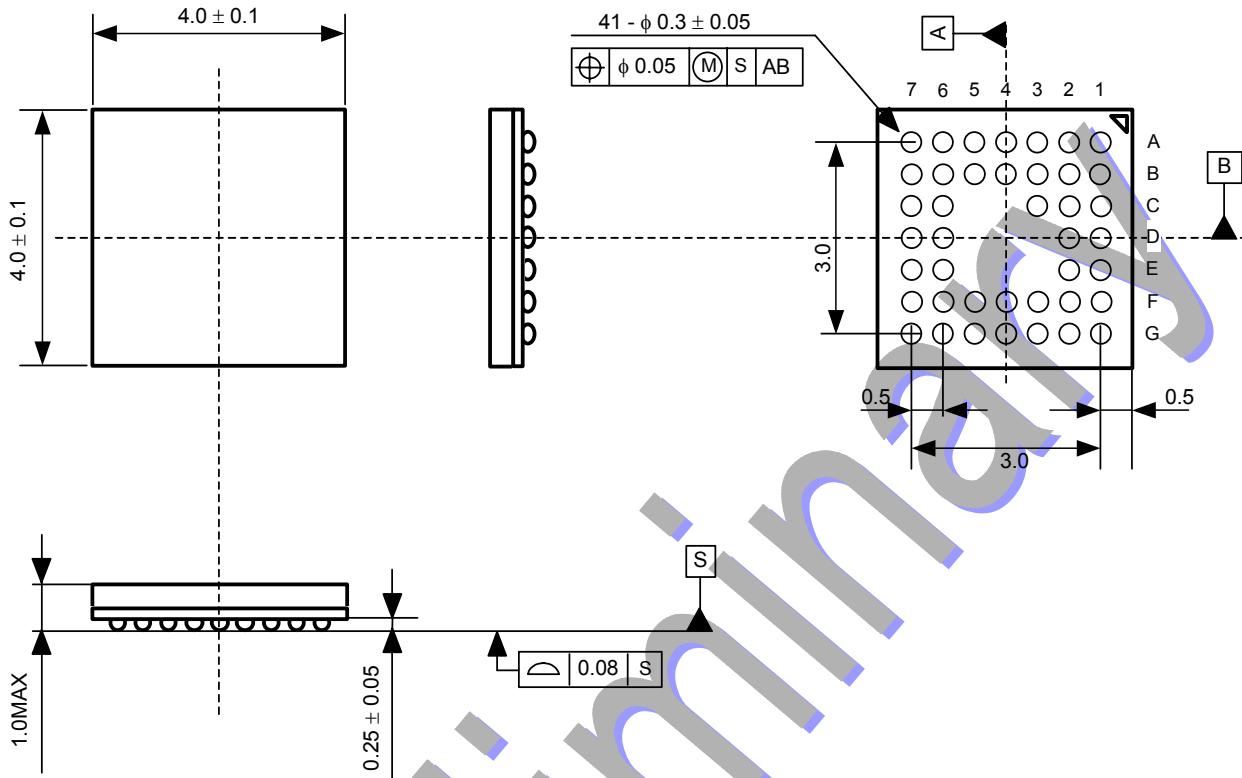
### System Connection Example





**Package Drawing**

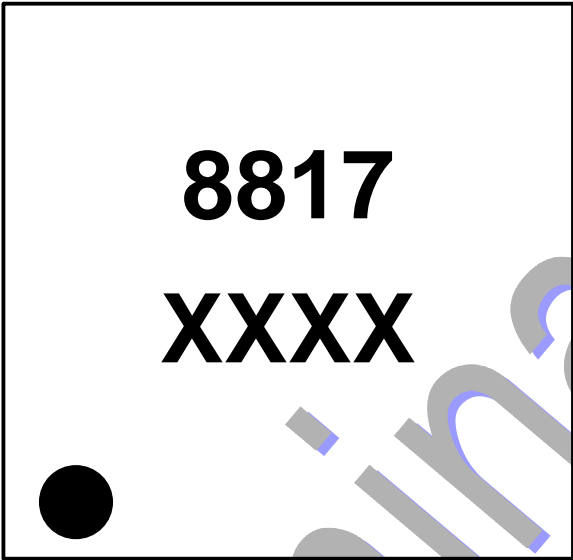
41pin FBGA



**Package & Lead frame material**

Package molding compound: Epoxy  
 Interposer material: BT resin  
 Solder ball material: SnAgCu

**Package Marking Drawing**



- a. Package Type: BGA
- b. Number of Pins: 41pins (Including INDEX pin )
- c. Product Number: 8817
- d. Control Code: XXXXX (4 digits)

Preliminary

liminary

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