AMD

Home Networking Board Design Using PCnet™-Home Devices

Application Note

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This application note is intended to assist customers in using AMD's Am79C978/Am79C978A PCnet™-Home devices. Details concerning application information, circuit design, EMI, printed circuit layout techniques, and component selection are provided to help ensure first-pass success in implementing a functional design that has optimized signal quality. This document should be used in conjunction with the product data sheet for functional descriptions and features of the devices, as well as the OrCAD schematics provided in the Evaluation Kit and on AMD's web page. Contact your local AMD Field Applications Engineer or Sales Office to ask any questions and discuss any concerns you may have.

INTRODUCTION

The Am79C978/Am79C978A devices are highly integrated PCI Home Networking devices implementing a Fast-Ethernet 10/100 Mbps 802.3 Media Access Controller, 10BASE-T Physical Transceiver, and 1 Mbps HomePNA technology. Figure 1 shows the block diagram of the PCnet-Home device.

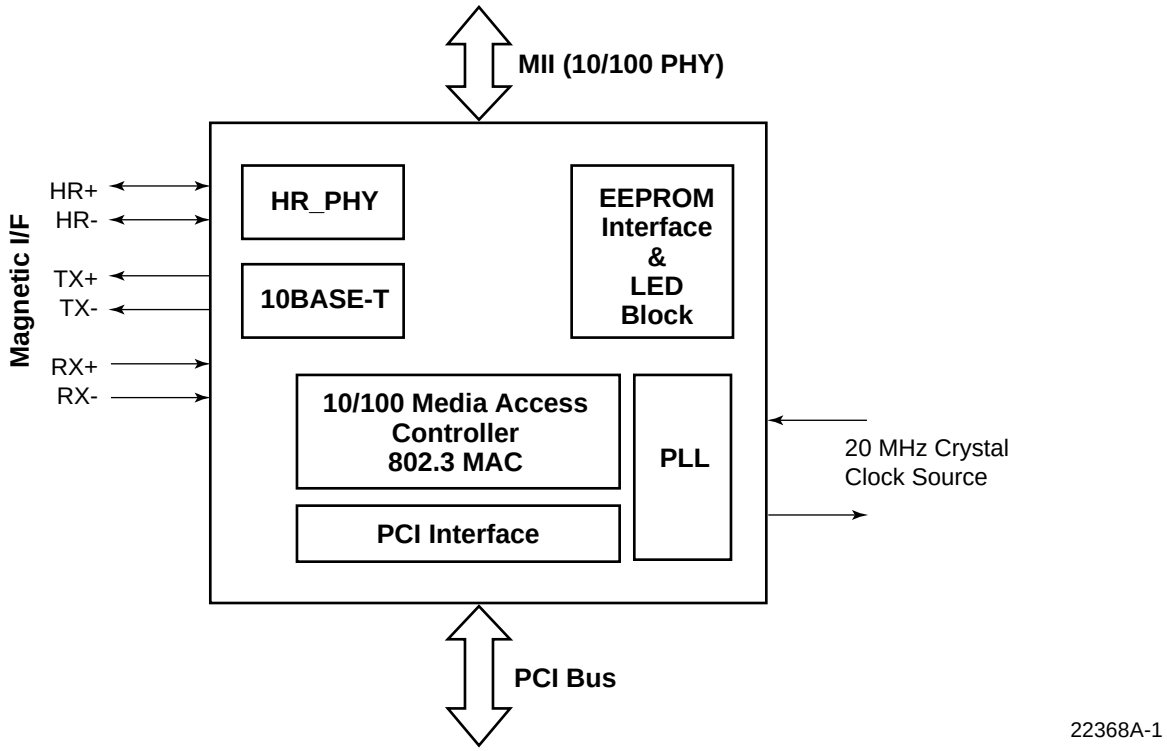

Figure 1. PCnet-Home Block Diagram

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Board Design Features

The Am79C978/Am79C978A PCnet-Home devices have the following features:

- Integrated 1 Mbps HomePNA PHY, 10BASE-T PHY, and 10/100 Mbps MAC
- Integrated magnetics with HomePNA bandpass filter and power surge protection against lightning
- EEPROM for subvendor and subsystem ID, as well as a 48-bit MAC address
- Magic Packet™ interfaced to motherboards supporting remote wake-up LAN
- Lowpass filter to prevent noise from the phone or G.lite to the HomePNA line
- NetPHY™-1LP (10/100 PHY) interface
- Two RJ-11s (one for HomePNA port or one for Phone/G.lite) and one RJ-45 for Ethernet port
- LEDs for Link, Activity, Speed, and Collision
- Glueless PCI 2.1 compliant interface
- PCI power management support
- PC98/PC99 compliance

Device Placement And Routing

The adapter card design in the appendix shows the optimized placement of the components (see layout plot). The pin location for the Am79C978/Am79C978A devices have been chosen to allow for minimum length signal routing. Short signal traces reduce the capacitive loading caused by the signal trace and noise from adjacent signals. Care should be given to avoid the routing of digital signals across the analog boundaries

Since there is minimum filtering on the secondary side of the transformer, it is also recommended that integrated magnetics are placed near the PCI bracket (next to the RJ-11) to prevent any EMI noise issue. See the appendix for PCB layout and placement.

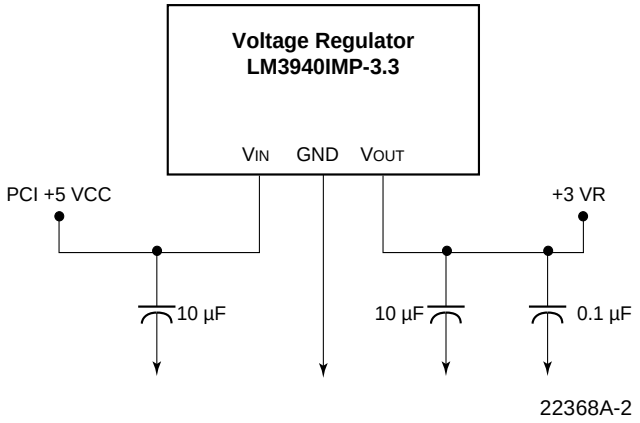


Figure 2. Typical Linear Regulator Implementation

POWER SUPPLY

AMD's PCnet-Home devices operate from a +3.3 V ±300 mV power supply. Some PCI systems do not have an available +3.3 V supply. The easiest way to convert from a +5 V supply to a +3.3 V supply is through the use of a linear regulator. See Figure 2. Converting from a +12 V supply to a +3.3 V supply is not recommended due to the additional power dissipation.

In addition, for optimal small signal receive sensitivity performance, a linear regulator should be used. The advantage of a linear regulator is that it provides a very quiet output, isolated from the noise on the +5 V digital supply from the PCI bus. Since small signal receive performance is sensitive to power supply noise, the clean outputs of the linear regulator contribute to improved receive performance.

Bypass Capacitors

Great care should be given to the power distribution and decoupling of specific Am79C978/Am79C978A power pins. Poor power decoupling on these pins can cause degradation of the HomePNA small signal receive sensitivity by as much as 5 mV.

Bypass capacitors are more effective when located close to VDD and VSS pins of the chip. See Table 1 for pins that require bypass. In the case of a 4-layer PCB design, it is recommended that each VDD and VSS pin be supplied from their own vias. The preferred method for the layout of the bypass capacitors is shown in Figure 3.

Table 1. Suggested Bypassed Power Pins for 160 PQFP

Pin No.	Power Names	Bypass Caps
100	VDDCO – power for PLL	0.1 µF – 0.2 µF
103	VDDHR_RX – power for HomePNA	0.1 µF – 0.2 µF
105	VDDHR_TX – power for HomePNA	0.1 µF – 0.2 µF
107	DVDDA_HR – ref voltage	0.1 µF – 0.2 µF
115	DVDD_TX – power for 10BASE-T	0.1 µF – 0.2 µF
119	DVDD_RX – power for 10BASE-T	0.1 µF – 0.2 µF
109	DVDDA_HR – power for HomePNA	0.1 µF – 0.2 µF
113	DVDDD – digital power	0.1 µF – 0.2 µF

Note: *For 144-pin design, refer to the power signals in Table 1.*

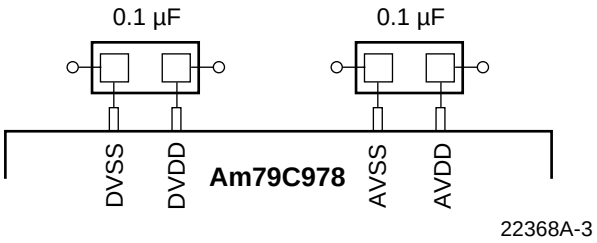


Figure 3. Recommended Bypass Capacitors

CRYSTAL OSCILLATOR

PCnet-Home devices include on-chip oscillator circuitry allowing the use of a 20 MHz external crystal attached to the XTAL1 and XTAL2 pins, and XCLK/$\overline{\text{XTAL}}$ pin tied LOW. Alternatively, a 60 MHz clock source can also be used to drive the XTAL1 pin, in which case the XTAL2 pin MUST be left unconnected and XCLK/$\overline{\text{XTAL}}$ tied HIGH. Table 2 shows the appropriate clock select and Figure 4 shows the clock interface.

Table 2. External Clock Source Selection

Clock Source	Clock Select Pin	Pin Name
20 MHz crystal	XCLK/$\overline{\text{XTAL}}$ LOW	XTAL1 and XTAL2
60 MHz osc.	XCLK/$\overline{\text{XTAL}}$ HIGH	XTAL1

When selecting a crystal for use in the PCnet-Home design, the crystal should meet the 50 ppm, 18 pF standard load capacitors (or 33 pF), and 0.005% tolerance at 20 MHz (see Table 3).

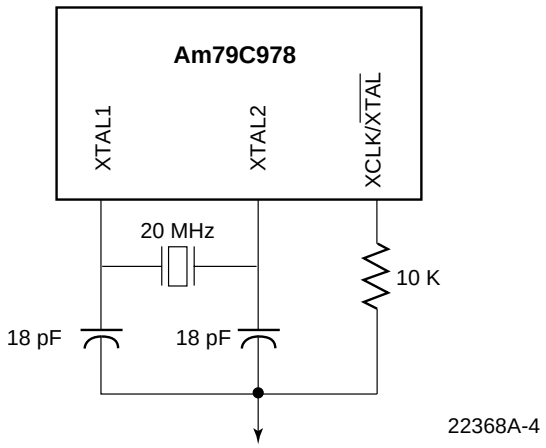


Figure 4. Crystal Clock Source

Two crystal suppliers are listed below:

- **Ecliptik Corporation -** www.ecliptik.com
- **Epson Corporation -** www.epson.com

External Crystal Characteristics

When using a crystal to drive the oscillator, the following crystal specification in Table 3 may be used to ensure less than ±0.5 ns jitter at DO±.

Table 3. Crystal Characteristics

Parameter	Min	Nom	Max	Units
1. Parallel Resonant Frequency		20		MHz
2. Resonant Frequency Error	-50		+50	ppm
3. Change in Resonant Frequency With Respect To Temperature (0°–70° C)*	-40		+40	ppm
4. Crystal Load Capacitance	15	18	33	pF
5. Motional Crystal Capacitance (C1)		0.022		pF
6. Internal Equivalent Series Resistance			50	ohm
7. Shunt Capacitance			7	pF

Note: **Requires trimming specification; not trimmed is 50 ppm total.*

EEPROM AND LED INTERFACES

PCnet-Home devices provide a 4-wire serial interface to standard EEPROMs, such as the 93C46 from Atmel Corporation and other vendors. The EEPROM device can operate from either a +3.3 V or a +5 V supply. The EEPROM is necessary to store unique board subvendor ID, as well as the IEEE address in order to obtain Microsoft's WHQL logo. Each adapter card manufacturer has the responsibility of ensuring that its card contains a unique 48-bit IEEE address assigned to the company by the IEEE. The assigned base address number is then programmed into the EEPROM.

In addition, the EEPROM provides manufacturer flexibility to change other home networking default settings, such as LED indication. The EEPROM signal interface itself is multiplexed with the LED signals. See Table 4.

Table 4. EEPROM and LED Interfaces

Pin Name	EEPROM I/F	LEDS
EECS	EECS	
EEDI/$\overline{\text{LED0}}$	EEDI	LED0
EESK/$\overline{\text{LED1}}$	EESK	LED1
EEDO/$\overline{\text{LED3}}$	EEDO	LED3
LED2	--	LED2
LED4	--	LED4

LED Indication

LED0 = default is active LOW to indicate LINK status.

LED1 = default is active LOW to indicate RECEIVE activity.

LED2 = default is active LOW to indicate SPEED.

LED3 = default is active LOW to indicate TRANSMIT activity.

LED4 = programmable to indicate various home network activity.

MAGNETIC INTERFACE

PCnet-Home devices include the internal 10BASE-T PHY for Ethernet and 1 Mbps home networking. If the internal 10BASE-T PHY is used, a 1.42:1 magnetic ratio is required. In addition, the voltage divider circuit is required to bias the received differential signal pair. The voltage bias network of 2K/1K should also have a bypass cap on that center 1.1 volt node to ground. See the attached schematic which has an improved Bit Error Rate (BER).

If the external 10/100 NetPHY-1LP device is used, a 1:1 magnetic ratio is required. Also, the appropriate signal termination is necessary for the unconnected 10BASE-T TX/RX signal pair. See *HomePNA Mode* section below.

According to the data sheets from the vendors below, the following surface mount magnetics should work in 1 Mbps HomePNA, 10BASE-T, and 100BASE-T/TX applications (see Table 5). Only a few part numbers for each vendor are listed for brevity, and most vendors offer a number of suitable devices. This is not meant to be a comprehensive list. Magnetics vendors change their product offering very frequently, so please contact the vendor directly before finalizing any design.

Note: *All magnetics listed below have bandpass filter and power surge protection built in.*

Table 5. Magnetics Vendors

Magnetics Vendor	Part No. of HomePNA-Only Magnetic	Part No. of 10BASE-T and HomePNA Integrated Magnetic	Part No. of 10/100 BASE-T/TX Ethernet and HomePNA Integrated Magnetic	Web URL
APC	APC76085	APC76160	APC76165	www.apcisdn.com
Belfuse	RS556-5000-05	RS556-5000-06	RS556-5000-07	www.belfuse.com
Halo	—	—	FGHR-S001NG1	www.haloelectronics.com
Midcom (Nanopulse)	7074-37	7084-30	7073-30	www.midcom-inc.com
PCA Electronics, Inc.	EPB5035G	EPB5036G	EPB5037G	www.pcainc.com
Pulse Engineering	B6003	B6006L	B6007	www.pulseeng.com
YCL	FH166911	FH166901	FH166916	www.ycl.com

HomePNA Only Mode (No 10BASE-T Port Connected)

If the internal 10BASE-T port is not utilized, appropriate 10BASE-T output signals (TX± and RX±) should be resistively terminated. See Figure 5 for more details. This termination helps to reduce the noise injected by the Ethernet link pulse back into the HomePNA analog section. In addition, only HomePNA magnetics should be used to prevent interference from the floating 10BASE-T magnetic section (if both 10BASE-T/HomePNA magnetics are used).

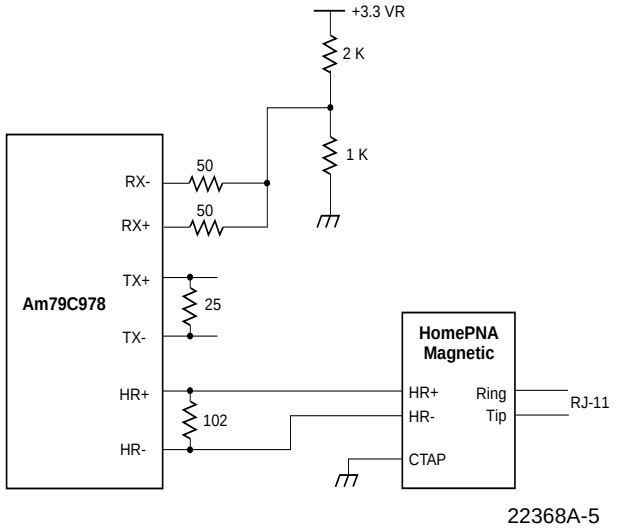


Figure 5. Recommended Termination for HomePNA Only Mode

PCB LAYOUT RECOMMENDATION

The following are some general guidelines that will ensure success of the PCnet-Home design:

- Component placement should be carefully considered in order to optimize and shorten the routing traces.
- Keep the bypass capacitors as close as possible to the power pins, and provide enough capacitors for the analog power pins. A good rule of thumb is to have a 0.1 µF capacitor for each analog power pin. See Table 1 for more details.
- Differential signal pairs from the chip side to the magnetic side, such as TX/RX for 10BASE-T, HRTRXP and HRTRXN for HomePNA, should be maintained identically (i.e., equal length and on the same side of the PCB to minimize impedance mismatch) between the routing pairs. A 10-15 mil trace thickness is recommended with an 8-10 mil space to maintain a 50-Ω impedance of the signal pair.
- Keep digital signals or other signals away from the differential signals that might introduce noise to the differential pairs.
- Keep the 20-MHz clock source away from the HomePNA differential output pair to prevent any coupling to the differential pair.
- Do not separate digital and analog ground planes if a 4-layer board is designed. Keep them the same to maintain the same current return path.

EMI and FCC

Since the PCnet-Home port utilizes the telephone or Ethernet cable, careful design techniques must be considered in order to ensure successful first-pass FCC requirements, Part 68 and Class B.

Note: *For Part 68, not all telecommunication requirements need to be tested since the PCnet-Home only transfers data and has no voice support like a modem. Consult with your FCC testing house for more details.*

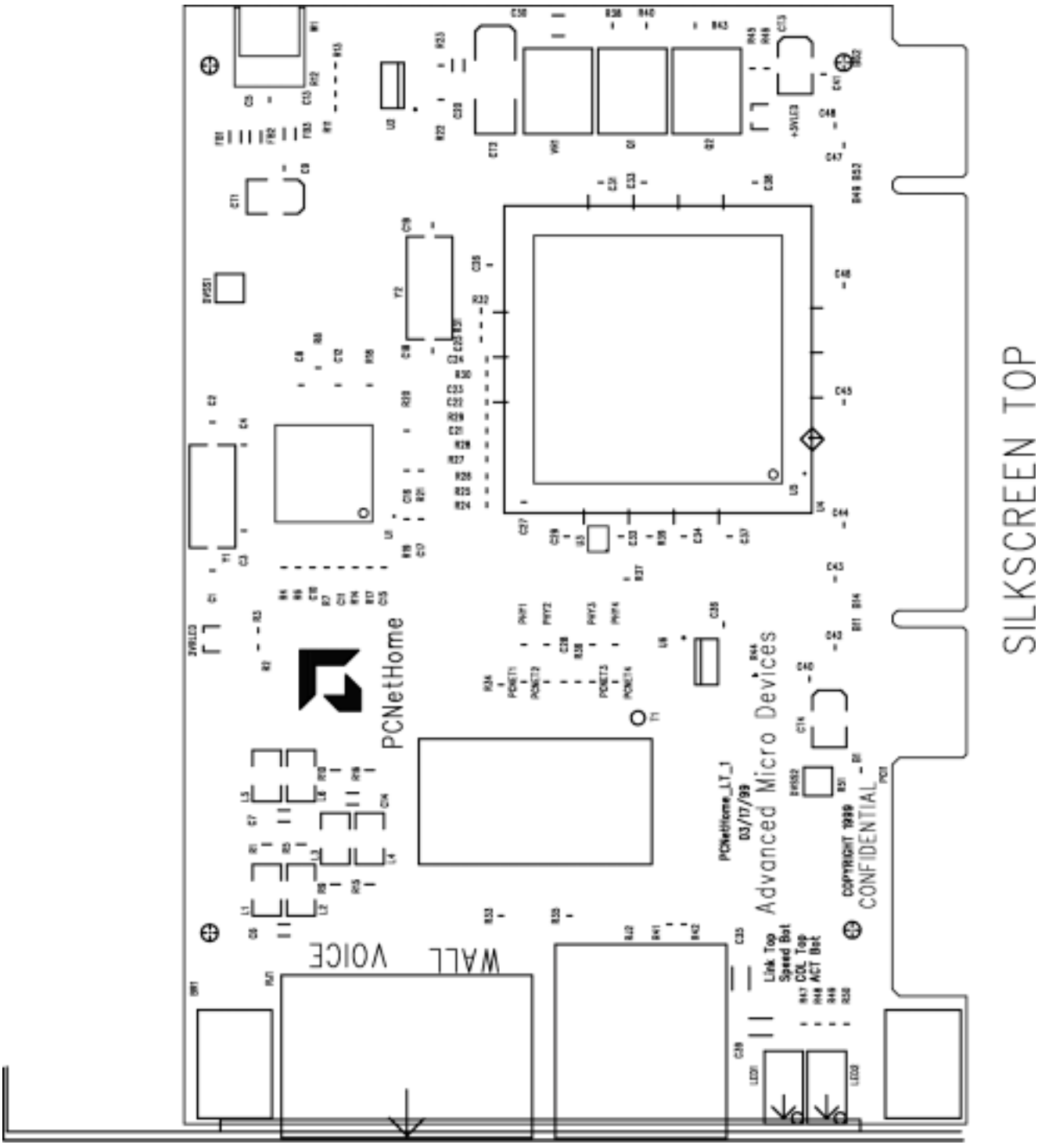
- When routing the HomePNA pair with magnetics close to the RJ-11 port, follow Part 68 requirements i.e., there should be no power plane around the area and all tip and ring traces must have enough clearance (at least 50 mils) to isolate potential power surges.
- Keep the AC ground return paths close to the signal paths. In AMD's design, there is the same ground, i.e., no separate analog or digital ground planes.
- Isolated planes, if any (i.e., +5 V to +3.3 V plane), should be avoided by capacitively coupling the planes together to prevent any discontinuities and provide a signal return path across the isolated planes. The cap used to tie the +3.3 V and +5 V planes together should be a good bypass cap (.01 µF or.1 µF), and it should be placed close to the center point of the signals that cross the boundary or on each side of the group.
- The chassis ground plane that is connected to the bracket should be isolated from the signal plane to prevent any radiation from leaking through and causing FCC failure.

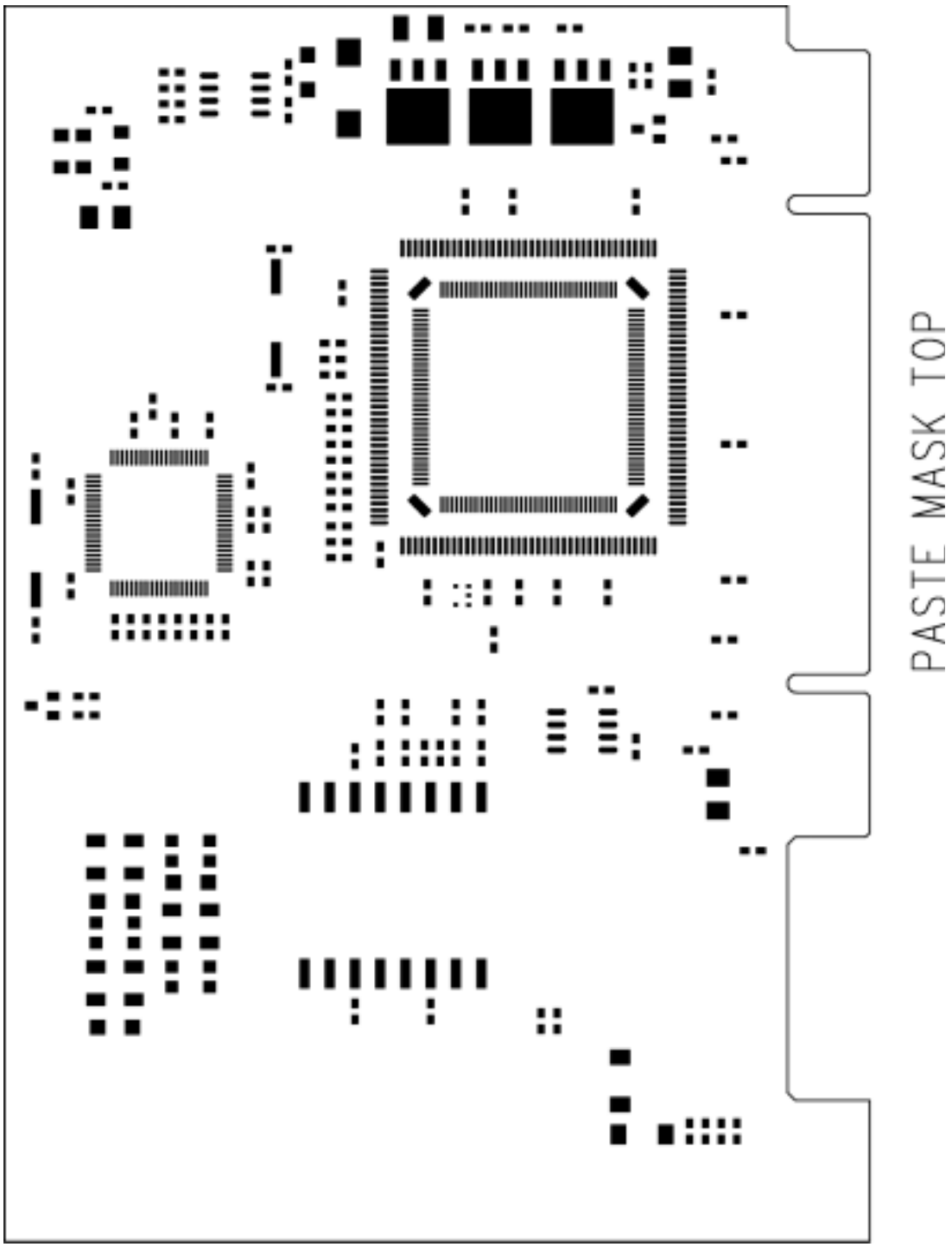
Additional information about PCB layout and how to reduce EMI may be found at: *http://www.amd.com/products/npd/techdocs/techdocs.html*.

CONCLUSION

Following the guidelines described in this document will help ensure that customers designing with PCnet-Home devices experience first-pass success. Contact your local AMD FAEs and SAEs for samples, schematics, and PCB layout reviews.

PCnet-Home PCB Design

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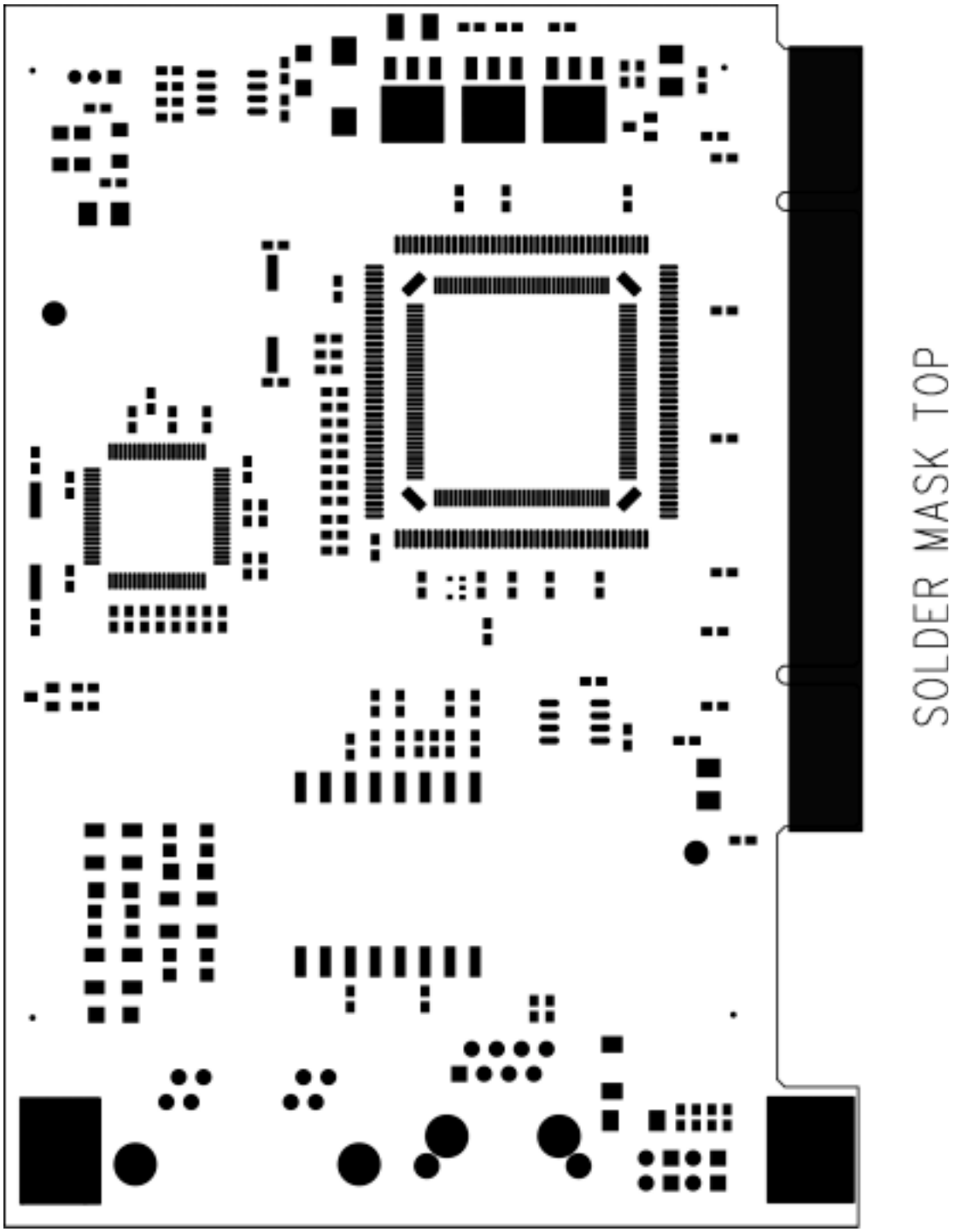
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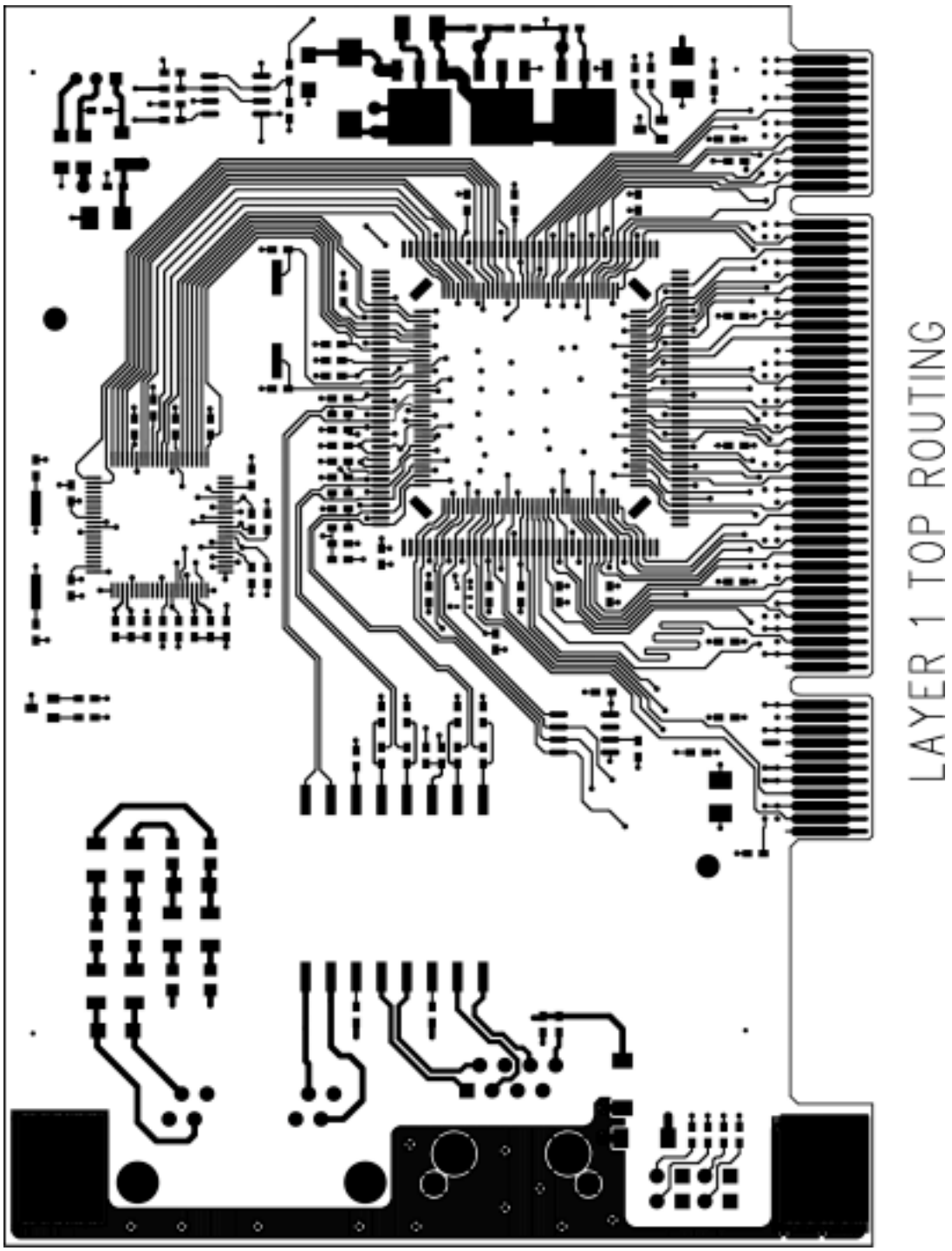
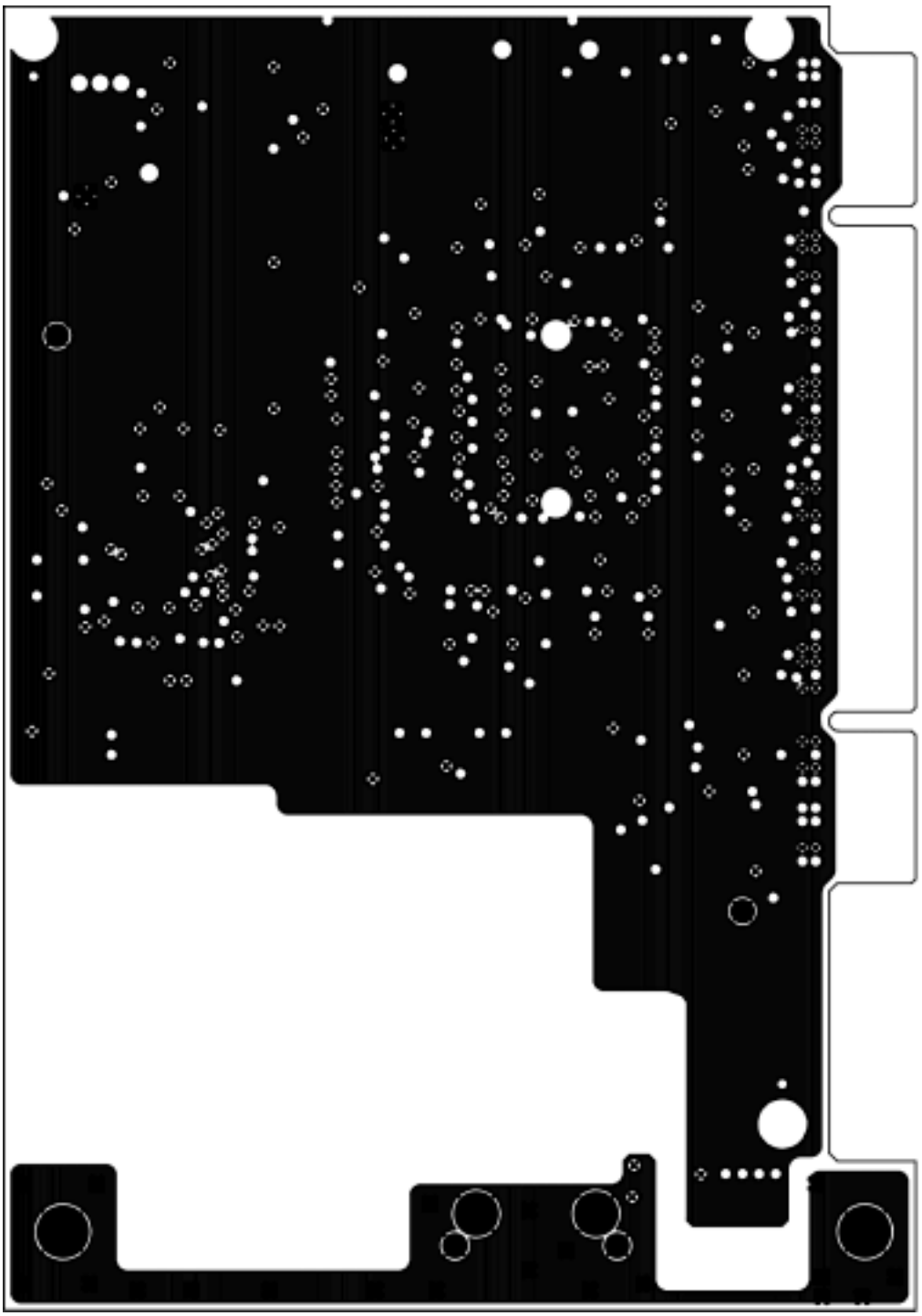
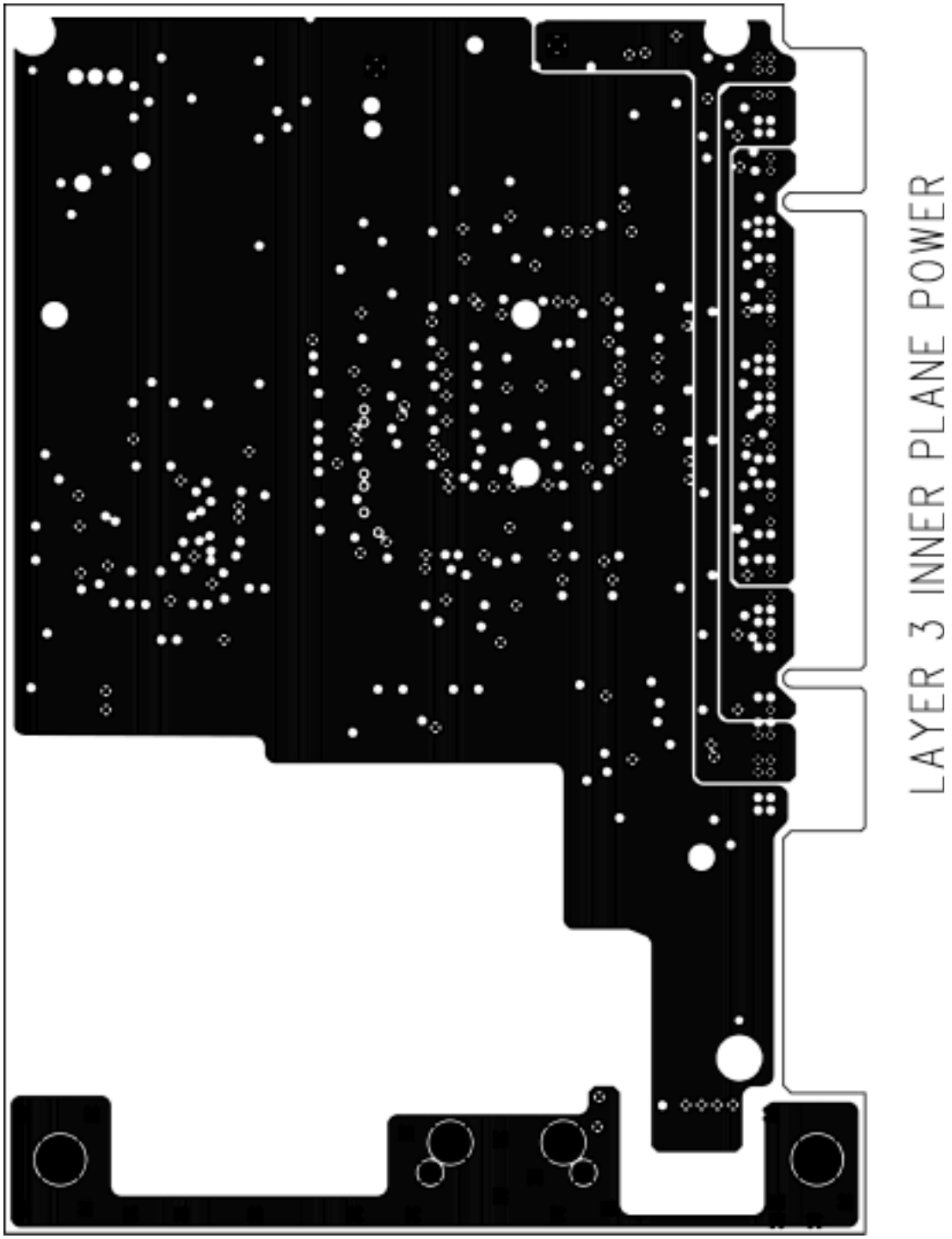

LAYER 1 TOP ROUTING



LAYER 2 INNER PLANE GROUND


LAYER 3 INNER PLANE POWER