PECL3 Series 3-Bit Programmable 10K ECL Delays

Electrical Specifications at 25°C

Part Number	Delay per Step (ns)	Output Delay (ns) per Program Setting (P3*P2*P1)								Max. Deviation ref. to 000 (ns)
		000	001	010	011	100	101	110	111	
PECL3-0.5	0.5 ± .25	3 ± .30	3.5	4	4.5	5	5.5	6	6.5	± .30
PECL3-1	1.0 ± .40	3 ± .30	4	5	6	7	8	9	10	± .50
PECL3-1.5	1.5 ± .50	3 ± .30	4.5	6	7.5	9	10.5	12	13.5	± .70
PECL3-2	2.0 ± .70	3 ± .30	5	7	9	11	13	15	17	± .80
PECL3-2.5	2.5 ± .70	3 ± .30	5.5	8	10.5	13	15.5	18	20.5	± .90
PECL3-3	3.0 ± .70	3 ± .30	6	9	12	15	18	21	24	± 1.0
PECL3-3.5	3.5 ± .80	3 ± .30	6.5	10	13.5	17	20.5	24	27.5	± 1.0
PECL3-4	4.0 ± .80	3 ± .30	7	11	15	19	23	27	31	± 1.0
PECL3-4.5	4.5 ± 1.0	3 ± .30	7.5	12	16.5	21	25.5	30	34.5	± 1.5
PECL3-5	5.0 ± 1.0	3 ± .30	8	13	18	23	28	33	38	± 1.5
PECL3-6	6.0 ± 1.0	3 ± .30	9	15	21	27	33	39	45	± 2.0
PECL3-7	7.0 ± 1.0	3 ± .30	10	17	24	31	38	45	52	± 2.0
PECL3-8	8.0 ± 1.0	3 ± .30	11	19	27	35	43	51	59	± 2.5
PECL3-9	9.0 ± 1.2	3 ± .30	12	21	30	39	48	57	66	± 2.5
PECL3-10	10.0 ± 1.5	3 ± .30	13	23	33	43	53	63	73	± 3.0

GENERAL: For Operating Specifications and Test Conditions, see Tables IV and VIII on page 7 of this catalog. Delays specified for the Leading Edge.

Minimum Input Pulse Width ..... 35% max. Delay
Temperature Coefficient ..... ≤300 ppm/°C
Supply Current, I_{EE} ..... 75 mA typ., 85 mA max.

3PECLH Series 3-Bit Programmable 10KH ECL Delays

Electrical Specifications at 25°C

Part Number	Delay per Step (ns)	Output Delay (ns) per Program Setting (P3*P2*P1)								Max. Deviation ref. to 000 (ns)
		000	001	010	011	100	101	110	111	
3PECLH-0.5	0.5 ± .25	1.5 ± .50	2.0	2.5	3.0	3.5	4.0	4.5	5.0	± .30
3PECLH-1	1.0 ± .40	1.5 ± .50	2.5	3.5	4.5	5.5	6.5	7.5	8.5	± .50
3PECLH-1.5	1.5 ± .50	1.5 ± .50	3.0	4.5	6.0	7.5	9.0	10.5	12.0	± .70
3PECLH-2	2.0 ± .70	1.5 ± .50	3.5	5.5	7.5	9.5	11.5	13.5	15.5	± .80
3PECLH-2.5	2.5 ± .70	1.5 ± .50	4.0	6.5	9.0	11.5	14.0	16.5	19.0	± .90
3PECLH-3	3.0 ± .70	1.5 ± .50	4.5	7.5	10.5	13.5	16.5	19.5	22.5	± 1.0
3PECLH-3.5	3.5 ± .80	1.5 ± .50	5.0	8.5	12.0	15.5	19.0	22.5	26.0	± 1.0
3PECLH-4	4.0 ± .80	1.5 ± .50	5.5	9.5	13.5	17.5	21.5	25.5	29.5	± 1.0
3PECLH-4.5	4.5 ± 1.0	1.5 ± .50	6.0	10.5	15.0	19.5	24.0	28.5	33.0	± 1.5
3PECLH-5	5.0 ± 1.0	1.5 ± .50	6.5	11.5	16.5	21.5	26.5	31.5	36.5	± 1.5
3PECLH-6	6.0 ± 1.0	1.5 ± .50	7.5	13.5	19.5	25.5	31.5	37.5	43.5	± 2.0
3PECLH-7	7.0 ± 1.0	1.5 ± .50	8.5	15.5	22.5	29.5	36.5	43.5	50.5	± 2.0
3PECLH-8	8.0 ± 1.0	1.5 ± .50	9.5	17.5	25.5	33.5	41.5	49.5	57.5	± 2.5
3PECLH-9	9.0 ± 1.2	1.5 ± .50	10.5	19.5	28.5	37.5	46.5	55.5	64.5	± 2.5
3PECLH-10	10.0 ± 1.5	1.5 ± .50	11.5	21.5	31.5	41.5	51.5	61.5	71.5	± 3.0

GENERAL: For Operating Specifications and Test Conditions, see Tables V and VIII on page 7 of this catalog. Delays specified for the Leading Edge.

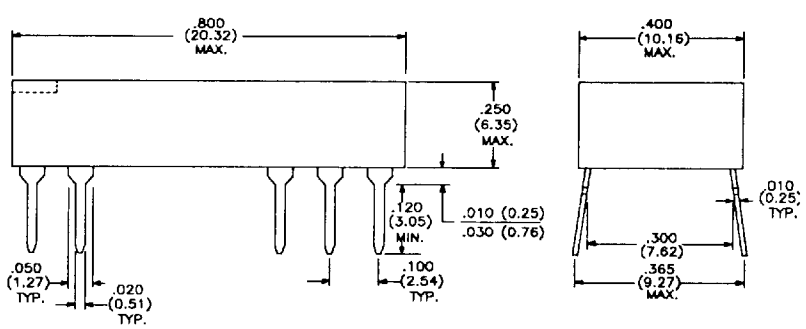
Minimum Input Pulse Width ..... 35% max. Delay
Temperature Coefficient ..... ≤300 ppm/°C
Supply Current, I_{EE} ..... 75 mA typ., 85 mA max.

CUMULATIVE TOLERANCES: Maximum Deviation Tolerances for Programmed Delays Referenced to Initial Delay, Setting "000." Tables display values of delay with respect to input, whose tolerance is the cumulative error of the initial delay (± 1.0) and the Maximum Deviation. For example, the setting "111" delay of PECL3-10 is 70.0 ± 3.0 ref. to "000," and 73.0 ± 4.0 ref. to the input.

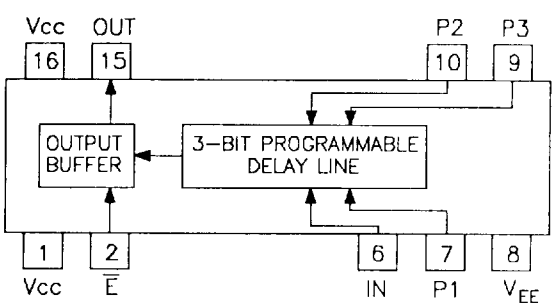
INPUT LOADING: Input, Pin 6, internally connected to eight 10K inputs terminated by Thevenin equivalent of 100 Ohms to -2V.

ENABLE: Enable input (Pin 2) is active low. Output will be disabled (remain low) when the Enable is high.

PHYSICAL DIMENSIONS inches (mm)



SCHEMATIC DIAGRAM



VARIATIONS AVAILABLE. FOR INTERMEDIATE VALUES AND/OR CUSTOM DESIGNS PLEASE CONSULT THE FACTORY.

Specifications subject to change without notice.

PECL 3-7/93

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