M64893AGP

SERIAL INPUT PLL FREQUENCY SYNTHES IZER FOR TV/VCR

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Description

The M64093FP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using Bi-CMOS process. It contains prescaler with operating up to. 1.0 GHz, 4 band driver and a tuning amplifier for direct tuning.

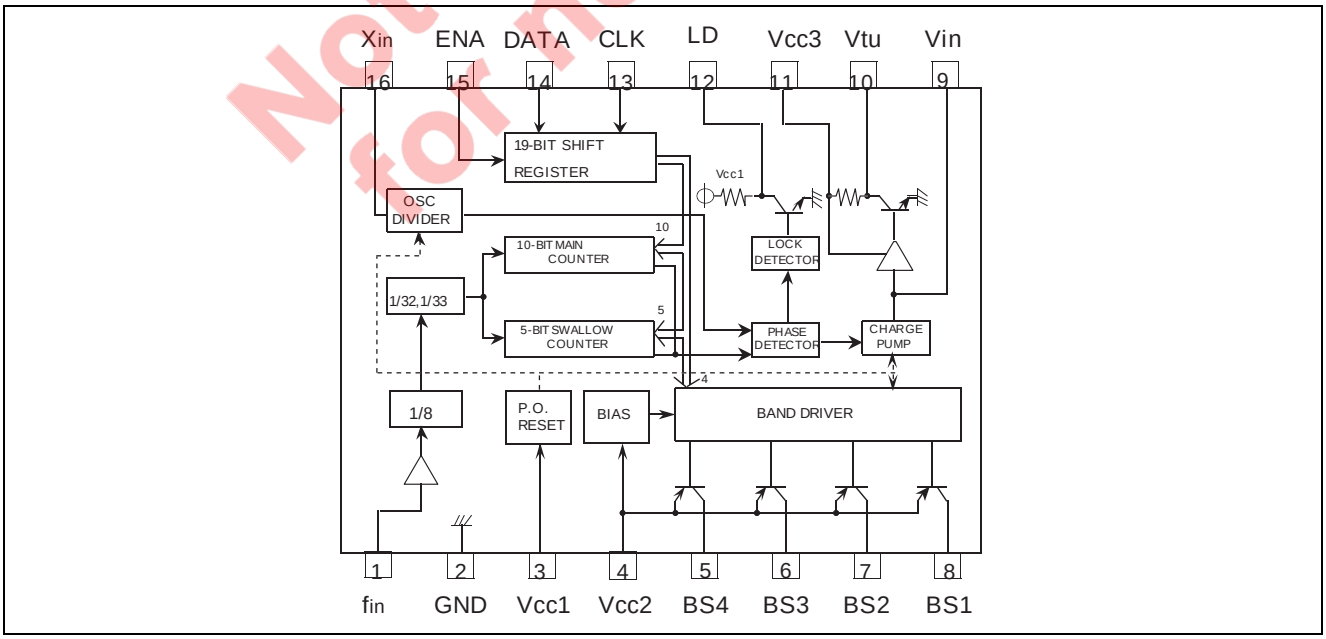
Features

- 4 integrated PNP band switching drivers (lo = 40 mA, Vsat = 0.2 V typ@Vcc1 to 13.2 V)
- Built-in tuning amplifier for direct tuning (33 V)
- Low power dissipation (lcc = 24 mA, at Vcc = 5 V)
- Built-in prescaler with input amplifier (Fmax = 1.0 GHz)
- PLL lock/unlock status display output (built-in pull-up resistor)
- Reference driver (Division radio 1/640)
- Serial data input (3 wire Bus)
- Built-in power on reset
- 16pin –plastic mold mini flat package (16pin SSOP)
- Without protection diode at CLK,DATA,ENA

Application

- TV,VCR tuners

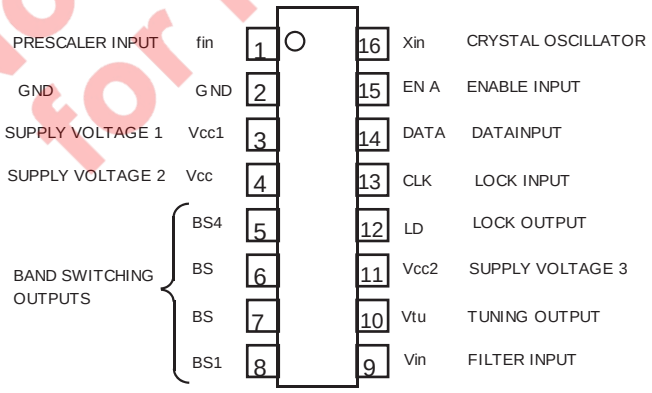
Block Diagram



Pin Description

Symbol	Pin No.	Pin name	Function
fin	1	Prescaler input	Input for the VCO frequency.
GND	2	GND	Ground to 0 V
Vcc1	3	Power supply voltage 1	Power supply voltage terminal. 5.0 V+/-0.5 V
Vcc2	4	Power supply voltage 2	Power supply voltage terminal. Vcc1 to 13.2 V
BS4	5	Band switching outputs	PNP open collector method is used.
BS3	6		When the band switching data is “H”, the output is “ON”.
BS2	7		When it is “L”, the output is “OFF”.
BS1	8		
Vin	9	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f1/N) is lead compared to the reference frequency (fref), the “source” current state becomes active. If it is lag, the same, the high impedance state be comes active.
Vtu	10	Tuning output	This supplies the tuning voltage.
Vcc3	11	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35 V
LD	12	Lock detect output	When 19 bit data is input, lock detector is output. When 27 bit data is input, lock detector is output. the programmable divider output and reference divider output is selected by the test mode.
CLOCK	13	Clock input	Data is read into the shift register when the clock signal falls.
DATA	14	Data input	Input for band SW and programmable freg. divider set falls.
ENABLE	15	Enable input	This is normally at an “L”. When this is at “H”, data and clock signals are received. Data is read into the latch when the 19th pulse of the clock signal falls.
X in	16	This is connected to the Crystal oscillator.	4.0MHz crystal oscillator connected.

Pin Arrangement



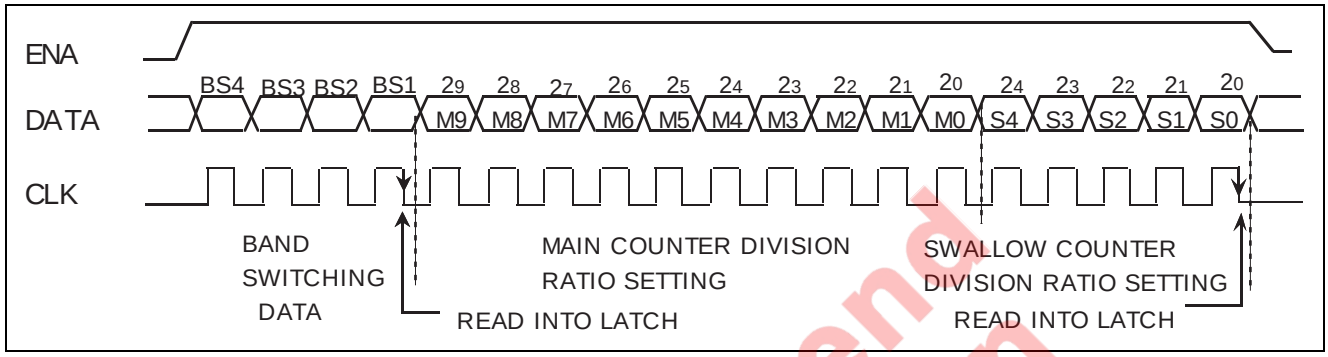
OUTLINE 16P2Z

Method of Setting Data

The programmable divider uses 15bits Setting up the band switching output uses 4bits.

The test mode data use s 8bits. The total bits used is 27bits. Data is read in when the enable signal is “H” and the clock signal falls.

The band switching data is read in the 4th pulse of the clock signal. The programmable driver data is read into the fall of the 19th pulse of the clock signal .When the enable signal goes to “L” Before the 19th pulse of the enable signal, only the band switching data is updated and other data is ignored.



How to Set The Dividing Radio of The Programmable Divider

Total division N is given by the following from formulas in addition to the prescaler used the previous stage.

$N = 8*(32 M+S)$ M: 10 bit main counter division

S: 5 bit swallow counter division

The M and S counters are binary the possible ranges of division are follows.

$32 \leq M \leq 1023$

$0 \leq S \leq 31$

Therefore, the rage of division N is 8,192 to 262, 136.
The tuning frequency fvco is given in the following equations.

$fvco = fref*N$

$= 6.25*8*(32M+S)$

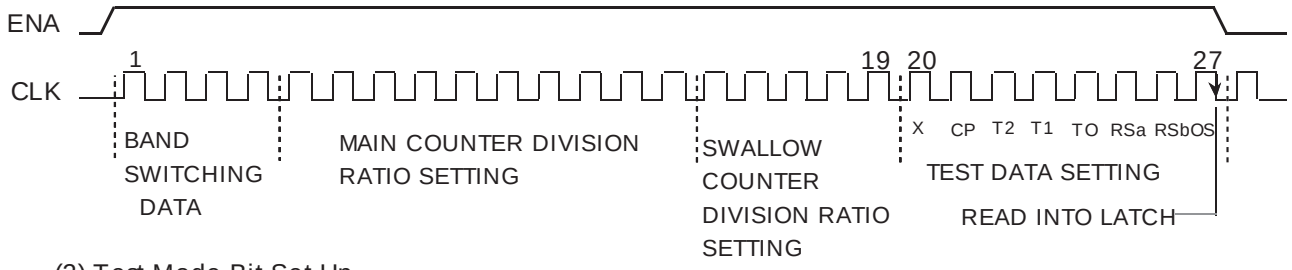
$= 50.0*8*(32M+S)$ [KHz]

Therefore, the tuning frequency range is from 51.2 MHz to 1000 MHz

Test Mode Data Set Up Method

The data for the test mode uses from 20 to 27 bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27 bit data



(2) Test Mode Bit Set Up

X :Random, 0 or 1.normal "0"
CP :Set up the charge pump current value
T0, T1,&T2 :Set up test modes
RSa, Rsa :Set the frequency division of the reference frequency
OS :Set up the tuning amplifier

Setting Up the Charge Pump Current of The Phase Comparator

CP	Charge pump current	Mode
0	50 µA	Normal
1	250 µA	Test

Setting Up The Test Mode

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Test
0	1	X	High impedance	LD	Test
1	1	0	Sink	LD	Test
1	1	1	Source	LD	Test
1	0	0	High impedance	fref	Test
1	0	1	High impedance	f1/N	Test

Set Up for The Reference Frequency Division Radio

RSa	RSb	Division radio
0	1	1/512
1	1	1/1024
X	0	1/640

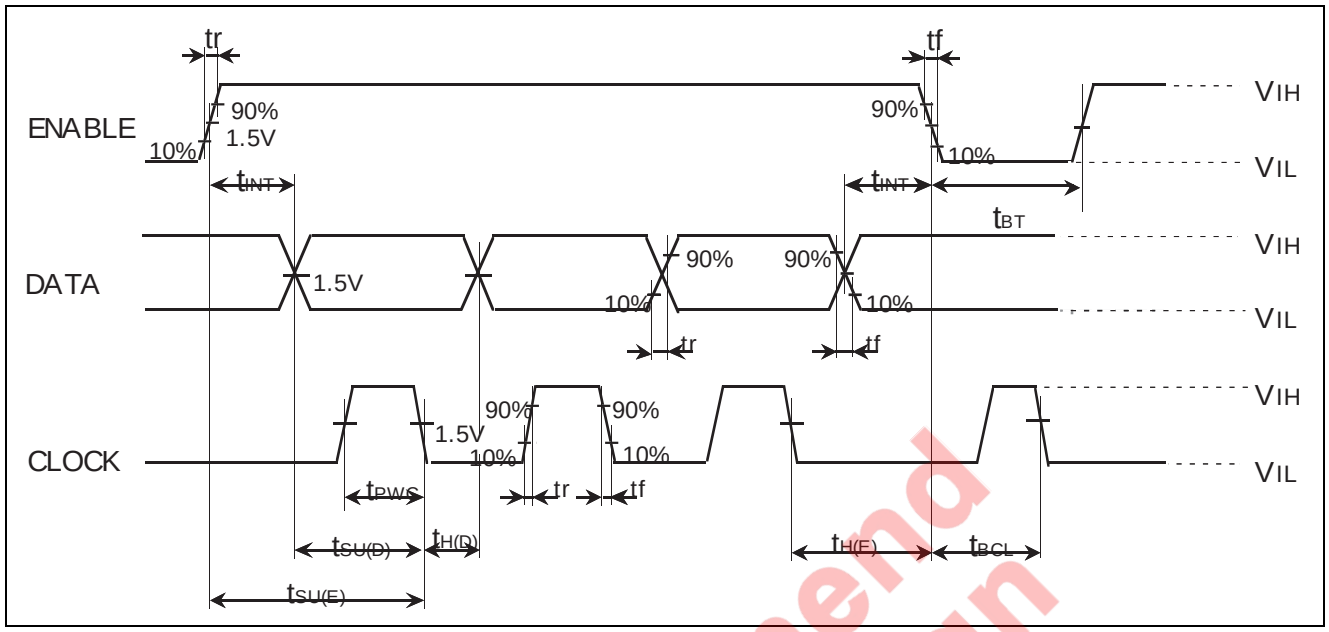
Set Up The Tuning Amplifier

OS	Tuning voltage output	mode
0	ON	Normal
1	OFF	Test

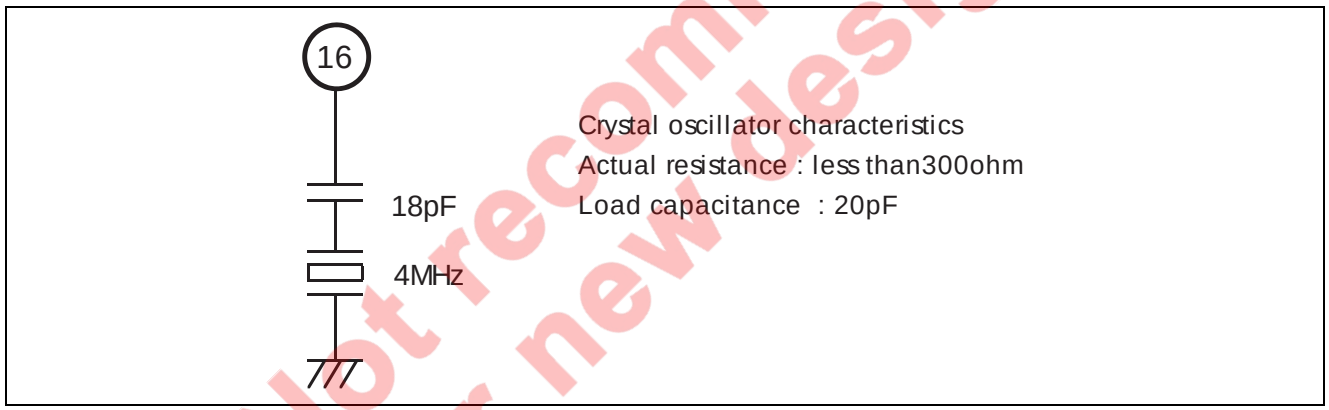
Power On Reset Operation (Initial State The Power is Turned ON)

- BS4 to BS1 :OFF
- Charge pump :high impedance
- Tuning amplifier :OFF
- Charge pump current :250 μA
- Frequency division radio :1/640
- Lock output :H

Timing Diagram



Crystal Oscillator Connection Diagram



Absolute Maximum Ratings

(Ta = –20°C to 75°C unless otherwise noted)

Parameter	Symbols	Max.ratings	Units	Conditions
Standby voltage1	Vcc1	6.0	V	Pin3
Standby voltage2	Vcc2	14.4	V	Pin4
Standby voltage3	Vcc3	36.0	V	Pin11
Input voltage	VI	6.0	V	Not to exceed Vcc1
Output voltage	V_{BSOFF}	6.0	V	Pin 12
Voltage applied when the band output current is OFF	I_{BSON}	14.4	V	
Band output current	t_{BSON}	50.0	mA	Per 1 band output circuit
ON the time when the band output is ON	Pd	10	sec	50 mA per 1 band output circuit 3 cicuits are pn at same time
Power dissipation	Topr	350	mW	Ta = 75°C
Operating temperature	Tstg	–20 to +75	°C	
Storage temperature	Tstg	–40 to +125	°C	

Recommended Operating Conditions

(Ta = –20°C to 75°Cunless otherwise noted)

Parameter	Symbols	Ratings	Units	Conditions
	Vcc1	4.5 to 5.5	V	
Standby voltage1	Vcc2	5.0 to 3.2	V	
Standby voltage2	Vcc3	30 to 35	V	
Standby voltage3	fopr2	4.0	MHz	Crystal oscillation circuit
Operating frequency(1)	fopr2	80 to 100	MHz	
Operating frequency(2) Band output current 5 to 8	I_{BDL}	0 to 40	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

Electrical Characteristics

(Ta = –20°C to 75°Cunless otherwise noted)Vcc1 = 5.0 V, Vcc = 12 V, Vcc3 s= 33 V

Parameters	Symbol	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
input terminals							
“H” input voltage	V_{IH}	13 to 15		3.0	—	Vcc1+0.3	V
“L” input voltage	V_{IL}	13 to 15		—	—	1.5	V
“H” input voltage	I_{IH}	13 to 15	Vcc1 = 5.5 V, Vi = 4.0 V	—	—	10	µA
“L” input current	I_{IL}	13 to 15	Vcc1 = 5.5 V, Vi = 0.4 V	—	–2	–10–	µA
Lock output							
“H” output voltage	V_{OH}	12	Vcc1 = 5.5 V	5.0	—	—	V
“L” output voltage	V_{OL}	12	Vcc1 = 5.5 V	—	0.3	0.5	V
Band SW							
output voltage	V_{BS}	5 to 8	Vcc2 = 12 V Io = -40 mA	11.6	11.8	—	V
Leak current	$I_{OIK}1$	5 to 8	Vcc2 = 12 V Band SW is OFF	—	—	1	µA
Tuning output			Vcc3 = 33 V				
output voltage “H”	V to H	10	Vcc3 = 33 V	32.5	—	—	V
output voltage “L”	V to L	10		—	0.2	0.4	V
Charge pump			Vcc1 = 5.0 V Vo = 1 V				
“H” output current	I_{OH}	9	Vcc1 = 5.0 V Vo = 1 V	—	±250	±470	µA
“L” output current	I_{OL}	9	Vcc1 = 5.0 V Vo = 2.5 V	—	±50	±130	µA
Leak current	I_{cpLK}	9		—	—	±50	nA
Supply current 1	I_{CC1}		Vcc1 = 5.5 V	—	24	31	mA
Supply current 2							
4circuits OFF	I_{CC2A}	4	Vcc2 = 12 V	—	—	0.5	mA
1 circuits ON,							
Output open	I_{CC2B}	4	Vcc2 = 12 V	—	5.0	6.0	mA
Output current 40mA	I_{CC2C}	4	Vcc2 = 12 V Io = –40 mA	—	45.0	46.0	mA
Supply current 3	I_{CC3C}	11	Vcc3 = 33 V Output ON	—	3.6	4.5	mA

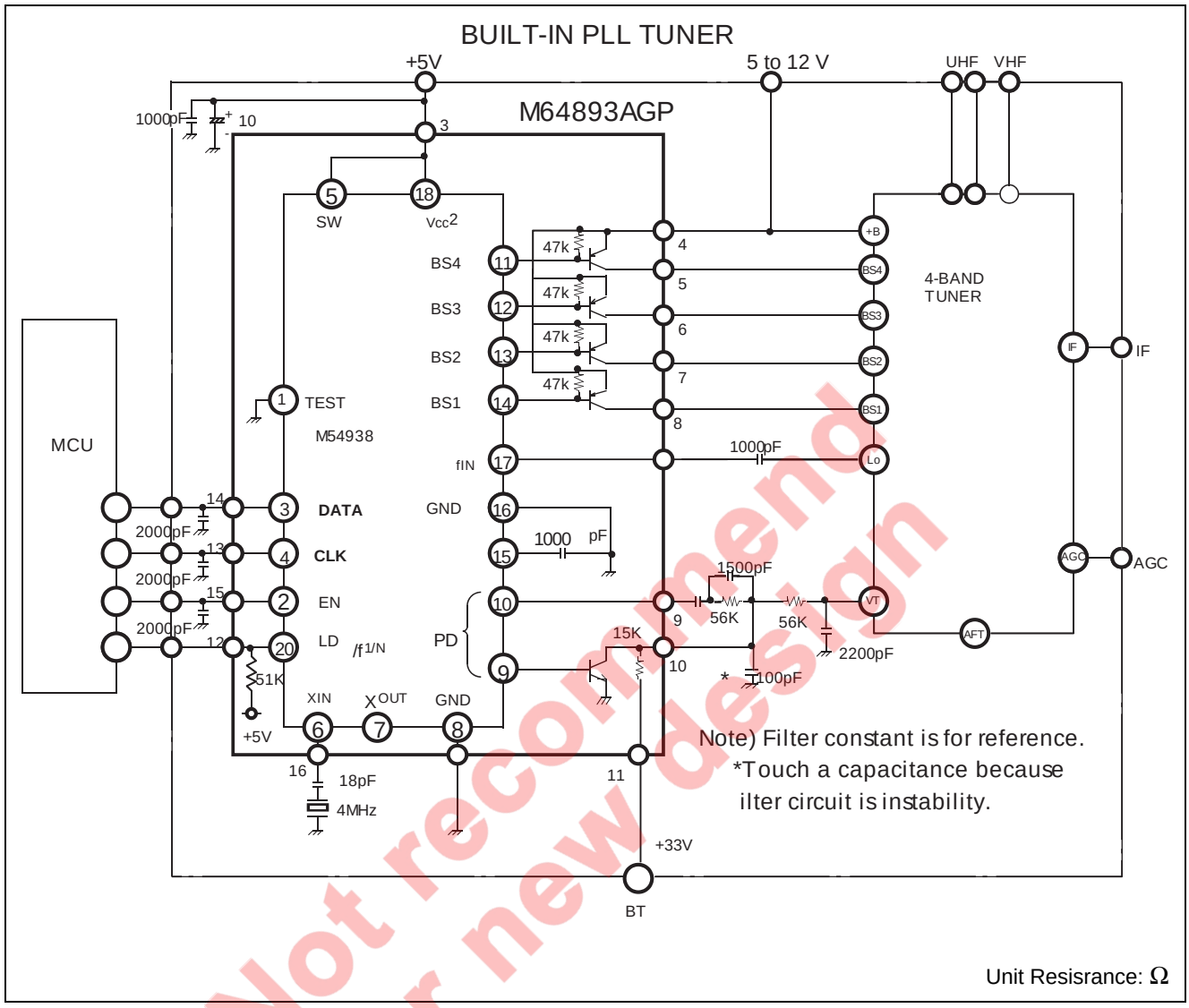
Note: The typical values are at Vcc1 = 5.0 V, Vcc2 = 12 V, Vcc3 = 33 V, Ta = 25°C

Switching Characteristics

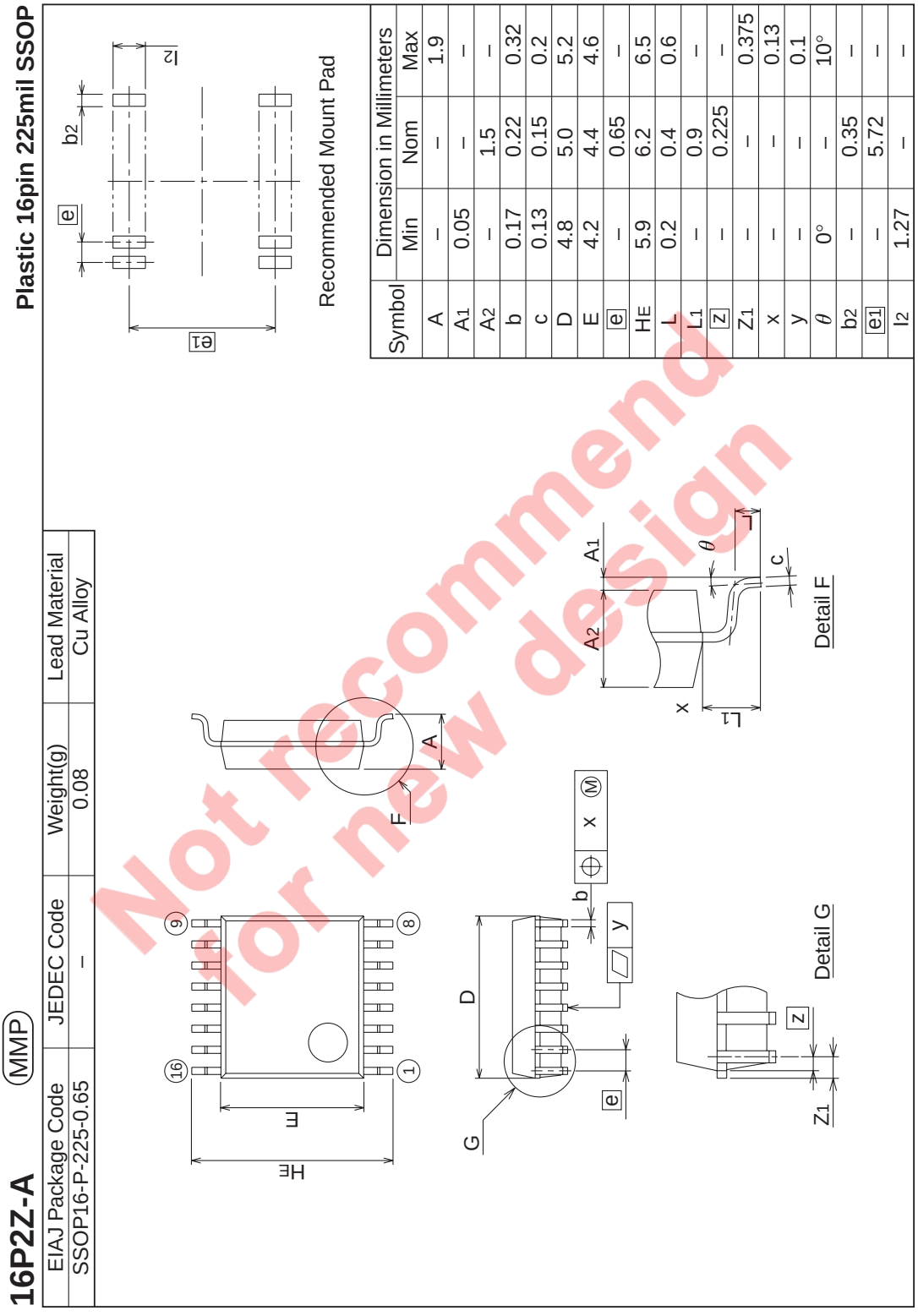
(Ta = –20°C to 75°C, Vcc1 = 5.0 V, Vcc = 12 V, Vcc3 = 33 V, unless otherwise noted)

Parameter	Symbol	Test pin	Test conditions	Limits			Unit used
				Min	Min	Max	
Prescaler operating frequency	fopr	1	Vcc1 = 4.5 to 5.5 V	80		1000	MHz
		1	Vin = Vinmin to Vinmax				
Operating input voltage	Vin	13	Vcc = 4.5 to 5.5 V				dBm
			80 to 100 MHz	–24	—	4	
			100 to 200 MHz	–27	—	4	
			200 to 800 MHz	–30	—	4	
			800 to 1000 MHz	–27	—	4	
			1000 to 1300 MHz	–24	—	4	
Clock pulse width	t PWC	14	Vcc1 = 4.5 to 5.5 V	1	—	—	µs
Data setup time	t SU(D)	14	Vcc1 = 4.5 to 5.5 V	2	—	—	µs
Data hold time	t H(D)	15	Vcc1 = 4.5 to 5.5 V	1	—	—	µs
Enable setup time	t SU(E)	15	Vcc1 = 4.5 to 5.5 V	3	—	—	µs
Enable hold time	t H(E)	15,14	Vcc1 = 4.5 to 5.5 V	3	—	—	µs
Enable data interval time	t INT	13,14,15	Vcc1 = 4.5 to 5.5 V	1	—	—	µs
Rise time	tr	13,14,15	Vcc1 = 4.5 to 5.5 V	—	—	1	µs
Fall time	tf	15	Vcc1 = 4.5 to 5.5 V	—	—	1	µs
Next enable prohibit time	tbt	13.15	Vcc1 = 4.5 to 5.5 V	5	—	—	µs
Next clock prohibit time	tbcl		Vcc1 = 4.5 to 5.5 V	5	—	—	µs

Application Example



Package Dimensions



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.9
A_1	0.05	–	–
A_2	–	1.5	–
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	4.8	5.0	5.2
E	4.2	4.4	4.6
e	–	0.65	–
H_E	5.9	6.2	6.5
L	0.2	0.4	0.6
L_1	–	0.9	–
Z	–	0.225	–
Z_1	–	–	0.375
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.35	–
e_1	–	5.72	–
l_2	1.27	–	–

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