CY7C432
CY7C433

CYPRESS SEMICONDUCTOR

Cascadable 4K x 9 FIFO

Features

- 4096 x 9 FIFO buffer memory
- Dual-port RAM cell
- Asynchronous read/write
- High-speed 28.5-MHz read/write independent of depth/width
- 25-ns access time
- Low operating power
  - I_{CC} (max.) = 142 mA commercial
  - I_{CC} (max.) = 155 mA military
- Half Full flag in standalone
- Empty and Full flags
- Expandable in width and depth
- Retransmit in standalone
- Parallel cascade minimizes bubble-through
- 5V ± 10% supply
- 300-mil DIP packaging
- 300-mil SOJ packaging
- TTL compatible
- Three-state outputs
- Pin compatible and functionally equivalent to IDT7204

Functional Description

The CY7C432 and CY7C433 are first-in first-out (FIFO) memories offered in 600-mil-wide and 300-mil-wide packages, respectively. They are 4096 words by 9 bits wide. Each FIFO memory is organized so that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

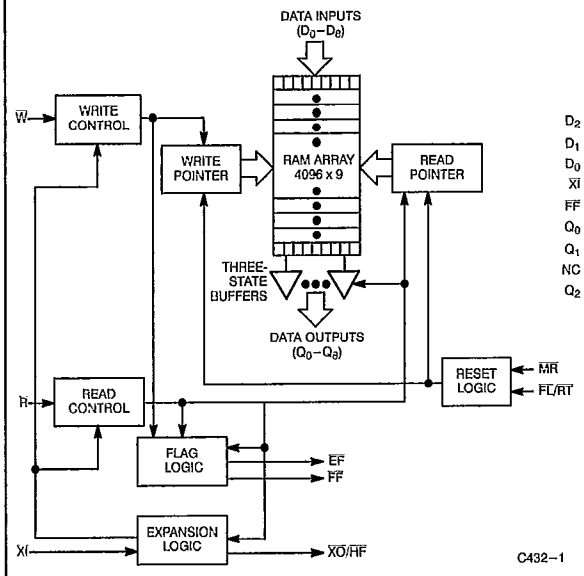
The read and write operations may be asynchronous; each can occur at a rate of 28.5 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFOs to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

The CY7C432 and CY7C433 are fabricated using advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

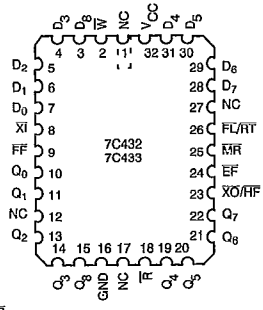
Logic Block Diagram



C432–1

Pin Configurations

PLCC/LCC
Top View



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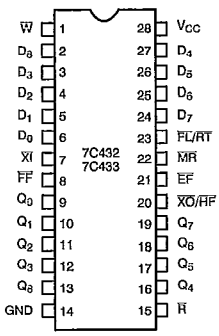
DIP
Top View



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CYPRESS SEMICONDUCTOR

Selection Guide

		7C432–25 7C433–25	7C432–30 7C433–30	7C432–40 7C433–40	7C432–65 7C433–65
Frequency (MHz)		28.5	25	20	12.5
Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	142	135	125	110
	Military/Industrial		155	145	130

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Power Dissipation 0.88W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	– 40°C to +85°C	5V ± 10%
Military[1]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C432–25 7C433–25 Min.	7C432–25 7C433–25 Max.	7C432–30 7C433–30 Min.	7C432–30 7C433–30 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.0 mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind			2.2	V_{CC}	
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	– 10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		– 10	+10	– 10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		140		135	mA
			Mil/Ind[4]				155	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil/Ind				30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} – 0.2V	Com'l		20		20	mA
			Mil/Ind				25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			–90		–90	mA

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 110 mA + [($\bar{f}$ – 12.5) • 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
4. I_{CC} (military) = 130 mA + [($\bar{f}$ – 12.5) • 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

5 FIFOs

Electrical Characteristics Over the Operating Range[2] (continued)

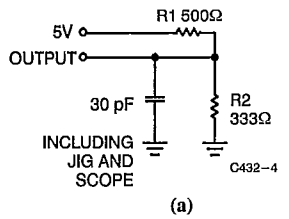
Parameter	Description	Test Conditions		77C432-40 77C433-40 Min.	77C432-40 77C433-40 Max.	77C432-65 77C433-65 Min.	77C432-65 77C433-65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2mA		2.4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.0	V_{CC}	2.0	V_{CC}	V
			Mil/Ind	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{R} \ge V_{IH}$, $GND \le V_O \le V_{CC}$		−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		125		110	mA
			Mil/Ind[4]		145		130	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		25		25	mA
			Mil/Ind		30		30	
I_{SB2}	Power-Down Current	All Inputs ≥ V_{CC} − 0.2V	Com'l		20		20	mA
			Mil/Ind		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			−90		−90	mA

Capacitance[6]

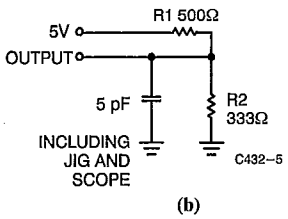
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Note:
6. Tested initially and after any design or process changes that may affect these parameters.

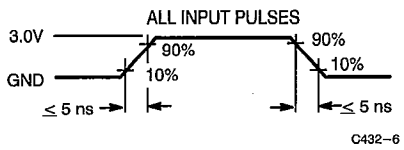
AC Test Loads and Waveforms



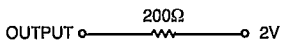
(a)



(b)



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[7,8]

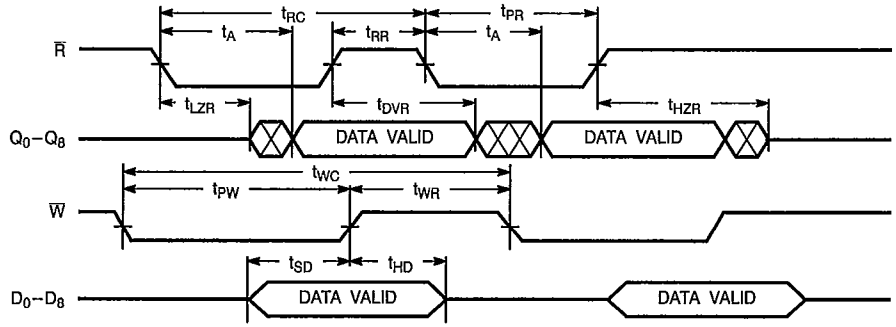
Parameter	Description	7C432–25 7C433–25		7C432–30 7C433–30		7C432–40 7C433–40		7C432–65 7C433–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_A	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[9]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[9,10]	Read HIGH to Data Valid	3		3		3		3		ns
t_{HZR}[9,10]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[9]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RTC}	Retransmit Cycle Time	35		40		50		80		ns
t_{PRT}	Retransmit Pulse Width	25		30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		35		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		30		35		60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW		35		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{EF}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{FF}$ HIGH	25		30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		25		30		40		65	ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance, as in part (a) of AC Test Loads, unless otherwise specified.
8. See the last page of this specification for Group A subgroup testing information.
9. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
10. t_{HZR} and t_{DVR} use capacitance loading as in part (a) of AC Test Loads.

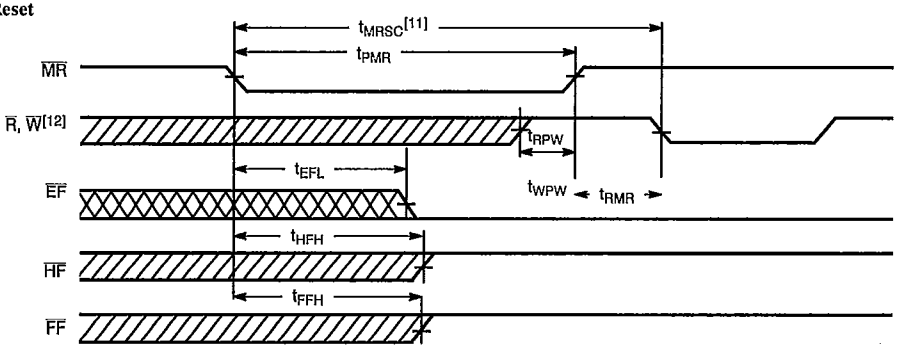
Switching Waveforms

Asynchronous Read and Write



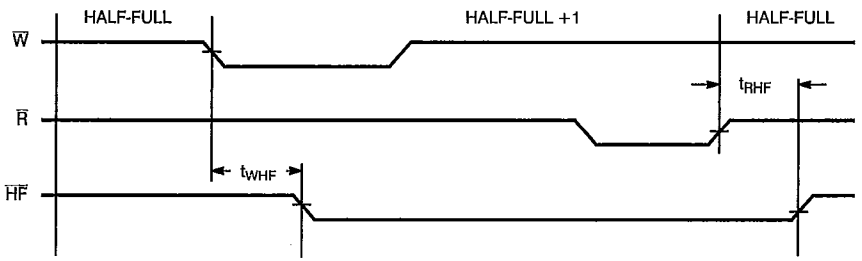
C432–7

Master Reset



C432–8

Half-Full Flag

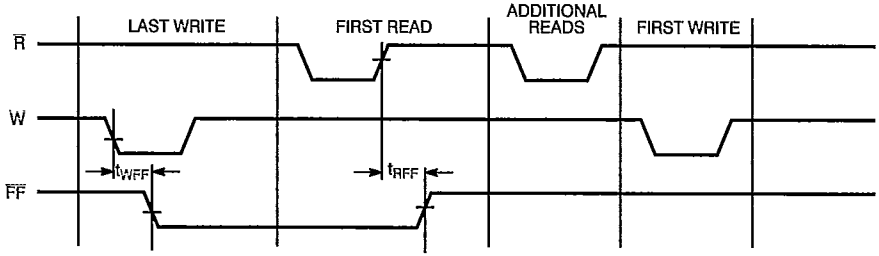


C432–9

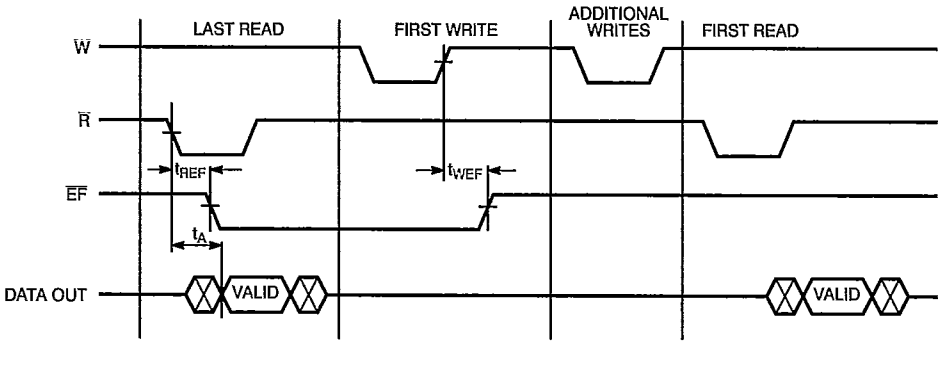
Notes:
11. $t_{MRSC} = t_{PMR} + t_{RMR}$.
12. $\overline{W}$ and $\overline{R} \geq V_{IH}$ for at least t_{WPW} or t_{RPR} before the rising edge of $\overline{MR}$.

Switching Waveforms (continued)

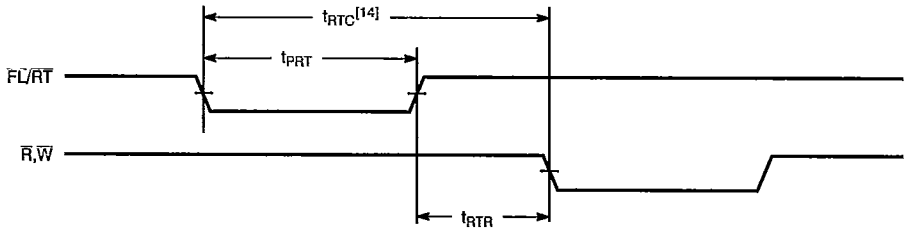
Last Write to First Read Full Flag



Last Read to First Write Empty Flag



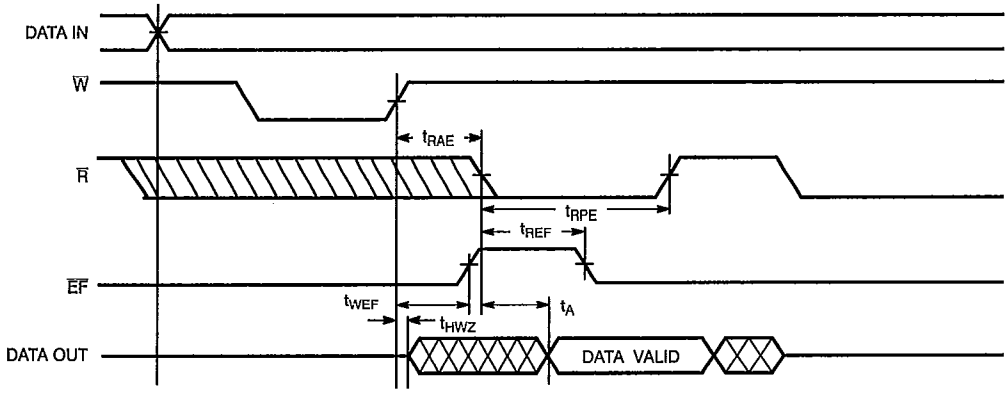
Retransmit[13]



Notes:
13. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.
14. $t_{RTC} = t_{PRT} + t_{RTR}$.

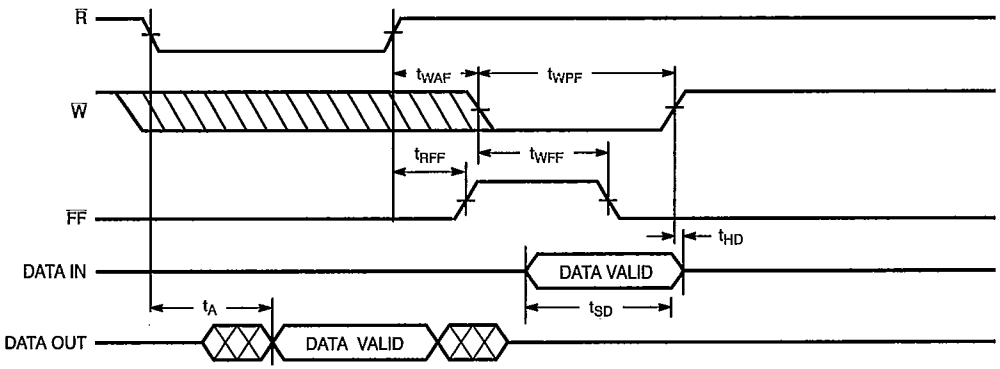
Switching Waveforms (continued)

Empty Flag and Read Data Flow-Through Mode



C432–13

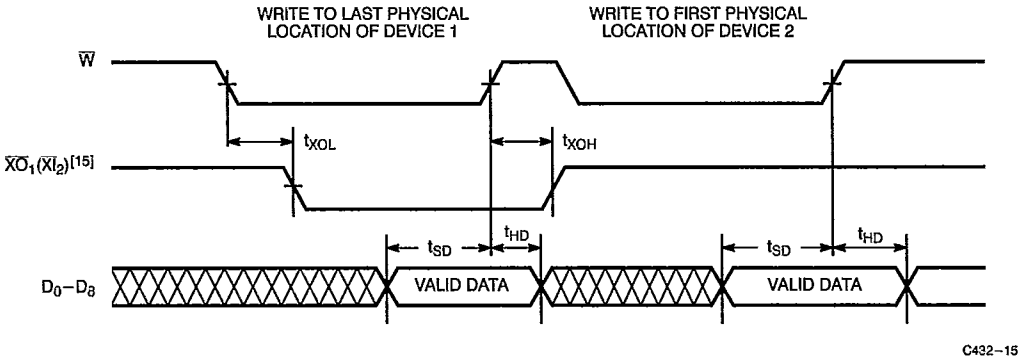
Full Flag and Write Data Flow-Through Mode

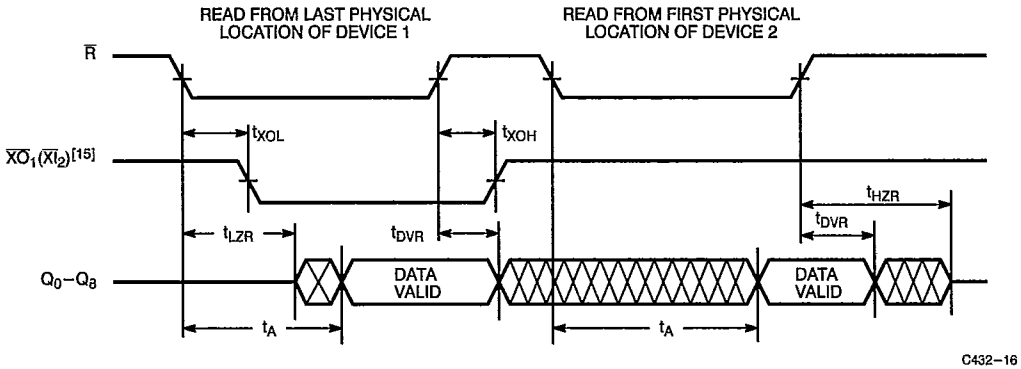


C432–14

Switching Waveforms (continued)

Expansion





Note:
15. Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

Architecture

The CY77C432/33 FIFOs consist of an array of 4096 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$), and Full, Half Full, and Empty flags.

Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operations of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a master reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} nanoseconds before and t_{RMR} nanoseconds after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full flag ($\overline{FF}$). A falling edge of write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs (D_0-D_8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{EF}$) LOW-to-HIGH transition occurs t_{WEF} nanoseconds after the first LOW-to-HIGH transition on the write clock of an empty FIFO. The Half Full flag ($\overline{HF}$) will go LOW on the falling edge of the write clock following the occurrence of half full. $\overline{HF}$ will remain LOW while less than one half of the total memory of this device is available for writing. The LOW-to-HIGH transition of the $\overline{HF}$ flag occurs on the rising edge of read ($\overline{R}$). $\overline{HF}$ is available in single device mode only. The Full flag ($\overline{FF}$) goes LOW on the falling edge of $\overline{W}$ during the cycle in which the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read of a full FIFO.

Reading Data from the FIFO

The falling edge of read ($\overline{R}$) initiates a read cycle if the Empty flag ($\overline{EF}$) is not LOW. Data outputs (Q_0-Q_8) are in a high-impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the depth expansion mode but is not the active device.

The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a HIGH-to-LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be interrogated by the receiver and retransmitted if necessary.

The retransmit ($\overline{RT}$) input is active in the single device mode only. The retransmit feature is intended for use when 4096 or less writes have occurred since the previous $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected. $\overline{R}$ and $\overline{W}$ must both be HIGH during a retransmit cycle. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and will be updated by a retransmit operation.

After a retransmit cycle, previously read data may be reaccessed using $\overline{R}$ to initiate standard read cycles beginning with the first physical location.

Single Device/Width Expansion Modes

Single device and width expansion modes are entered by connecting $\overline{XI}$ to ground prior to an $\overline{MR}$ cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During width expansion mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Depth Expansion Mode (see *Figure 1*)

Depth expansion mode is entered when, during a $\overline{MR}$ cycle, expansion Out ($\overline{XO}$) of one device is connected to expansion in ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the first load ($\overline{FL}$) input, when grounded, indicates that this part is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

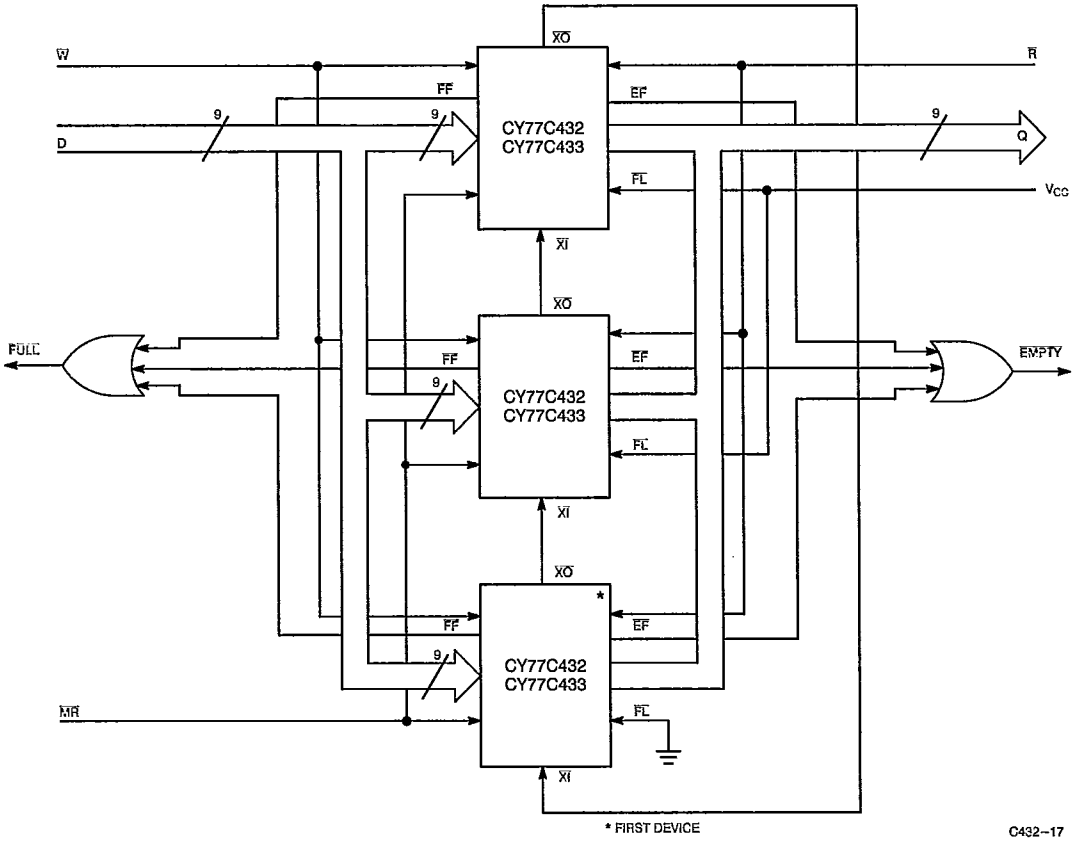
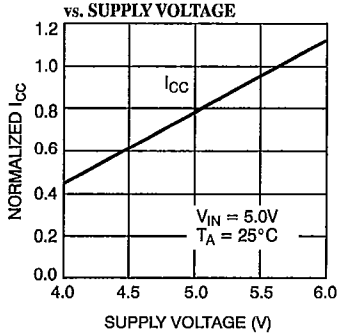


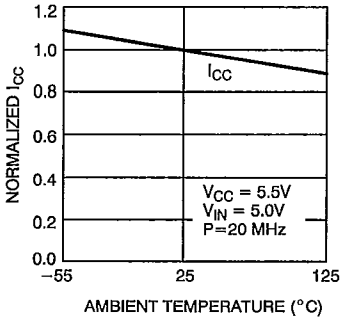
Figure 1. Depth Expansion

Typical DC and AC Characteristics

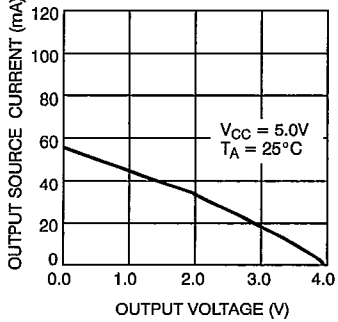
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



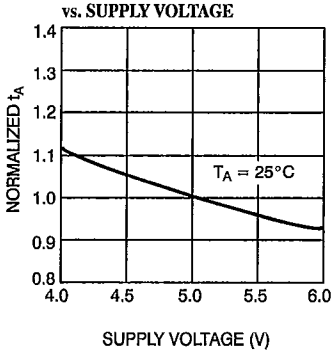
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



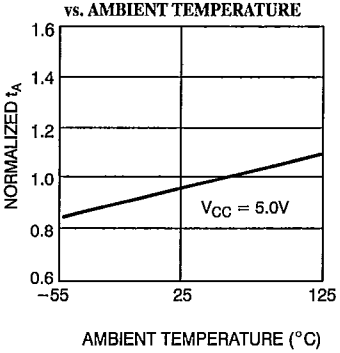
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



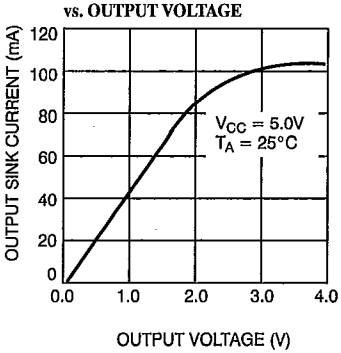
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



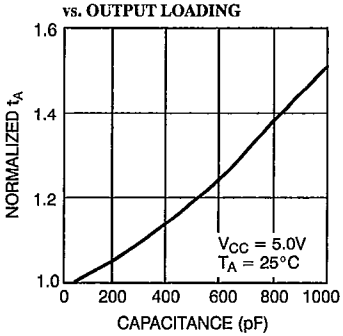
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



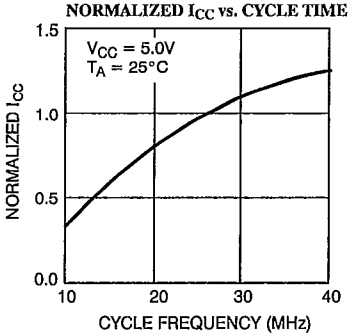
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



C432–18

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C432–25DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–25PC	P15	28-Lead (600-Mil) Molded DIP	
30	CY7C432–30DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C432–30PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–30DMB	D16	28-Lead (600-Mil) CerDIP	Military
40	CY7C432–40DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C432–40PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–40DMB	D16	28-Lead (600-Mil) CerDIP	Military
65	CY7C432–65DC	D16	28-Lead (600-Mil) CerDIP	Commercial
	CY7C432–65PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C432–65PI	P15	28-Lead (600-Mil) Molded DIP	Industrial
	CY7C432–65DMB	D16	28-Lead (600-Mil) CerDIP	Military

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C433–25DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–25VC	V21	28-Lead (300-Mil) Molded SOJ	
30	CY7C433–30DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–30JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–30PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–30KMB	K74	28-Lead Rectangular Cerpack	
	CY7C433–30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C433–40DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–40JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–40PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–40KMB	K74	28-Lead Rectangular Cerpack	
	CY7C433–40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
65	CY7C433–65DC	D22	28-Lead (300-Mil) CerDIP	Commercial
	CY7C433–65JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY7C433–65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65VC	V21	28-Lead (300-Mil) Molded SOJ	
	CY7C433–65JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C433–65PI	P21	28-Lead (300-Mil) Molded DIP	
	CY7C433–65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C433–65KMB	K74	28-Lead Rectangular Cerpack	
	CY7C433–65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPW}	9, 10, 11
t_{WPW}	9, 10, 11
t_{RTC}	9, 10, 11
t_{PRT}	9, 10, 11
t_{RTR}	9, 10, 11
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{FFH}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{XOL}	9, 10, 11
t_{XOH}	9, 10, 11

Document #: 38–00109–C