PRELIMINARY

Integrated Circuit Systems, Inc.

# ICS843001I-23

## FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL/LVCMOS FREQUENCY SYNTHESIZER

## GENERAL DESCRIPTION

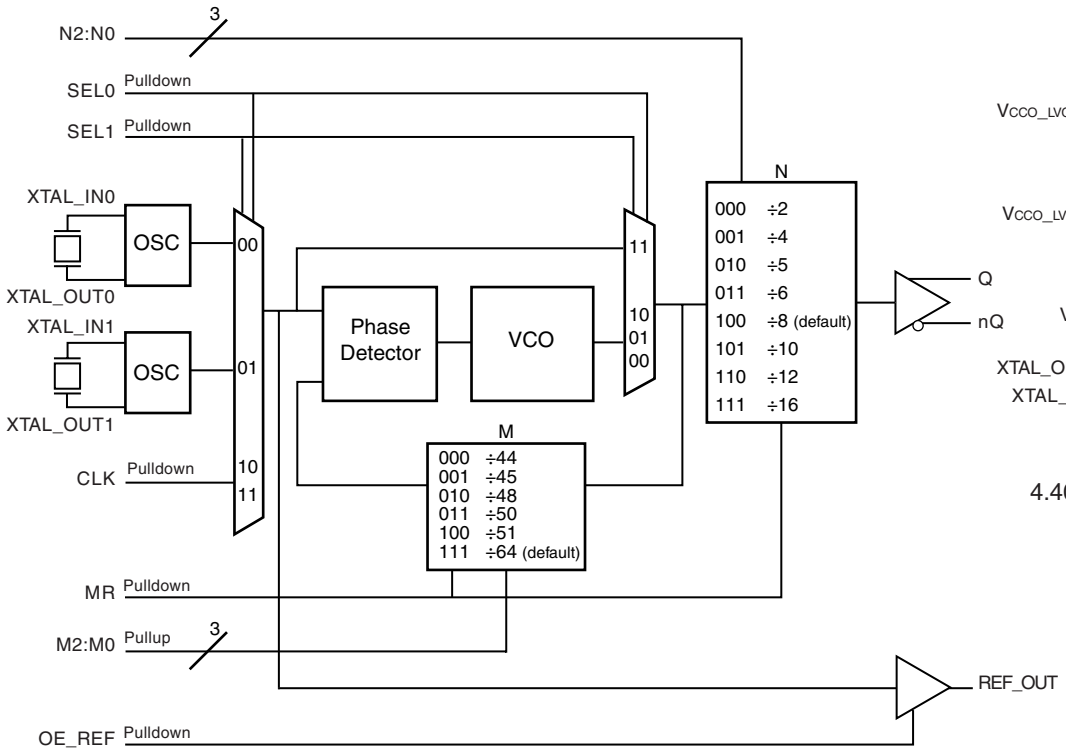
The ICS843001I-23 is a highly versatile, low phase noise LVPECL/LVCMOS Synthesizer which can generate low jitter reference clocks for a variety of communication applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The dual crystal interface allows the synthesizer to support up to three communication standards in a given application (i.e. SONET with a 19.44MHz crystal, 1Gb/10Gb Ethernet and Fibre Channel using a 25MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET, GbE/10Gb Ethernet and SAN applications. The ICS843001I-23 is packaged in a small 24-pin TSSOP package.



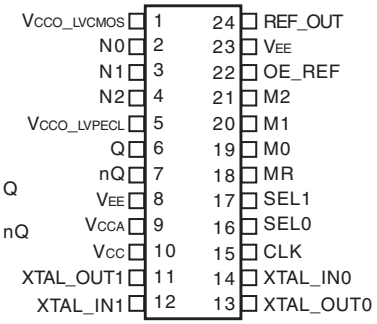
## FEATURES

- One 3.3V LVPECL output pair and one LVCMOS/LVTTL REF_OUT output
- Selectable crystal oscillator interfaces or LVCMOS/LVTTL single-ended input
- Crystal and CLK range: 17.5MHz - 29.54MHz
- Able to generate GbE/10GbE/12GbE, Fibre Channel (1Gb/4Gb/10Gb), PCI-E and SATA from a 25MHz crystal
- VCO range: 1.12GHz - 1.3GHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): <1ps (typical) design target
- Supply modes:
  $V_{CC}/V_{CCO}$
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM




## PIN ASSIGNMENT




**ICS843001I-23**
**24-Lead TSSOP**
4.40mm x 7.8mm x 0.92mm
package body
**G Package**
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{CCO\_CMOS}$ | Power | | Output supply pin for LVCMOS/LVTTL REF_OUT output. |
| 2, 3 | N0, N1 | Input | Pulldown | Output divider select pins. See Table 3C. LVCMOS/LVTTL interface levels. |
| 4 | N2 | Input | Pullup | |
| 5 | $V_{CCO\_LVPECL}$ | Power | | Output supply pin for LVPECL output. |
| 6, 7 | Q, nQ | Ouput | | Differential output pair. LVPECL interface levels. |
| 8, 23 | $V_{EE}$ | Power | | Negative supply pin. |
| 9 | $V_{CCA}$ | Power | | Analog supply pin. |
| 10 | $V_{CC}$ | Power | | Core supply pin. |
| 11<br>12 | XTAL_OUT1,<br>XTAL_IN1 | Input | | Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input. |
| 13<br>14 | XTAL_OUT0,<br>XTAL_IN0 | Input | | Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input. |
| 15 | CLK | Input | Pulldown | LVCMOS/LVTTL clock input. |
| 16, 17 | SEL0, SEL1 | Input | Pulldown | Input MUX select pins. LVCMOS/LVTTL interface levels. |
| 18 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 19, 20 , 21 | M0, M1, M2 | Input | Pullup | Feedback divider select pins. See Table 3B. LVCMOS/LVTTL interface levels. |
| 22 | OE_REF | Input | Pulldown | Reference clock output enable. Default Low. See Table 3E. LVCMOS/LVTTL interface levels. |
| 24 | REF_OUT | Output | | Reference clock output. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{out}$ | Output Impedance | REF_OUT | 5 | 7 | 12 | Ω |

### TABLE 3A. COMMON CONFIGURATIONS TABLE

| Input XTAL Input (MHz) | Feedback Divider | VCO (MHz) | N Divider Value | Output Frequency (MHz) | Application |
|---|---|---|---|---|---|
| 27 | 44 | 1188 | 16 | 74.25 | HDTV |
| 24.75 | 48 | 1188 | 16 | 74.25 | HDTV |
| 19.44 | 64 | 1244.16 | 8 | 155.52 | SONET |
| 19.44 | 64 | 1244.16 | 2 | 622.08 | SONET |
| 19.44 | 64 | 1244.16 | 4 | 311.04 | SONET |
| 25 | 50 | 1250 | 10 | 125 | GigE |
| 25 | 50 | 1250 | 8 | 156.25 | 10 GigE |
| 25 | 50 | 1250 | 5 | 250 | GigE |
| 25 | 50 | 1250 | 4 | 312.5 | XGMII |
| 25 | 50 | 1250 | 2 | 625 | 10 GigE |
| 25 | 45 | 1125 | 6 | 187.5 | 12 GigE |
| 25 | 48 | 1200 | 12 | 100 | PCI Express |
| 25 | 48 | 1200 | 8 | 150 | SATA |
| 25 | 48 | 1200 | 16 | 75 | SATA |
| 25 | 51 | 1275 | 12 | 106.25 | Fibre Channel |
| 25 | 51 | 1275 | 8 | 159.375 | 10 Gig Fibre Channel |
| 25 | 51 | 1275 | 6 | 212.5 | 4 Gig Fibre Channel |



### TABLE 3B. PROGRAMMABLE M OUTPUT DIVIDER FUNCTION TABLE

| Inputs | | | M Divider Value | Input Frequency | |
|---|---|---|---|---|---|
| M2 | M1 | M0 | | Minimum | Maximum |
| 0 | 0 | 0 | 44 | 25.5 | 29.54 |
| 0 | 0 | 1 | 45 | 24.9 | 28.88 |
| 0 | 1 | 0 | 48 | 23.3 | 27.08 |
| 0 | 1 | 1 | 50 | 22.4 | 26.0 |
| 1 | 0 | 0 | 51 | 22.0 | 25.49 |
| 1 | 1 | 1 | 64 (default) | 17.5 | 20.31 |

### TABLE 3C. PROGRAMMABLE N OUTPUT DIVIDER FUNCTION TABLE

| Inputs | | | N Divide Value |
|---|---|---|---|
| N2 | N1 | N0 | |
| 0 | 0 | 0 | 2 |
| 0 | 0 | 1 | 4 |
| 0 | 1 | 0 | 5 |
| 0 | 1 | 1 | 6 |
| 1 | 0 | 0 | 8 (default) |
| 1 | 0 | 1 | 10 |
| 1 | 1 | 0 | 12 |
| 1 | 1 | 1 | 16 |

### TABLE 3D. BYPASS MODE FUNCTION TABLE

| Inputs | | Reference Input | PLL Mode |
|---|---|---|---|
| SEL1 | SEL0 | | |
| 0 | 0 | XTAL0 | Active |
| 0 | 1 | XTAL1 | Active |
| 1 | 0 | CLK | Active |
| 1 | 1 | CLK | Bypass |

### TABLE 3E. OE_REF OUTPUT FUNCTION TABLE

| Inputs | Output |
|---|---|
| OE_REF | REF_OUT |
| 0 | Hi-Z |
| 1 | Active |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ (LVPECL) | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{CCO}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 70°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.



**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO\_LVPECL}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO\_LVCMOS}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | OE_REF = 0 | | TBD | | mA |
| | | OE_REF = 1, REF_OUT = 29.54MHz | | TBD | | mA |
| $I_{CCA}$ | Analog Supply Current | | | 5 | | mA |
| $I_{CCO\_LVPECL}$ | Output Supply Current | OE_REF = 0 | | TBD | | mA |
| $I_{CCO\_LVCMOS}$ | Output Supply Current | OE_REF = 1, REF_OUT = 29.54MHz | | TBD | | mA |

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA}$ = 3.3V±5%, $V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO\_LVPECL}$ | Output Supply Voltage | | 2.625 | 2.5 | 2.625 | V |
| $V_{CCO\_LVCMOS}$ | Output Supply Voltage | | 2.625 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | OE_REF = 0 | | TBD | | mA |
| | | OE_REF = 1, REF_OUT = 29.54MHz | | TBD | | mA |
| $I_{CCA}$ | Analog Supply Current | | | TBD | | mA |
| $I_{CCO\_LVPECL}$ | Output Supply Current | OE_REF = 0 | | TBD | | mA |
| $I_{CCO\_LVCMOS}$ | Output Supply Current | OE_REF = 1, REF_OUT = 29.54MHz | | TBD | | mA |

**TABLE 4C. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO\_LVPECL}, V_{CCO\_LVCMOS}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 2.625 | 2.5 | 2.625 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 2.625 | 2.5 | 2.625 | V |
| $V_{CCO\_LVPECL}$ | Output Supply Voltage | | 2.625 | 2.5 | 2.625 | V |
| $V_{CCO\_LVCMOS}$ | Output Supply Voltage | | 2.625 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | OE_REF = 0 | | TBD | | mA |
| | | OE_REF = 1, REF_OUT = 29.54MHz | | TBD | | mA |
| $I_{CCA}$ | Analog Supply Current | | | 5 | | mA |
| $I_{CCO\_LVPECL}$ | Output Supply Current | OE_REF = 0 | | TBD | | mA |
| $I_{CCO\_LVCMOS}$ | Output Supply Current | OE_REF = 1, REF_OUT = 29.54MHz | | TBD | | mA |



**TABLE 4D. LVCMOS / LVTTL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO\_LVCMOS}$ = 3.3V±5% OR 2.5V±5%, OR $V_{CC} = V_{CCA}$ = 3.3V±5%, $V_{CCO\_LVCMOS}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $V_{CC}$ = 3.3V | 2 | | $V_{CC}$ + 0.3 | V |
| | | | $V_{CC}$ = 2.5V | 1.7 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{CC}$ = 3.3V | -0.3 | | 0.8 | V |
| | | | $V_{CC}$ = 2.5V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | CLK, SEL0, SEL1, OE_REF, MR, N0, N1 | $V_{CC} = V_{IN}$ = 3.465V or 2.625V | | | 150 | µA |
| | | N2, M0:M2 | $V_{CC} = V_{IN}$ = 3.465V or 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK, SEL0, SEL1, OE_REF, MR, N0, N1 | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -5 | | | µA |
| | | N2, M0:M2 | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | REF_OUT | $V_{CCO\_LVCMOS}$ = 3.465V | 2.6 | | | V |
| | | | $V_{CCO\_LVCMOS}$ = 2.625V | 1.8 | | | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | REF_OUT | $V_{CCO\_LVCMOS}$ = 3.465V or 2.625V | | | 0.5 | V |
| ΔV/ΔT | Input Edge Rate | CLK | 20% - 80% | | | TBD | V/ns |

NOTE 1: Output terminated with 50Ω to $V_{CCO\_LVCMOS}/2$. See Parameter Measurement Information Section, "Output Load Test Circuit Diagram" diagrams.

**TABLE 4E. LVPECL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO\_LVPECL}$ = 3.3V±5% OR 2.5V±5%, OR $V_{CC} = V_{CCA}$ = 3.3V±5%, $V_{CCO\_LVPECL}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO\_LVPECL}$ - 1.4 | | $V_{CCO\_LVPECL}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO\_LVPECL}$ - 2.0 | | $V_{CCO\_LVPECL}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_LVPECL}$ - 2V.

**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | MHz |
| Frequency | | 17.5 | | 29.54 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

NOTE: Characterized using an 18pF parallel resonant crystal.



**TABLE 6A. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO\_LVPECL}$, $V_{CCO\_LVCMOS}$ = 3.3V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | 56 | | 650 | MHz |
| $t_{PD}$ | Propagation Delay, NOTE 1 | CLK to REF_OUT | | | TBD | | ns |
| *t*jit(Ø) | RMS Phase Jitter, (Random); NOTE 2, 3 | | 622.08MHz (12kHz - 20MHz) | | TBD | | ps |
| $f_{VCO}$ | PLL VCO Lock Range | | | 1.12 | | 1.3 | GHz |
| $tL_{\_SEL}$ | Select Time | | | | TBD | | ms |
| $tL_{\_M}$ | PLL Lock Time | | | | TBD | | ms |
| $t_R$ / $t_F$ | Output Rise/Fall Time | Q/nQ | 20% to 80% | | 500 | | ps |
| | | REF_OUT | 20% to 80% | | 500 | | ps |
| odc | Output Duty Cycle | Q/nQ | | | 50 | | % |
| | | REF_OUT | | | 50 | | % |

NOTE 1: Measured from the $V_{CC}$/2 of the input to $V_{CCO\_LVCMOS}$/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 6B. AC CHARACTERISTICS,** $V_{CC} = V_{CCA}$ = 3.3V±5%, $V_{CCO\_LVPECL}$, $V_{CCO\_LVCMOS}$ = 2.5V±5%,
TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | 56 | | 650 | MHz |
| $t_{PD}$ | Propagation Delay, NOTE 1 | CLK to REF_OUT | | | TBD | | ns |
| *t*jit(Ø) | RMS Phase Jitter, (Random); NOTE 2, 3 | | 622.08MHz (12kHz - 20MHz) | | TBD | | ps |
| $f_{VCO}$ | PLL VCO Lock Range | | | 1.12 | | 1.3 | GHz |
| $tL_{\_SEL}$ | Select Time | | | | TBD | | ms |
| $tL_{\_M}$ | PLL Lock Time | | | | TBD | | ms |
| $t_R$ / $t_F$ | Output Rise/Fall Time | Q/nQ | 20% to 80% | | 500 | | ps |
| | | REF_OUT | 20% to 80% | | 500 | | ps |
| odc | Output Duty Cycle | Q/nQ | | | 50 | | % |
| | | REF_OUT | | | 50 | | % |

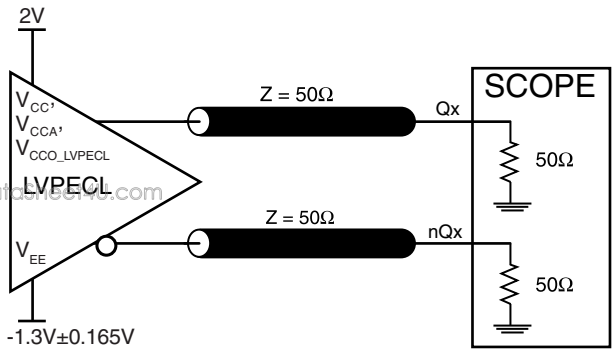
NOTE 1: Measured from the $V_{CC}$/2 of the input to $V_{CCO\_LVCMOS}$/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 6C. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO\_LVPECL,}$ $V_{CCO\_LVCMOS}$ = 2.5V±5%, TA = -40°C TO 85°C

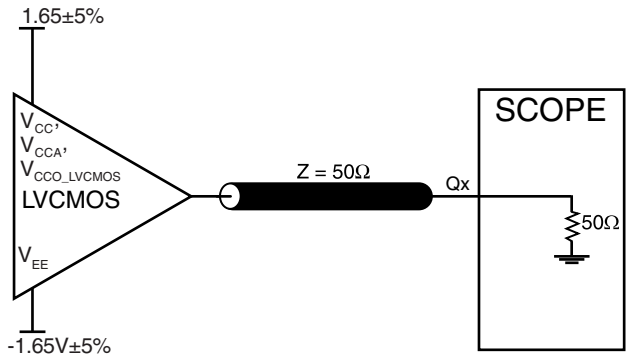
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | 56 | | 650 | MHz |
| $t_{PD}$ | Propagation Delay, NOTE 1 | CLK to REF_OUT | | | TBD | | ns |
| *t*jit(Ø) | RMS Phase Jitter, (Random); NOTE 2, 3 | | 622.08MHz (12kHz - 20MHz) | | TBD | | ps |
| $f_{VCO}$ | PLL VCO Lock Range | | | 1.12 | | 1.3 | GHz |
| $tL_{\_SEL}$ | Select Time | | | | TBD | | ms |
| $tL_{\_M}$ | PLL Lock Time | | | | TBD | | ms |
| $t_R$ / $t_F$ | Output Rise/Fall Time | Q/nQ | 20% to 80% | | 500 | | ps |
| | | REF_OUT | 20% to 80% | | 500 | | ps |
| odc | Output Duty Cycle | Q/nQ | | | 50 | | % |
| | | REF_OUT | | | 50 | | % |

NOTE 1: Measured from the $V_{CC}$/2 of the input to $V_{CCO\_LVCMOS}$/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

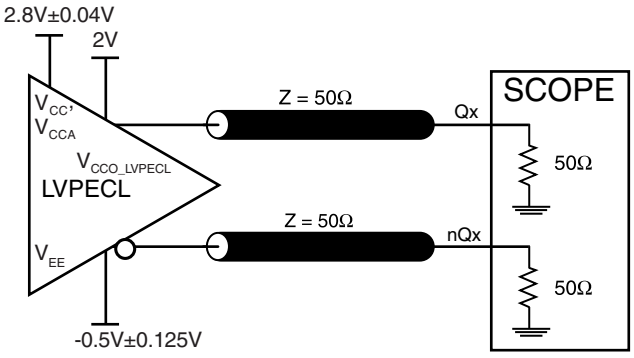
# PARAMETER MEASUREMENT INFORMATION



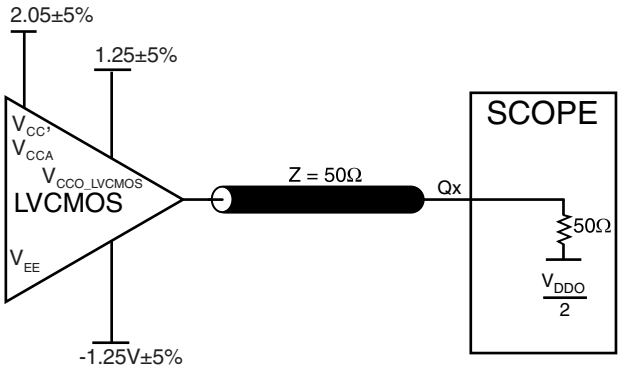

**3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT**



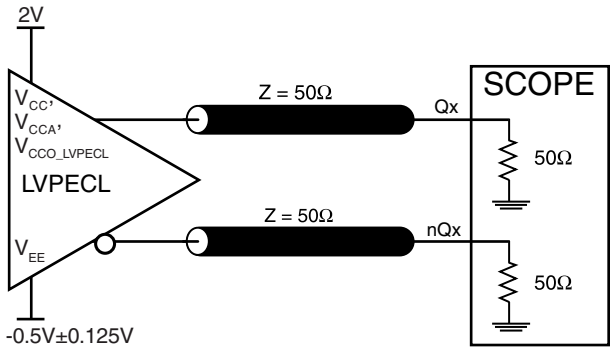

**3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT**



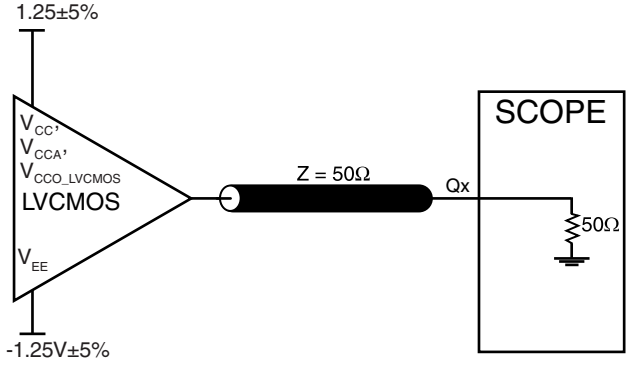

**3.3V CORE/2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT**



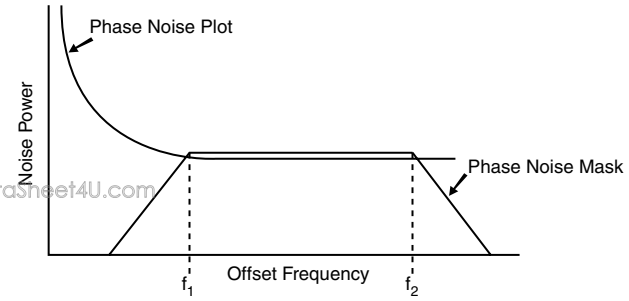

**3.3V CORE/2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT**




**2.5V LVPECL OUTPUT LOAD AC TEST CIRCUIT**

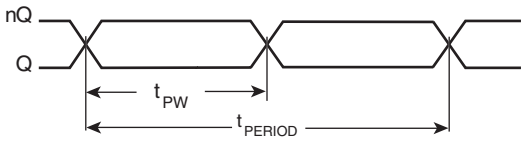



**2.5V LVCMOS OUTPUT LOAD AC TEST CIRCUIT**



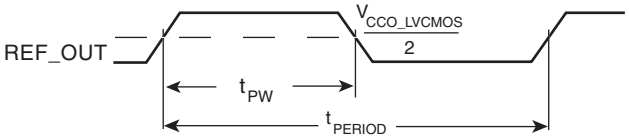

$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

**RMS PHASE JITTER**



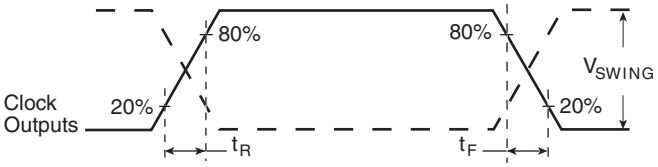

$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**LVPECL OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

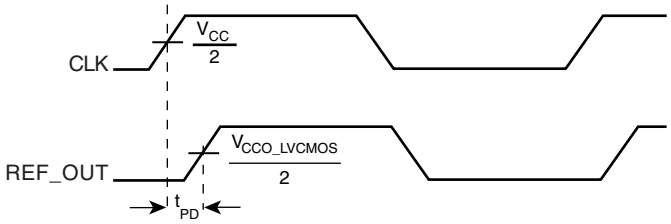



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**




**OUTPUT RISE/FALL TIME**




**PROPAGATION DELAY**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001I-23 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCA}$, and $V_{CCO\_x}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$.



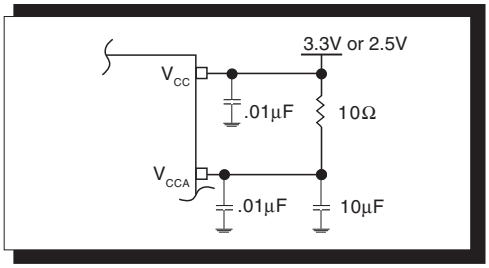



FIGURE 1. POWER SUPPLY FILTERING

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

**CRYSTAL INPUT:**
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

**CLK INPUT:**
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

**CONTROL PINS:**
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### OUTPUTS:

**LVCMOS OUTPUT:**
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

**LVPECL OUTPUT**
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## CRYSTAL INPUT INTERFACE

The ICS843001I-23 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.



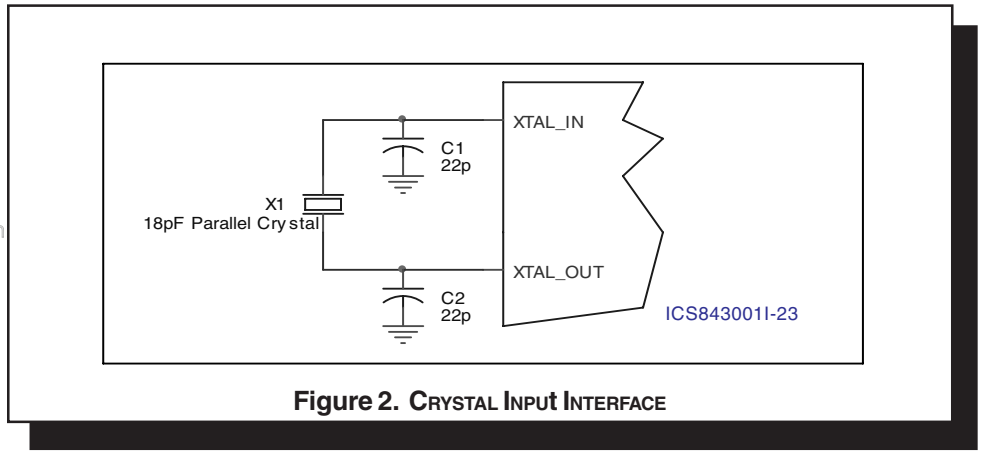



**Figure 2. CRYSTAL INPUT INTERFACE**

## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

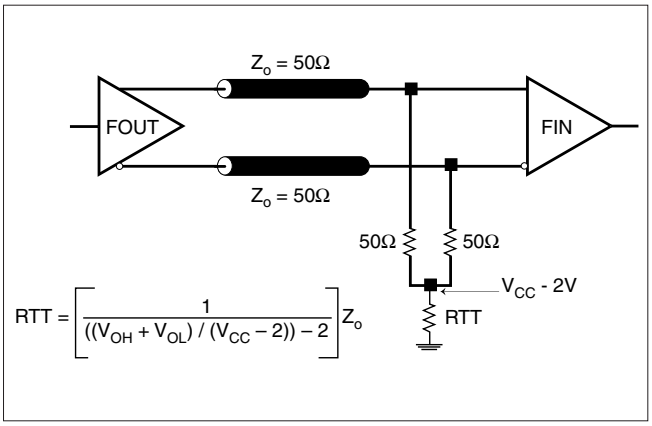



**FIGURE 3A. LVPECL OUTPUT TERMINATION**

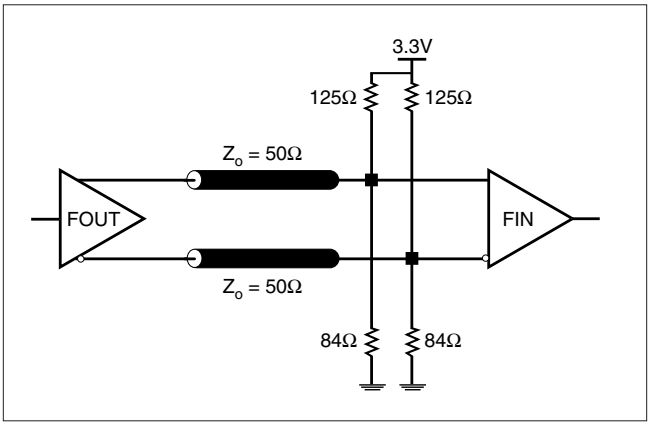



**FIGURE 3B. LVPECL OUTPUT TERMINATION**

## TERMINATION FOR 2.5V LVPECL OUTPUT

*Figure 4A* and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC}$ - 2V. For $V_{CC}$ = 2.5V, the $V_{CC}$ - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*



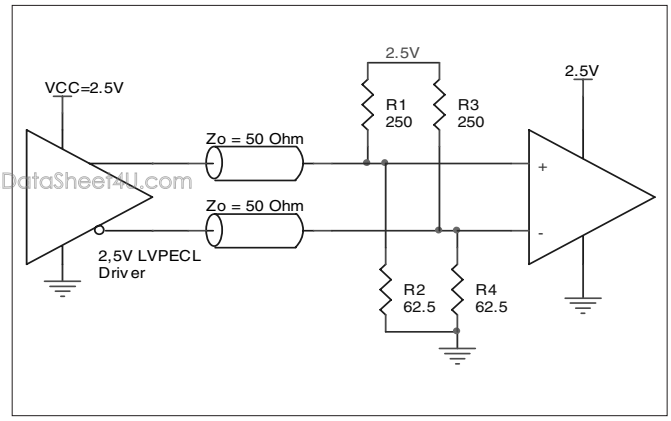



FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

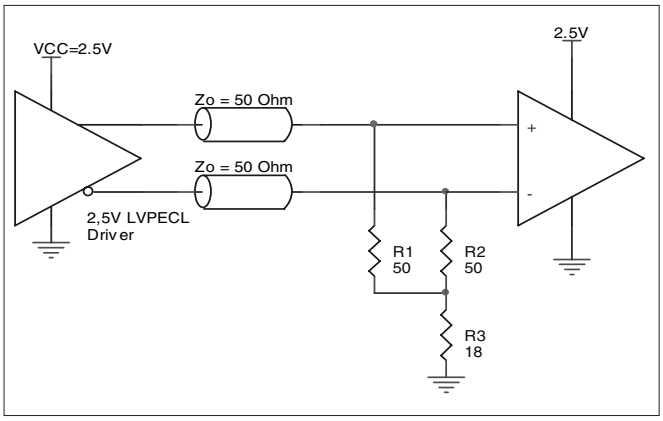



FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

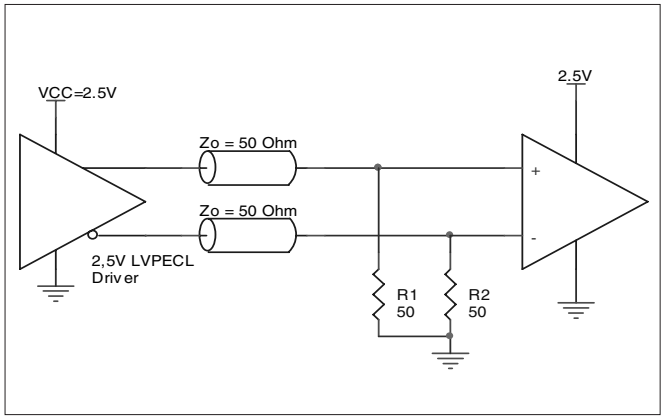



FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

# RELIABILITY INFORMATION

**TABLE 7. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 24 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |



## TRANSISTOR COUNT

The transistor count for ICS843001I-23 is: 4165

## PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

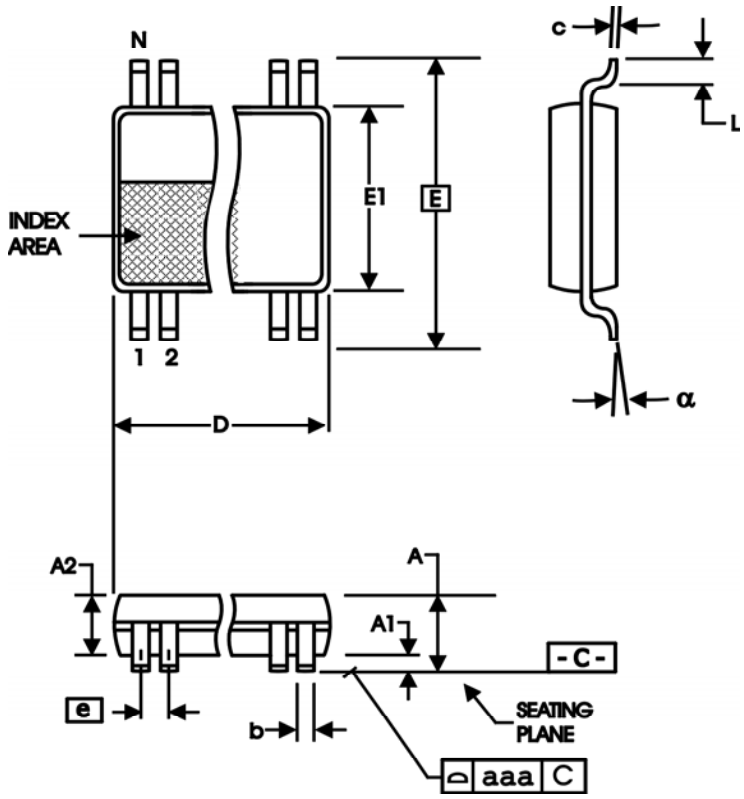





**TABLE 8. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 24 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 7.70 | 7.90 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS843001AGI-23 | ICS843001AI23 | 24 Lead TSSOP | tube | -40°C to 85°C |
| ICS843001AGI-23T | ICS843001AI23 | 24 Lead TSSOP | 2500 tape & reel | -40°C to 85°C |
| ICS843001AGI-23LF | TBD | 24 Lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| ICS843001AGI-23LFT | TBD | 24 Lead "Lead-Free" TSSOP | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.