EMIF10-COM01F2

EMI FILTER INCLUDING ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS

EMI filtering and ESD protection for:

- Computers and printers
- Communication systems
- Mobile phones

DESCRIPTION

The EMIF10-COM01F2 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

BENEFITS

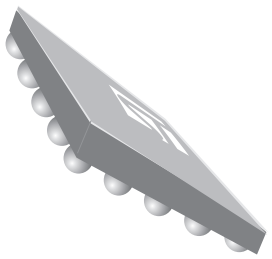
- EMI symmetrical (I/O) low-pass filter
- Lead free package
- Very low PCB space consuming: < 6mm^2
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on both input & output pins
- High reliability offered by monolithic integration

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2 level 4

15kV (air discharge)

8kV (contact discharge)



Flip-Chip (25 Bumps)

Table 1: Order Code

Part Number	Marking
EMIF010-COM01F2	FE

Figure 1: Pin Configuration (Ball side)

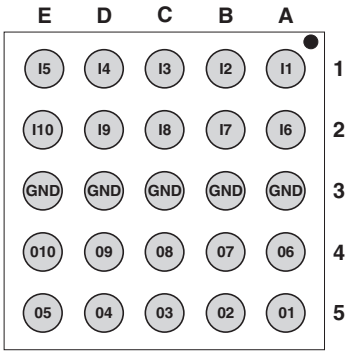


Figure 2: Basic cell configuration

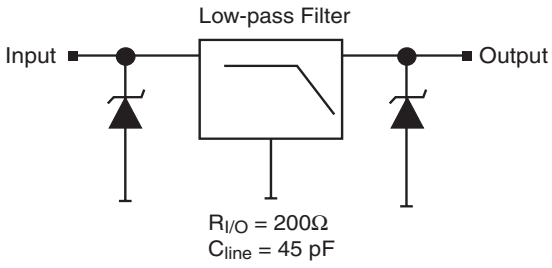


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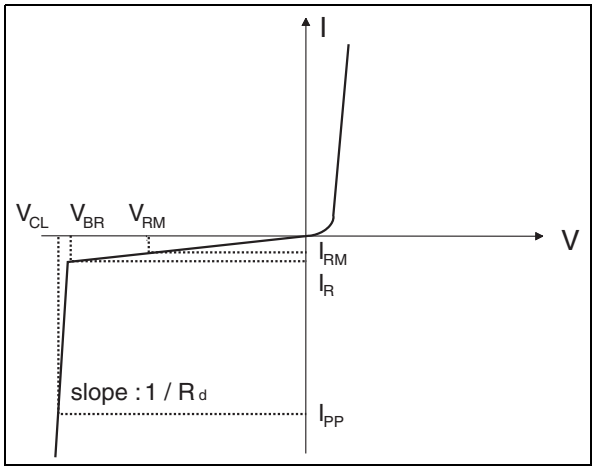
Table 2: Absolute Ratings (T_{amb} = 25°C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3V per line			500	nA
R_d	I_{PP} = 10A, t_p = 2.5µs		1		Ω
$R_{I/O}$		180	200	220	Ω
C_{line}	At 0V bias		45	50	pF
t_{LH}	Vinput = 2.8V Rload = 100kΩ			25	ns

Figure 3: S21(db) attenuation measurement

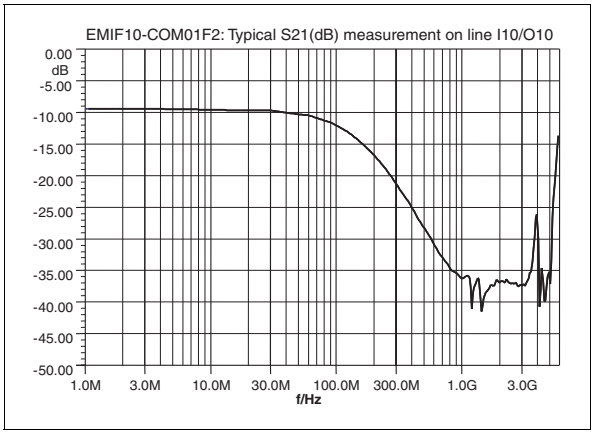
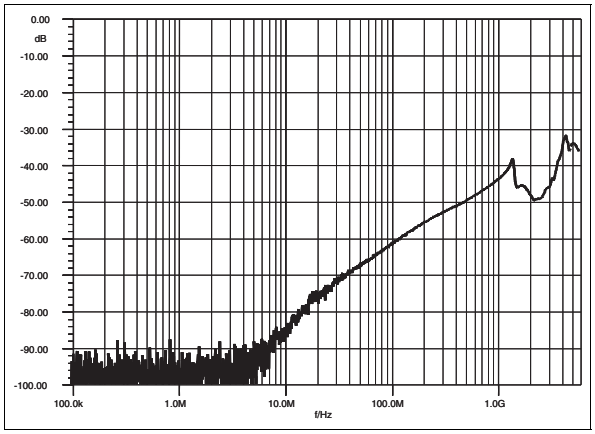


Figure 4: Analog crosstalk



Note: Spikes at high frequencies are induced by the PCB layout

Figure 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)

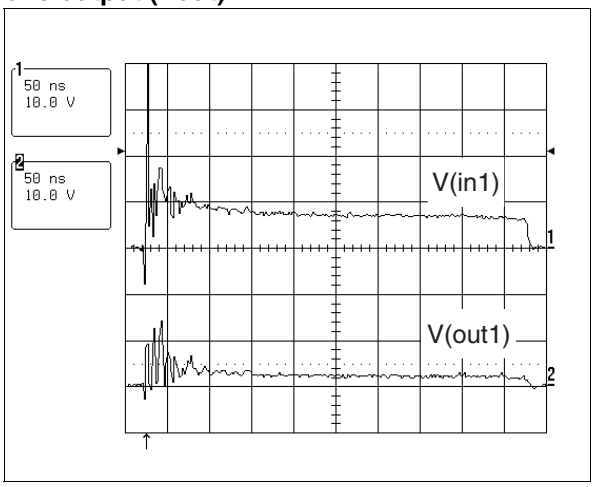


Figure 6: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout)

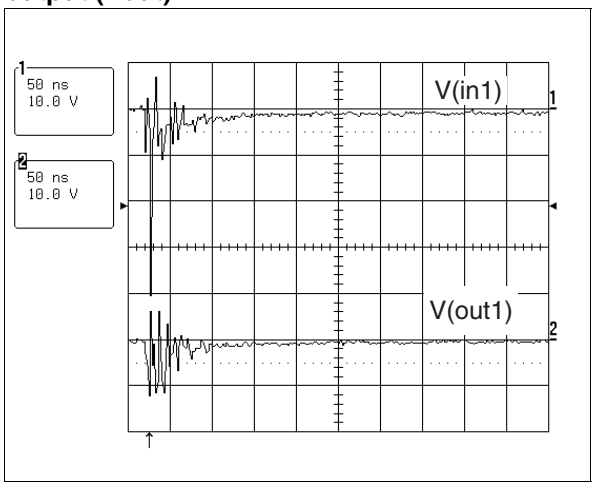


Figure 7: Rise time measurement

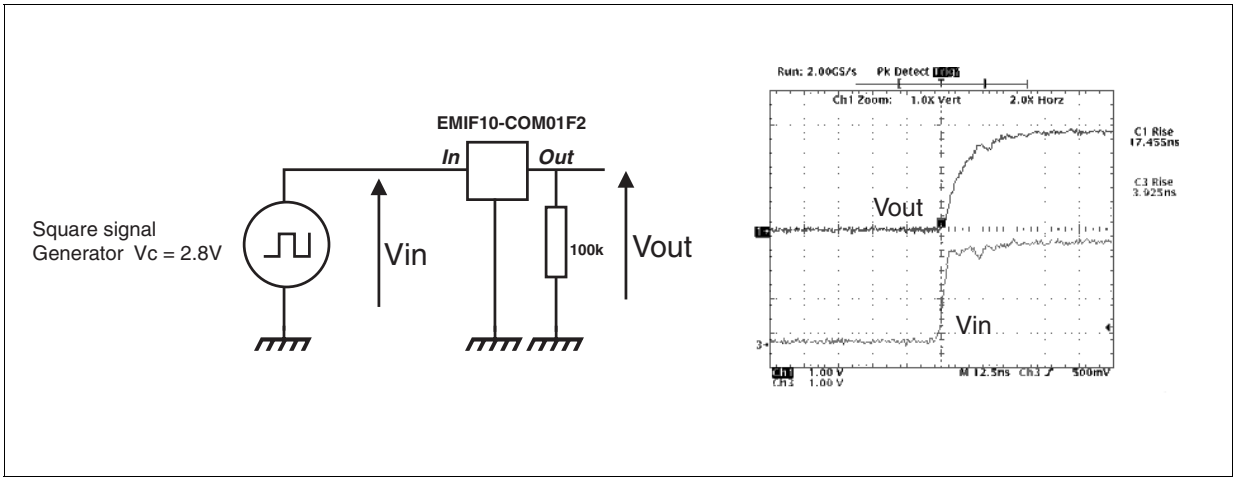


Figure 8: Capacitance versus reverse applied voltage

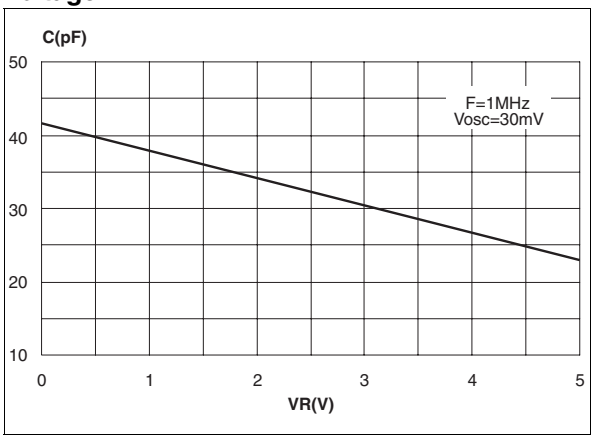
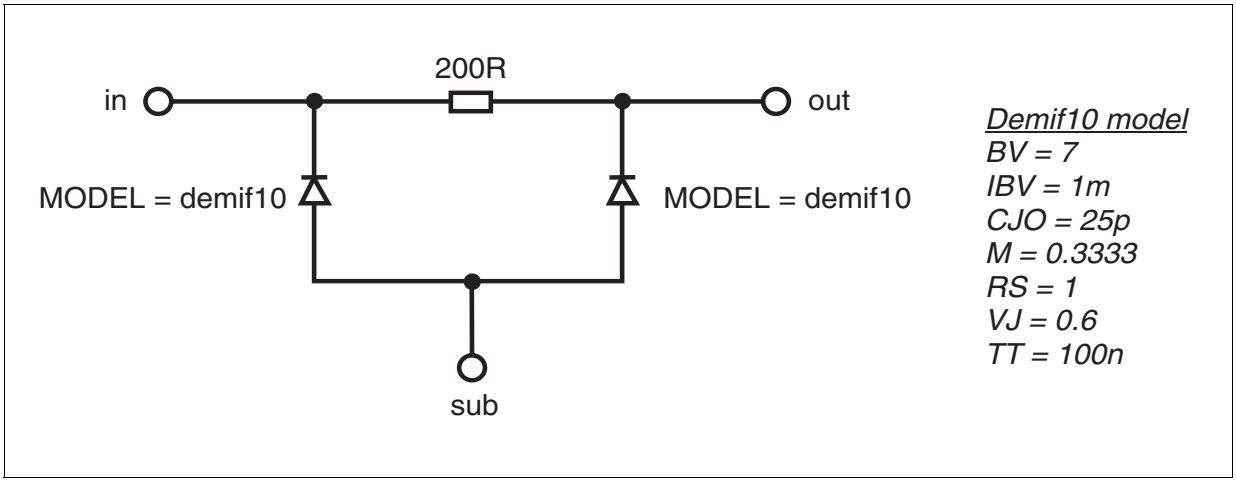


Figure 9: Aplac model



PCB grounding recommendations

In order to ensure a good efficiency in terms of ESD protection and filtering behavior, we recommend to implement microvias (100 µm dia.) between the GND bumps and the GND layer. GND bumps can be connected together in PCB layer 1, and in addition, if possible, use through hole vias (200 µm dia.) in both sides of filter to improve contact to GND (layer). This layout will minimize the distance to the ground and thus parasitic inductances. In addition, we recommend to have GND plane wherever possible.

Figure 10: Ordering Information Scheme

EMIF yy - xxx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
F = Flip-Chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm
= 3: Leadfree Pitch = 400µm, Bump = 250µm

Figure 11: FLIP-CHIP Package Mechanical Data

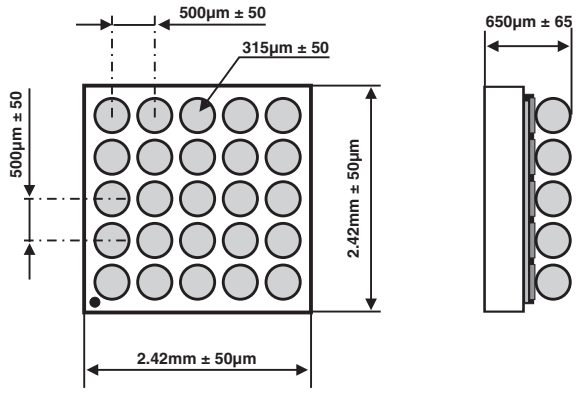


Figure 12: Foot print recommendations

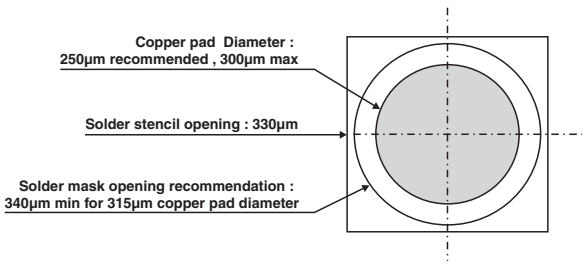


Figure 13: Marking

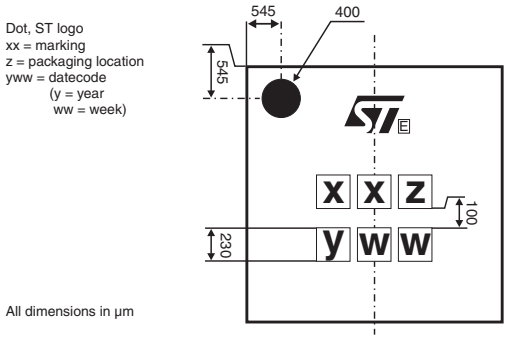


Figure 14: FLIP-CHIP Tape and Reel Specification

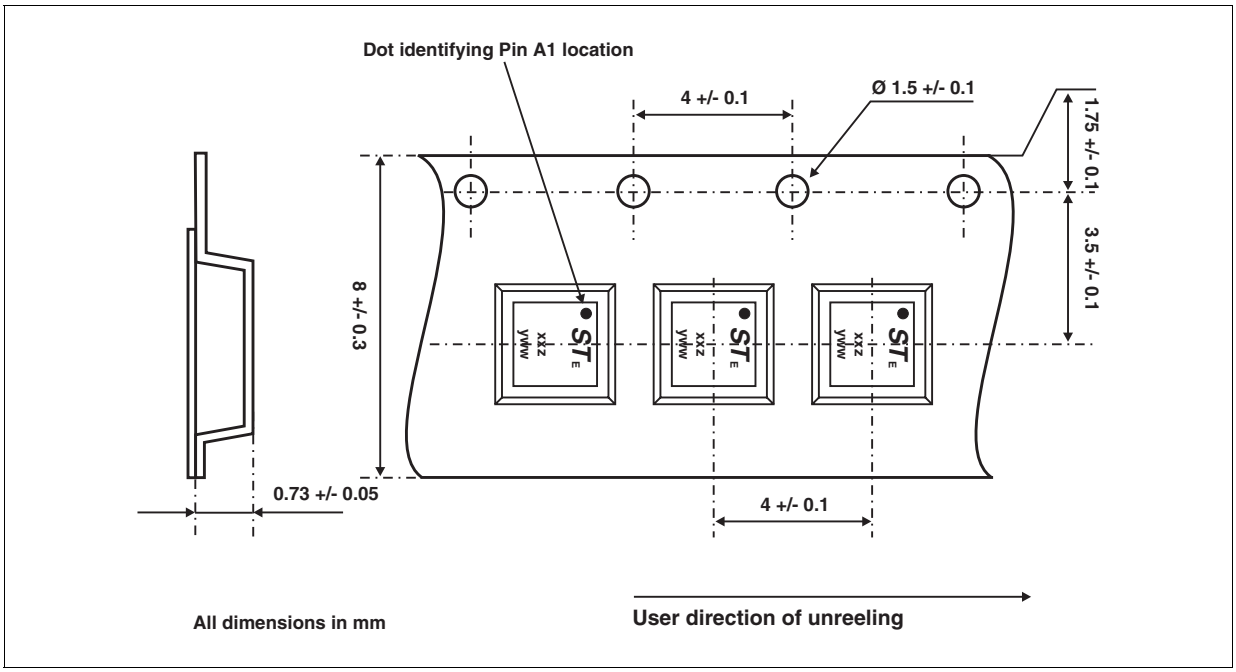


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-COM01F2	FE	Flip-Chip	8.3 mg	5000	Tape & reel

Note: More informations are available in the application notes:
AN1235: “Flip-Chip: Package description and recommendations for use”
AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
14-Dec-2004	1	First issue.
12-Apr-2005	2	Die clearance reduction.