CYPRESS SEMICONDUCTOR

32K x 9 Synchronous Pentium™ CPU Cache R/W RAM

Features

- **Supports 66-MHz Pentium CPU cache systems**
- **Supports zero-wait-state performance**
- **7.5-ns access delay (clock to output) with 0 pF**
- **9-ns access delay (clock to output) with 85 pF**
- **Allows Pentium CPU address pipelining**
- **Available in PQFP with 25-Mil lead pitch and standard PLCC/LCC**
- **BiCMOS for optimum speed/power**
- **Two-bit wraparound counter supporting the Pentium microprocessor burst sequence**
- **Separate address strobes from processor and from cache controller**
- **Synchronous self-timed write**
- **Internal clamp diodes**
- **Direct interface with the processor and external cache controller**
- **Two complementary synchronous chip enables**
- **Asynchronous output enable**
- **JEDEC-standard 44-pin PLCC pinout**

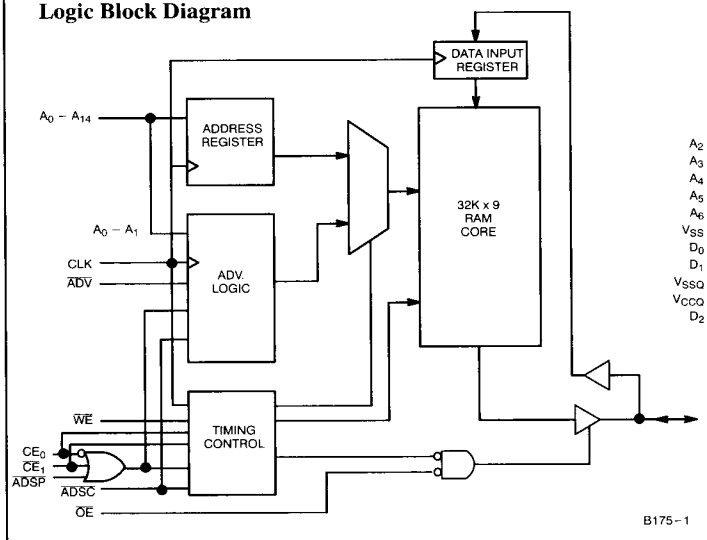
Functional Description

The CY7B175 is a 32K by 9 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. A two-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7B175 is designed for Intel Pentium microprocessor–based systems; its counter follows the burst sequence of the Pentium microprocessor. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

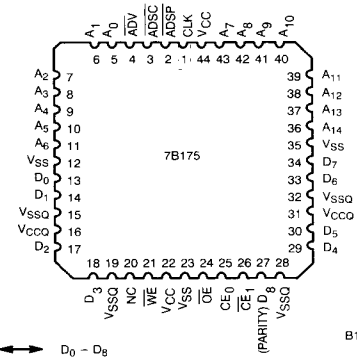
A synchronous self-timed write mechanism is provided to simplify the write interface. Two complementary synchronous chip select inputs are provided to support two banks of memory (256 Kbytes) with no external logic. These signals, in conjunction with the asynchronous output enable ($\overline{OE}$) signal, greatly simplify memory bank selection. The I/O and ADDR pins have internal clamp diodes to prevent overshoot and undershoot. The part is available in the very small outline plastic quad flat pack (PQFP) and PLCC/LCC packages.

Logic Block Diagram



Pin Configuration

LCC/PLCC/PQFP
Top View



Selector Guide

		7B175–7	7B175–8	7B175–11
Maximum Access Time (ns)		7.5	8.5	11.5
Maximum Operating Current (mA)	Commercial	210	210	210
	Military			250

Pentium is a trademark of Intel Corporation.

Functional Description (continued)

Single-Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) CE_0 = 1 and $\overline{CE_1}$ = 0 and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic use this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7B175 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if CE_0 = 0 or $\overline{CE_1}$ = 1.

If $\overline{WE}$ is LOW at the next clock rise, information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Because the CY7B175 is a common I/O device, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single-Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at the rising edge of the clock: (1) CE_0 = 1 and $\overline{CE_1}$ = 0, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is LOW. $\overline{ADSC}$-triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. Information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Since the CY7B175 is a common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WE}$ is sampled LOW regardless of the state of the $\overline{OE}$ input.

Single-Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) CE_0 = 1 and $\overline{CE_1}$ = 0, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at D_0 through D_8 a maximum of 14 ns after clock rise. $\overline{ADSP}$ is ignored if CE_0 = 0 or $\overline{CE_1}$ = 1.

Burst Sequences

The CY7B175 provides a two-bit wraparound counter implementing the Intel Pentium sequence (see *Table 1*). Note that the burst sequence depends on the location of the first burst address.

Table 1. Counter Implementation for the Intel Pentium Sequence

First Address		Second Address		Third Address		Fourth Address	
A_{X+1}	A_X	A_{X+1}	A_X	A_{X+1}	A_X	A_{X+1}	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

Application Example

Figure 1 shows a 256-Kbyte secondary cache for the Pentium microprocessor using eight CY7B175 cache RAMs and a CY7B181 cache tag. Address from the Pentium CPU is checked by the cache tag at the beginning of each access. Match reset is delivered to the cache controller after 10 ns.

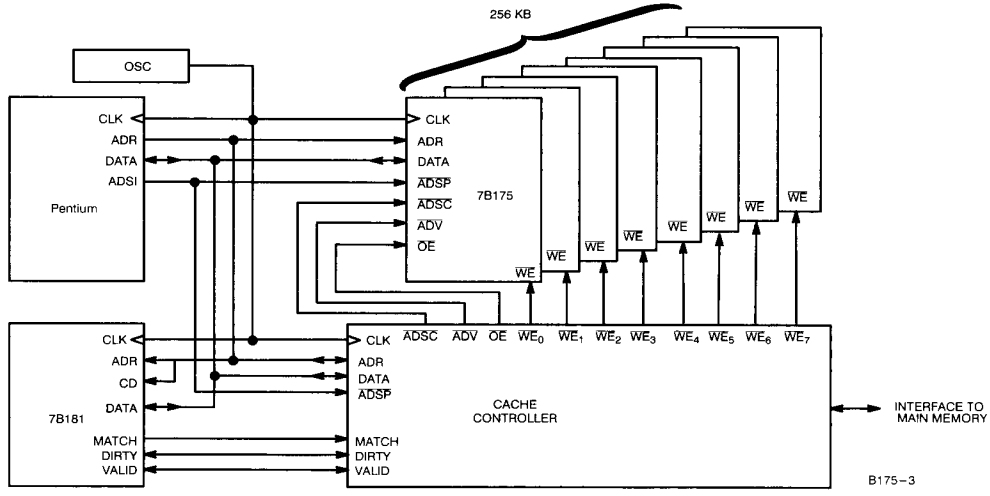


Figure 1. Cache Using Eight CY7B175s

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_{14}$	I	Address Inputs
CLK	I	Clock
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable
CE_0, $\overline{CE_1}$	I	Chip Enables
$\overline{ADV}$	I	Address Advance
$\overline{ADSP}$	I	Processor Address Strobe
$\overline{ADSC}$	I	Cache Controller Address Strobe
$D_0 - D_8$	I/O	Data I/O
V_{CC}	–	+5V Power Supply
V_{SS}	–	Ground
V_{CCQ}	–	Output Buffer (Driver) Power Supply
V_{SSQ}	–	Output Buffer (Driver) Ground
NC	–	Not Connected Internally

Pin Descriptions

Input Signals	
CLK	Clock signal used as the reference for most on-chip operations.
$\overline{ADSP}$	Address strobe signal from the processor: $\overline{ADSP}$ is asserted when the processor address is valid. If $\overline{ADSP}$ is LOW at clock rise, the address at A_0 through A_{14} will be loaded into the address register and the address advancement logic. The write signal, $\overline{WE}$, is ignored in the clock cycle where $\overline{ADSP}$ is asserted. If both $\overline{ADSP}$ or $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized. $\overline{ADSP}$ is ignored when $CE_0 = 0$ or $\overline{CE_1} = 1$.
$\overline{ADSC}$	Address strobe signal from the cache controller: $\overline{ADSC}$ is asserted when a new address generated by the cache controller is ready to be strobed into the CY7B175/4A. The write signal, $\overline{WE}$, is recognized in the clock cycle where $\overline{ADSC}$ is asserted. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$A_0 - A_{14}$	Address lines: These address inputs are loaded into the address register and the address advancement logic at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. They are used to select one of the 32K locations.
$\overline{WE}$	Write Enable: This signal is sampled at the rising edge of the clock signal. If $\overline{WE} = 0$, a self-timed write operation will be initiated and data on $D_0 - D_8$ will be stored into the selected memory location. The only exception occurs if both $\overline{ADSP}$ and $\overline{WE}$ are LOW at clock rise. In this case, the write signal is ignored.
$\overline{ADV}$	Address Advance input: $\overline{ADV}$ is sampled at the rising edge of the clock. In the case of the CY7B175, LOW at this input will advance the address in the advancement logic according to the Intel 80486 burst sequence. In the case of the CY7B174A, the addresses will be advanced linearly. This input is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is active (LOW).
$CE_0 - \overline{CE_1}$	Chip Enable inputs: CE_0 is active HIGH and $\overline{CE_1}$ is active LOW. If $CE_0 = 0$, $\overline{CE_1} = 1$ and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $CE_0 = 1$, $\overline{CE_1} = 0$ and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $CE_0 = 0$ or $\overline{CE_0} = 1$, $\overline{ADSP}$ is ignored.
$\overline{OE}$	Output Enable: $\overline{OE}$ is an asynchronous signal that disables all output drivers ($D_0 - D_8$) when it is deasserted. $\overline{OE}$ should be deasserted during write cycles because the CY7B175/4A is a common I/O device and three-state conflict may occur at the data pins.
NC	Not connected internally: Can be left open or tied to V_{SS} or V_{CC}.
Bidirectional Signals	
$D_0 - D_8$	Data I/O lines: During a read cycle, if $\overline{OE}$ is asserted, data in the selected location will appear at these pins. During a write cycle, data presented at these pins is captured at clock rise and stored into the selected RAM location if $\overline{WE}$ is LOW. All nine outputs will be placed in a three-state condition when $\overline{OE}$ is deasserted, when the RAM is deselected via the chip select inputs, or during a write cycle.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B175−7, 8 Min.	7B175−7, 8 Max.	7B175−11 Min.	7B175−11 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−1.0	+1.0	−1.0	+1.0	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		210		210	mA
			Mil				250	
I_{SB1}	AC Standby Current	$\overline{CE_0}$, $\overline{CE_1}$ = V_{IH}, I_{OUT} = 0 mA, All Inputs= V_{IL} or V_{IH}, V_{IL}=0.0V and V_{IH} ≥ 3.0V, Cycle Time ≥ t_{CYC} Min.			50		50	mA
I_{SB2}	CMOS Standby Current	$\overline{CE_0}$, $\overline{CE_1}$ ≥ V_{CC} −0.2V, All Inputs=V_{CC} −0.2V or ≤ 0.2V, Cycle Time ≥ t_{CYC} Min.			40		40	mA

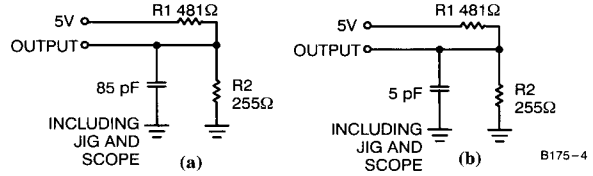
Capacitance[4]

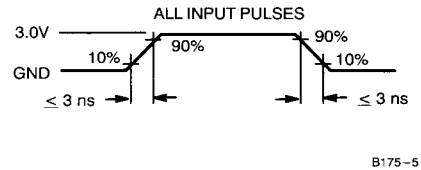
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	3.5	pF
C_{IN}: Other Inputs			4	pF
C_{OUT}	Output Capacitance		5.5	pF

Notes:

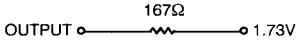
1. $V_{IL\,(min.)}$ = − 1.5V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters (PLCC package).

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



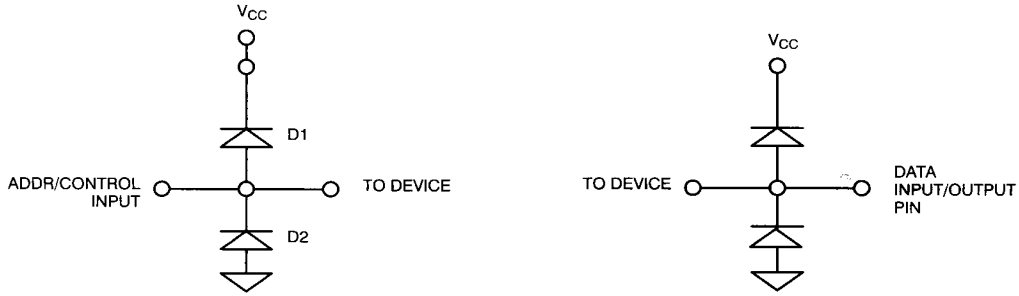
Switching Characteristics Over the Operating Range[5]

Parameter	Description	7B175–7		7B175–8		7B175–11		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15		16.6		20		ns
f_{MAX}	Maximum Frequency		66		60		50	MHz
t_{CH}	Clock HIGH	4		5		7		ns
t_{CL}	Clock LOW	4		5		7		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CDV1}	Data Output Valid After CLK Rise (0-pF Load)		7.5		8.5		11.5	ns
t_{CDV2}	Data Output Valid After CLK Rise (85-pF Load)		9		10		13.5	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{WES}	$\overline{WE}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{WEH}	$\overline{WE}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		1		ns
t_{CES}	Chip Enable Set-Up	2.5		2.5		3		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		1		ns
t_{CEOZ}	Chip Enable Sampled to Output High Z[6, 7]	2	6	2	6	2	7	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[6]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		6		6		6	ns
t_{WEOZ}	$\overline{WE}$ Sampled LOW to Output High Z[6]		6		6		7	ns
t_{WEOV}	$\overline{WE}$ Sampled HIGH to Output Valid		9		10		13.5	ns

Notes:

5. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
6. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given voltage and temperature, t_{CSOZ} (t_{WEOZ}) min. is less than t_{CSOV} (t_{WEOV}) min.

Input/Output ESD and Clamp Diode Protection

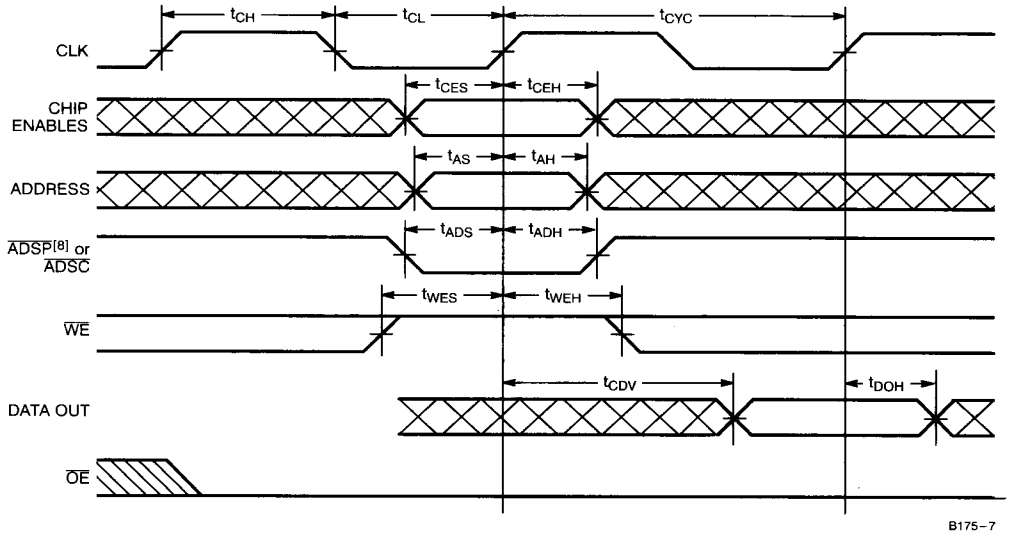


(a) Input ESD and Clamp Diode **(b) Input/Output ESD and Clamp Diode**

B175-6

Switching Waveforms

Single Read

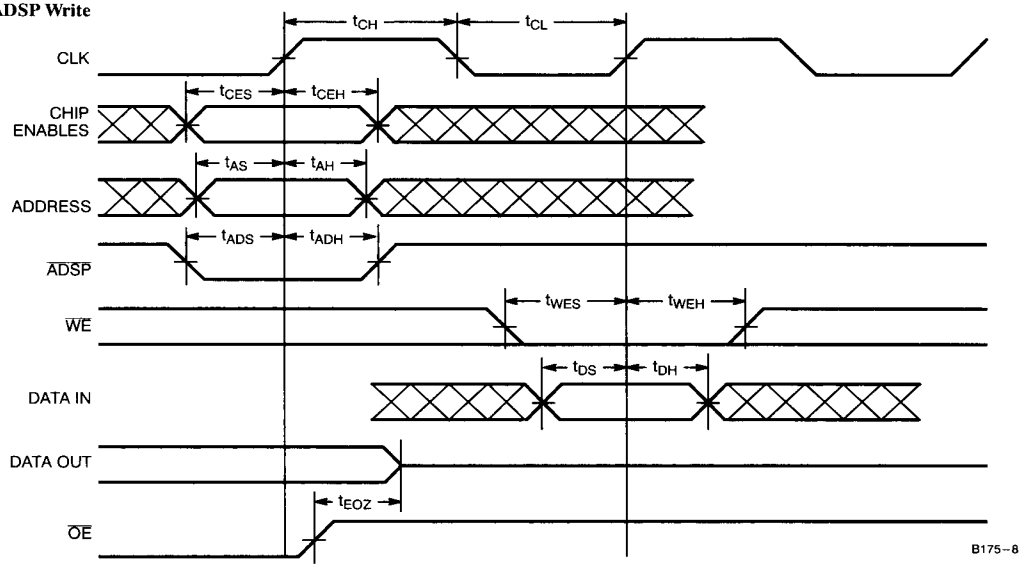


B175-7

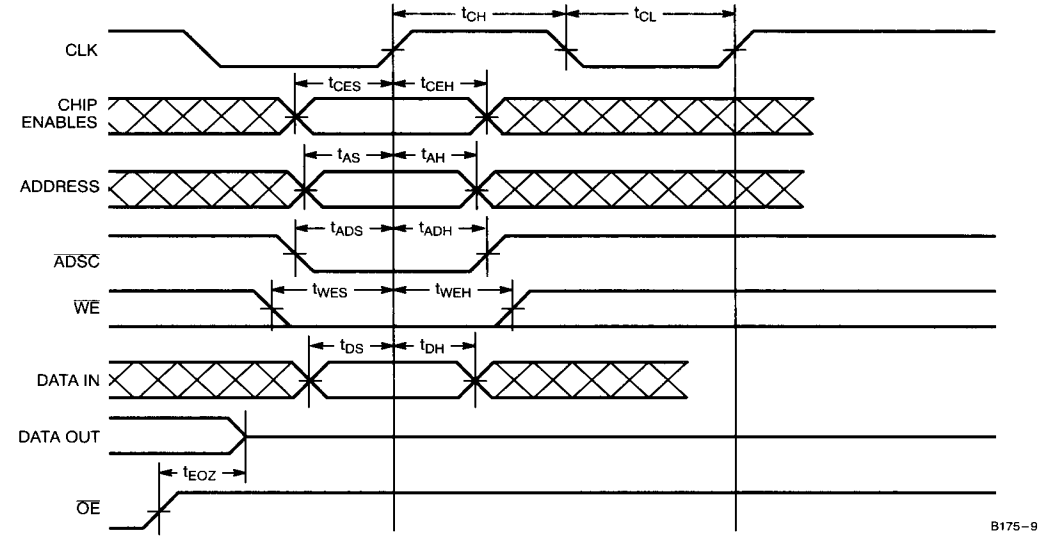
Note:
8. If $\overline{ADSP}$ is asserted while $CE_0 = 0$ or $\overline{CE_0} = 1$, $\overline{ADSP}$ will be ignored.

Switching Waveforms (continued)

ADSP Write

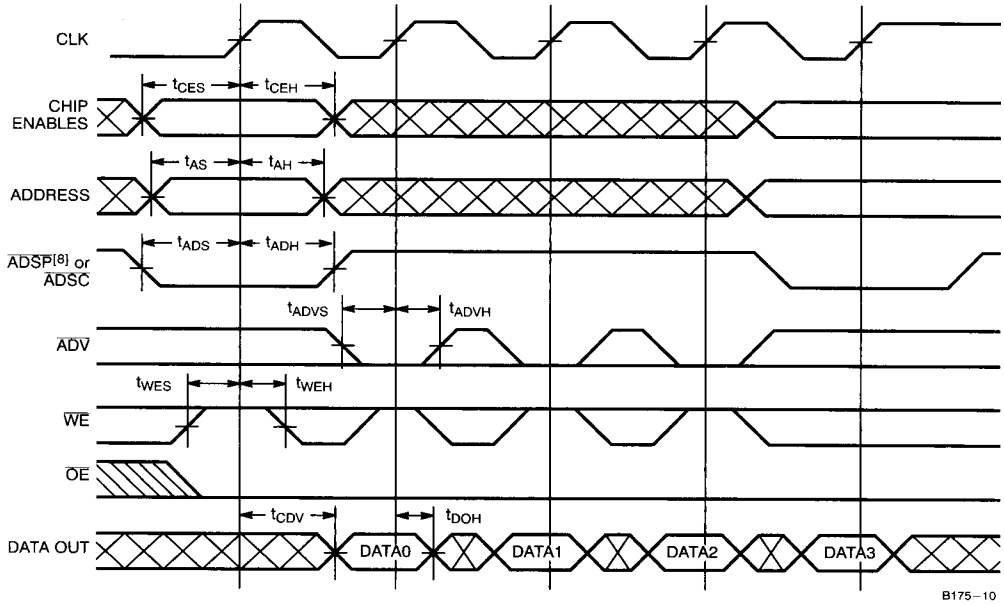


Single Cache Controller Write



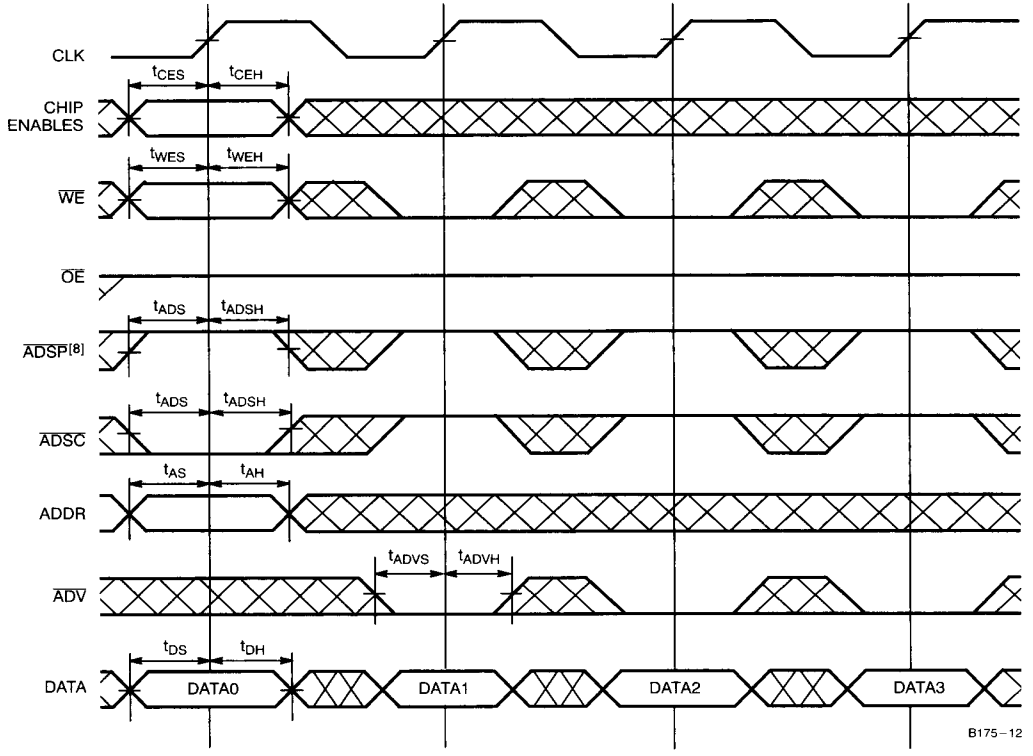
Switching Waveforms (continued)

Burst Read Sequence with Four Accesses

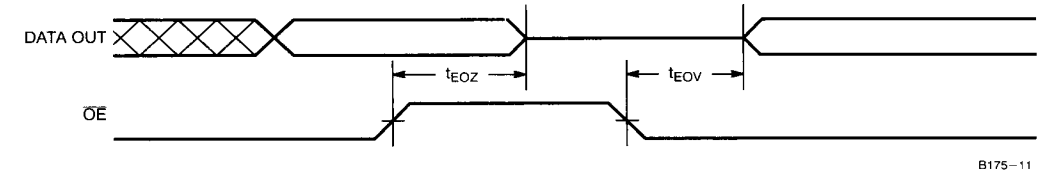


Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSC}$

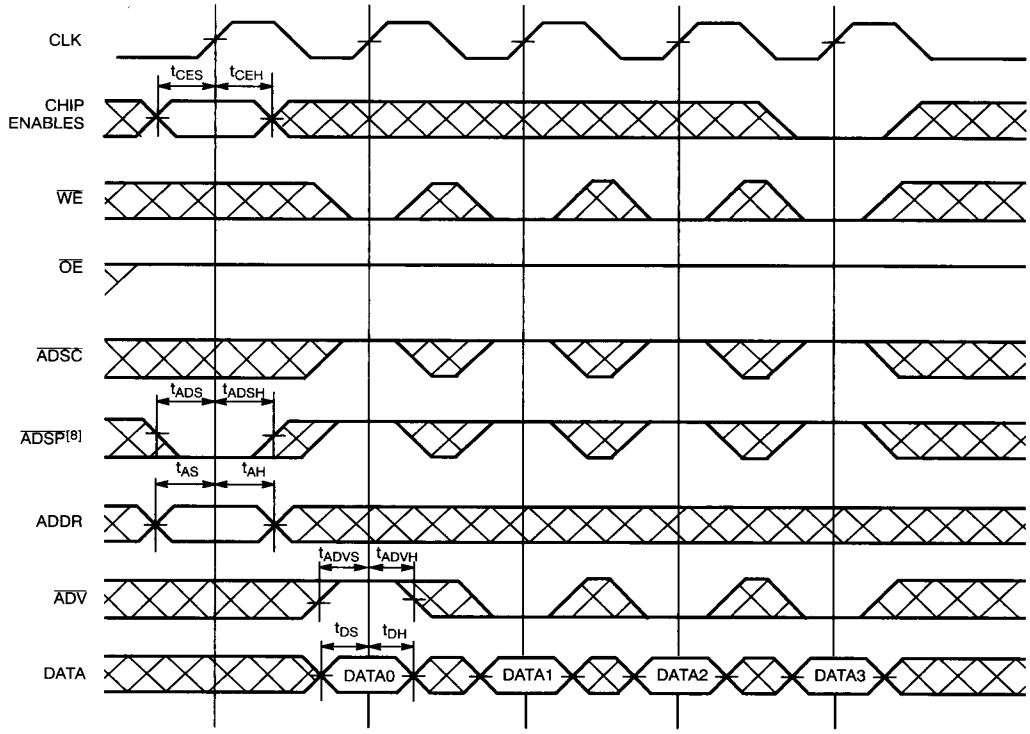


Output (Controlled by $\overline{OE}$)

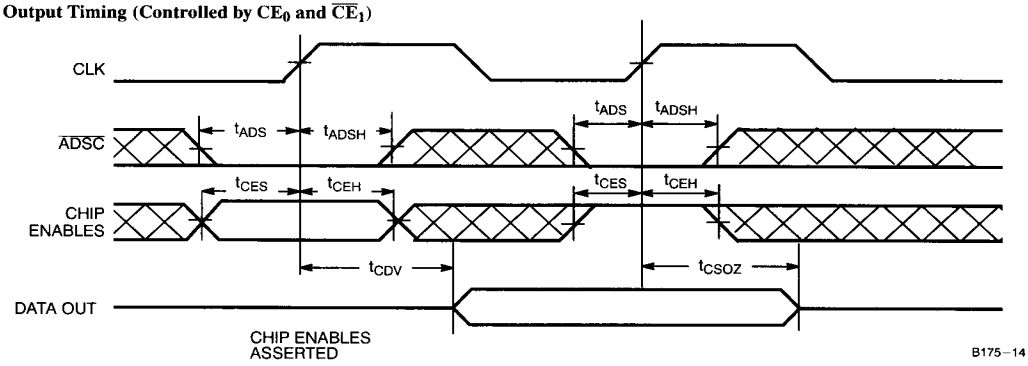


Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

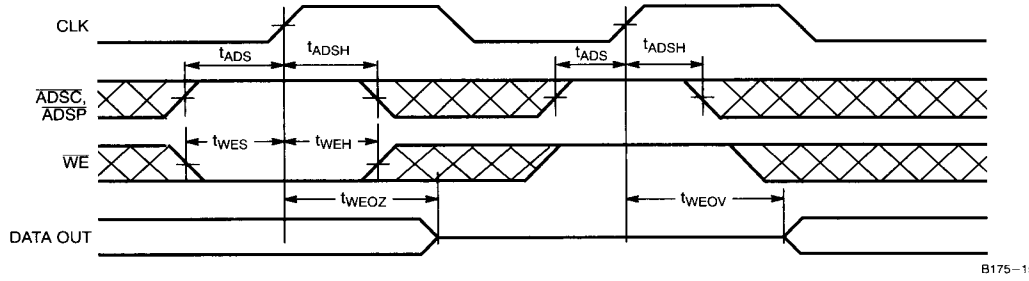


Output Timing (Controlled by CE_0 and $\overline{CE_1}$)



Switching Waveforms (continued)

Output Timing (Controlled by $\overline{WE}$)



Synchronous Truth Table[9, 10, 11, 12]

Inputs						Address	Mode
E	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K		
F	X	L	X	X	L-H	N/A	Deselected
F	L	H	H	H	L-H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
F	L	H	L	H	L-H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
F	L	H	H	L	L-H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
F	L	H	L	L	L-H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
T	L	X	X	X	L-H	External address	Read cycle, begin burst
T	H	L	X	L	L-H	External address	Write cycle, begin burst
T	H	L	X	H	L-H	External address	Read cycle, begin burst
X	H	H	L	L	L-H	Next address	Write cycle, continue burst
X	H	H	L	H	L-H	Next address	Read cycle, continue burst
X	H	H	H	L	L-H	Current address	Write cycle, suspend burst
X	H	H	H	H	L-H	Current address	Read cycle, suspend burst

Asynchronous Truth Table[9, 11, 13]

E	Input/Output	Mode
T	Data Out (DQ_0 – DQ_8)	Read
F	High Z	Read
X	High Z, Data In (DQ_0 – DQ_8)	Write
X	High Z	Deselected

Notes:
9. X means Don't Care.
10. All inputs except $\overline{E}$ must meet set-up and hold times for the low-to-high transition of clock (K).
11. E represents CE_0 and $\overline{CE}_1$. T implies $\overline{CE}_1$ = L and CE_0 = H; F implies $\overline{CE}_1$ = H or CE_0 = L.
12. Wait states are inserted by suspending burst.
13. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time and held high through the input data hold time.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
7.5	CY7B175–7JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B175–7NC	N67	TBD	
8.5	CY7B175–8JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B175–8NC	N67	TBD	
11.5	CY7B175–11JC	J67	44-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B175–11NC	N67	TBD	
	CY7B175–11LC	L67	44-Square Leadless Chip Carrier	
	CY7B175–11LMB	L67	44-Square Leadless Chip Carrier	Military

Document #: 38–A–00043