8K × 8 Bit Electrically Erasable PROM

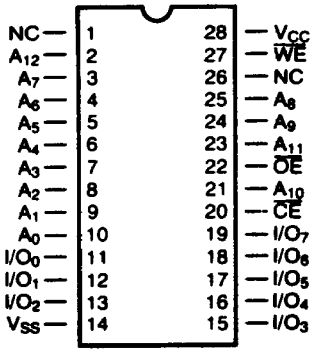
FEATURES

- **Fast Read Access Time: 250ns**
- **5 Volt-Only Operation – Including Write**
- **Fast Nonvolatile Write Cycle: 10ms Max.**
  - **Automatic Write Timeout**
  - **Internally Latched Data**
  - **Internally Latched Address**
  - **Automatic Erase Before Write**
  - **$\overline{\text{DATA}}$ Polling Status Indicator**
- **Automatic Page Write – 1 to 32 Bytes in 10ms Max.**
- **On-Chip False Write Protection**
- **TTL Compatible Inputs and Outputs**
- **10,000 Rewrites per Byte**
- **10 Year Data Retention**
- **JEDEC Approved Byte Wide Memory Pinout**

The BR2864A is a full featured 8,192 × 8 bit electrically erasable programmable read only memory (E^2PROM). It is remarkably easy to use, operating from a single 5-volt power supply and utilizing read and write cycle timing very similar to that of a static RAM. The internally self-timed nonvolatile write cycle latches both address and data to provide a free system bus during the write period. The BR2864A incorporates an automatic and transparent byte erase cycle in its byte write operation, completing the erase/write cycle in a maximum of 10ms.

The device is exceptionally system friendly, incorporating a device status indicator and a fully automatic 32-byte page write feature. $\overline{\text{DATA}}$ polling is provided to maximize device versatility and

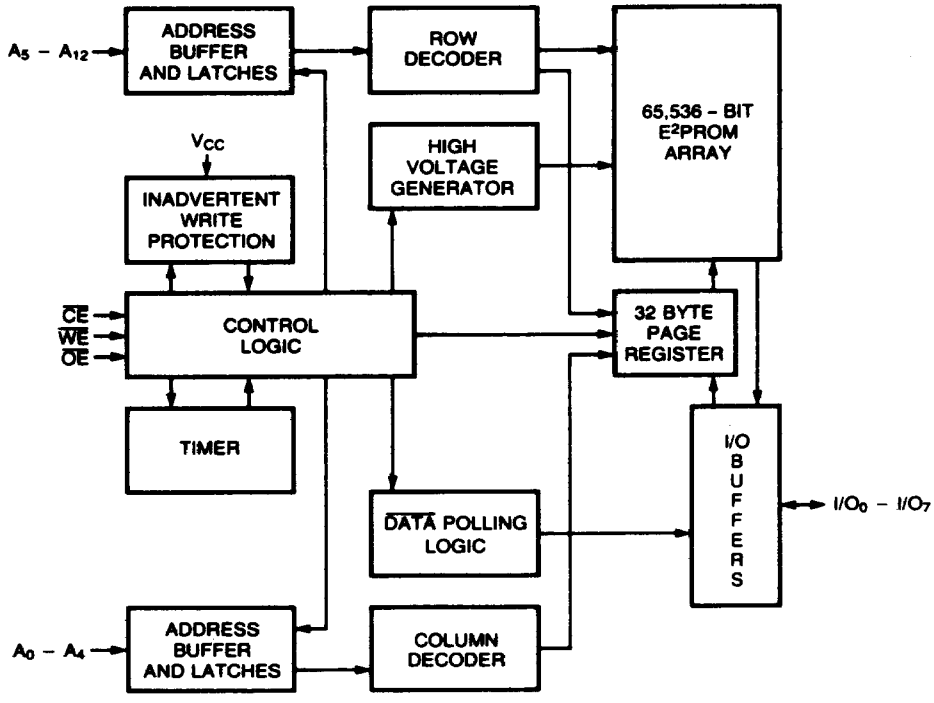
PIN CONFIGURATION



PIN NAMES

$A_0 - A_{12}$	ADDRESS INPUTS
$I/O_0 - I/O_7$	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
NC	NO CONNECT
V_{CC}	+5V
V_{SS}	GROUND

BLOCK DIAGRAM



allow the host system to exploit the actual nonvolatile write cycle time. This is a software technique which is used to observe nonvolatile write cycle completion without requiring external hardware.

The automatic page write feature allows the system to program up to 32 bytes during a single nonvolatile write cycle, providing an effective write speed of at most 312μs/byte. The entire 8K byte memory may be programmed in a maximum of 2.6 seconds when the page write mode is employed.

The BR2864A is the ideal device to use in applications requiring a fast, high density, nonvolatile memory capable of simple in-system modification. Typical applications include robotics, self-calibrating equipment, user programmable firmware, data loggers, security and encryption systems, and remotely reprogrammable machinery.

DEVICE OPERATION

Read Cycle

Data is read from the BR2864A as simply as it is from a static RAM, with $\overline{WE}$ high and $\overline{CE}$ and $\overline{OE}$ low. Since the stored charge which defines the bit state is not affected by read cycles, there is no restriction on the number of times that the BR2864A may be read. Data access times from the last to be asserted of $\overline{CE}$, $\overline{OE}$, or valid address are specified in the Read Cycle Timing section of this data sheet. The I/O pins remain in a high impedance state whenever $\overline{OE}$ or $\overline{CE}$ are high providing a dual line control architecture to eliminate bus contention hazards.

Write Cycle

The BR2864A is designed for exceptional ease of use, integrating data latches, address latches, a high voltage generator, and fully self-timed control logic on-chip so that it writes like a static RAM. Two distinct write cycles are utilized by the BR2864A: one is the write operation performed by the host system and the second is an internal write operation that programs the E^{2}PROM array. In this data sheet the term 'system write cycle' refers to that cycle executed by the system wherein data is written to the BR2864A's internal data latches, while the term 'nonvolatile write cycle' refers to the internal operation wherein data is transfered from these latches into the E^{2}PROM array.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊔	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⊔	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_{IH}	V_{IH}	Read and Write Inhibit	High Z	Active
V_{IL}	15V	⊔	Chip Erase	$D_{IN} = V_{IH}$	Active

During a system write cycle, the address is latched into the internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$ providing that $\overline{OE}$ is a logic '1'. The first rising edge of $\overline{WE}$ or $\overline{CE}$ latches the data into the data latches (see figures 2 and 3).

The nonvolatile write cycle is completed off-line in a fully self-timed operation in two transparent stages. During the first stage, the data then present in the locations to be programmed is erased. The second stage copies the data from the internal latches into the appropriate locations in the E^{2}PROM array for nonvolatile storage.

The E^{2}PROM memory array is not accessible while the nonvolatile write cycle is in progress. Thus neither a read nor a system write operation should be attempted until the nonvolatile write cycle is completed, except that the device may be polled to determine whether the write cycle is complete (see $\overline{DATA}$ Polling).

Automatic Page Write

The BR2864A contains a 32-byte temporary (volatile) buffer which allows the user to simultaneously program from one to 32 bytes in a page during a single 10ms (max) nonvolatile write cycle without any special setup or software procedures. This can effectively reduce the byte write time by a factor of 32. The device will begin its nonvolatile write cycle from 300 to 600 μs (t_{PL}) after the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). At this point, the device commences a nonvolatile write cycle and copies data from each of the latches which were updated into the designated E^{2}PROM locations (see Endurance and Data Retention section). Thus, all bytes to be programmed during an automatic page write cycle must be written into the page buffer within t_{PL} minimum to guarantee that they are transferred into the E^{2}PROM array.

The 32-byte page into which the data will be written is specified by the most significant bits of the address (A_5-A_{12}) presented during the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). The byte within the specified page is identified by the five least significant bits of the address (A_0-A_4) presented during the first and subsequent system write cycles. Bytes may be written into the page in any order. If data is written more than once to the same byte in the temporary buffer during a single page load operation, then the most recently written data will be valid.

If a read operation is attempted during loading of the page buffer, the buffer load cycle is not affected. However, that read cycle will be interpreted as a $\overline{DATA}$ polling cycle.

$\overline{DATA}$ Polling

$\overline{DATA}$ polling is a software method of detecting the end of a nonvolatile write cycle. This is accomplished by allowing the system to monitor the device status via system busses using a simple read and compare operation. $\overline{DATA}$ polling does not require any external hardware. During the nonvolatile write cycle the most significant bit of the last byte written to the BR2864A is inverted and routed to the output buffer. The I/O pins remain in a high impedance state unless a read command is issued to the device by the system. In this event, an inverted most significant bit will be available at I/O_7 (I/O_0-I/O_6 are indeterminate) and, consequently, a comparison of bit 7 of the data read from the BR2864A with bit 7 of the last byte written will indicate unequal values. Once the nonvolatile write cycle is completed, the true data will be accessed with a normal read command.

False Write Protection

Three mechanisms are designed into the BR2864A to protect the device from inadvertent write commands during power supply transitions and system noise periods.

V_{CC} Level Detection

A sensor on-board the BR2864A monitors the supply voltage level and disables the internal write circuitry whenever V_{CC} is less than 4.0V (V_{WI}). This serves to protect the data integrity while allowing the device to tolerate an erratic control bus during power transitions, brownouts and blackouts.

Noise Protected $\overline{WE}$

A noise filter designed into the $\overline{WE}$ input ensures that a write pulse of less than 20ns duration will not activate a write cycle.

Write Inhibit Logic

Logical inadvertent write protection is provided to the system by ensuring that the application of a logic '0' to $\overline{OE}$ or a logic '1' to $\overline{CE}$ or $\overline{WE}$ will inhibit the device's internal write circuitry.

Chip Erase

All data in the BR2864A can be erased by bringing $\overline{OE}$ to 15V while simultaneously bringing $\overline{WE}$ low and holding all data inputs high. Following the erase cycle all storage locations will contain a logic '1'.

Standby

Power consumption may be reduced by approximately 55% by deselecting the device with a logic '1' applied to $\overline{CE}$.

Endurance and Data Retention

The BR2864A is designed for applications requiring up to 10,000 rewrites per E²PROM byte and ten years of secure data retention. This means that each byte may be reliably rewritten 10^4 times without degrading device operation, and that data will remain valid after the last rewrite for ten years with or without power applied.

The latches in the automatic page write buffer include corresponding flag bits which are set when a given latch is written. In the event that a nonvolatile write cycle occurs with less than 32 bytes of data, only those bytes in the E²PROM array corresponding to the locations in the buffer which were actually written will be reprogrammed. This feature eliminates unnecessary cycling and ensures maximum endurance. This is in contrast to some competing E²PROM devices which reprogram the full page of nonvolatile locations independent of the number of page latches actually written to. This wastes cell cycles and may substantially reduce device endurance and, consequently, system reliability.

ABSOLUTE MAXIMUM RATINGS [1]

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... −65°C to +125°C
Voltage on any Pin with Respect to Ground (Except $\overline{OE}$) [2] ... −1.0V to +6.0V
Voltage on $\overline{OE}$ Pin with Respect to Ground [2] ..... −1.0V to +22.0V
DC Output Current ..... −5mA

Operating Range

Range	Ambient Temperature
Standard	0°C to 75°C

DC OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400μA
V_{WI}	V_{CC} Voltage for Write Inhibit	3.5	4.0	V	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to 5.5V
I_{LO}	Output Leakage Current		±10	μA	V_{OUT} = 0 to 5.5V
I_{CC}	V_{CC} Current — Active		110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; All I/Os open; Other Inputs = 5.5V
I_{SB}	V_{CC} Current — Standby		50	mA	$\overline{CE}$ = V_{IH}; $\overline{OE}$ = V_{IL}; All I/Os open; Other Inputs = 5.5V

CAPACITANCE

T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
$C_{I/O}$	Input/Output Capacitance		10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance		10	pF	V_{IN} = 0V

Notes:

1. Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages higher than the rated maxima.
3. AC conditions of test:
   - Input Pulse Levels: 0.45V to 2.4V
   - Input Rise and Fall Times: ≤20 nsec
   - Timing Reference Levels: 0.8V and 2.0V
   - Output Load: 1 TTL Gate and C_L = 100 pF
4. This parameter also defines the minimum time that $\overline{CE}$ and $\overline{WE}$ must be asserted simultaneously in order to ensure that the write cycle occurs.
5. $\overline{WE}$ is noise protected. A write pulse of less than 20ns duration will not activate a write cycle.
6. There is no intrinsic value for this parameter, i.e., $\overline{CE}$ and $\overline{WE}$ may be asserted indefinitely. However, if both $\overline{CE}$ and $\overline{WE}$ are asserted upon the expiration of t_{PL}, then the input data currently present will be automatically latched into the addressed buffer and the nonvolatile write portion of the cycle will commence.
7. $\overline{DATA}$ Polling: DATA lines go to Low-Z, with $\overline{DATA}$ out on I/O_7, for $\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}.
8. This timing diagram shows the storage of two bytes of data. One to 32 bytes may be loaded in a single write cycle. (See Automatic Page Write section.)

AC CHARACTERISTICS [3]

T_A = 0°C to 70°C V_{CC} = 5V ± 5%

Read Cycle – See Figure 1.

Symbol	Parameter	BR2864A-250 Limits		BR2864A-300 Limits		BR2864A-350 Limits		BR2864A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		80		80		120		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

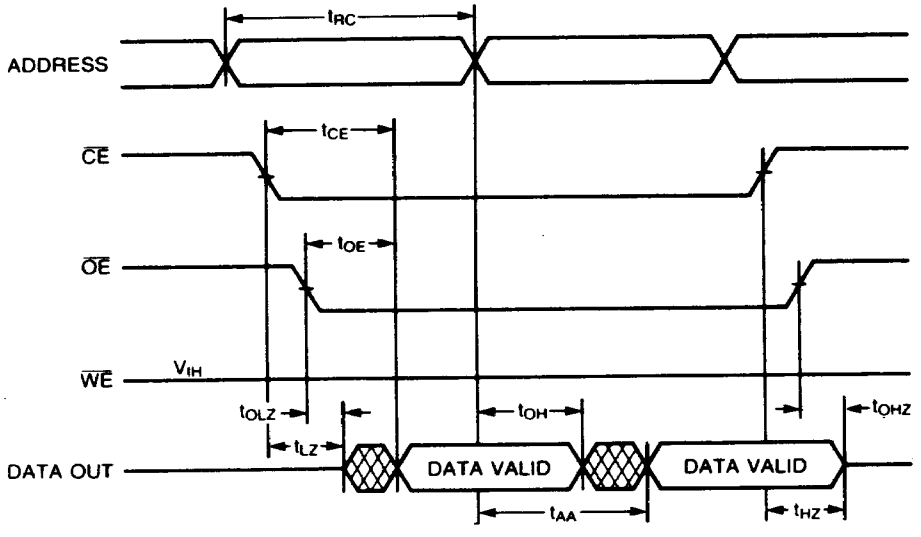


Figure 1. Read Cycle

Write Cycle – See Figures 2 and 3.

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_{NW}	Nonvolatile Write Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	125		ns
t_{CS}	Chip Enable or Write Setup Time	0		ns
t_{CH}	Chip Enable or Write Hold Time	0		ns
t_{CW} [4]	Chip Enable Pulse Width	150	Note 6	ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP} [5]	Write Enable Pulse Width	150	Note 6	ns
t_{DL}	Data Latch Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{PL}	Page Load Time	300	600	μs
t_{WC}	Byte Load Cycle	1	25	μs

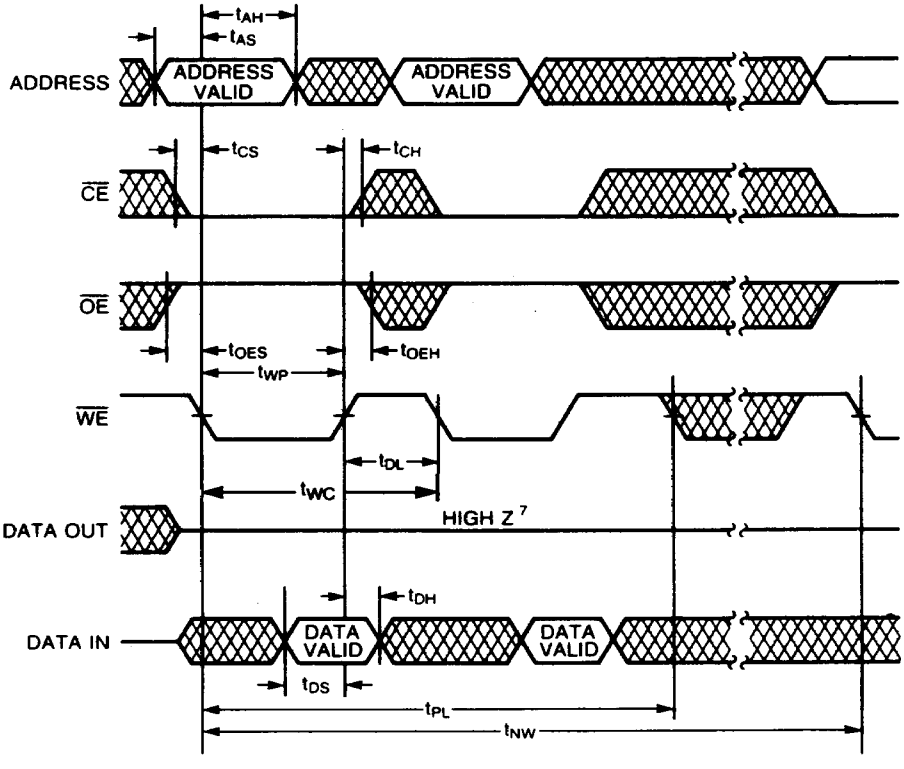


Figure 2. $\overline{WE}$ Controlled Write Cycle [8]

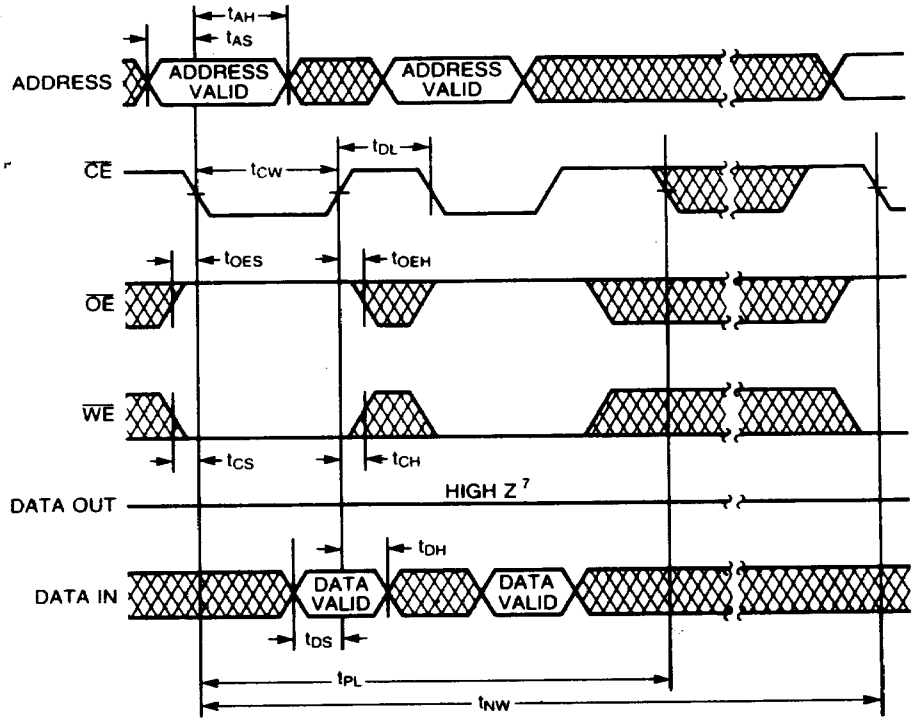


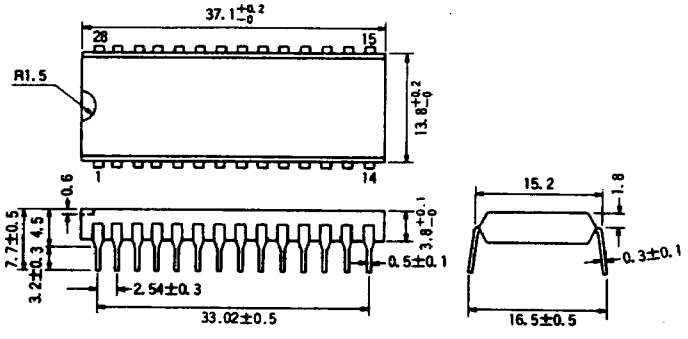
Figure 3. $\overline{CE}$ Controlled Write Cycle [8]

ORDERING INFORMATION

Part Number	Access Time (ns)	Temperature Range	Operating Supply Variation (V)	Package
BR2864A -250 BR2864AF-250	250	0 - 70°C	4.75 - 5.25	DIP28 MF28
BR2864A -300 BR2864AF-300	300	0 - 70°C	4.75 - 5.25	DIP28 MF28
BR2864A -350 BR2864AF-350	350	0 - 70°C	4.75 - 5.25	DIP28 MF28
BR2864A -450 BR2864AF-450	450	0 - 70°C	4.75 - 5.25	DIP28 MF28

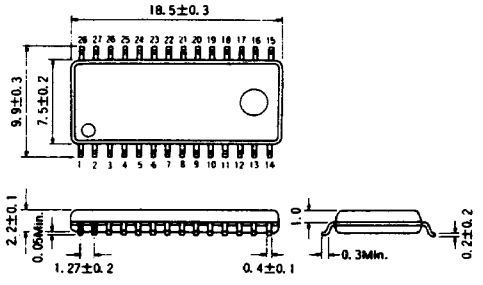
PACKAGE INFORMATION: Unit in mm.

BR2864A



DIP28pin

BR2864AF



MF28 pin

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