512K x 32 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-94611
- MIL-STD-883

FEATURES

- Operation with single 5V supply
- High speed: 17, 20, 25 and 35ns
- Built in decoupling caps for low noise
- Organized as 512Kx32 , byte selectable
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Theta JC =1.00°C/w
- **Future offerings**
  - 3.3V Power Supply
  - 15 ns Ultra High Speed

OPTIONS MARKINGS

- Timing

17ns	-17
20ns	-20
25ns	-25
35ns	-35
45ns	-45
55ns	-55

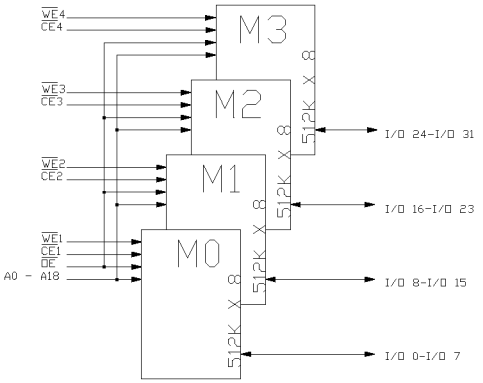
- Package

Ceramic Quad Flatpack	Q	No.702
Pin Grid Array	P	No.904

GENERAL DESCRIPTION

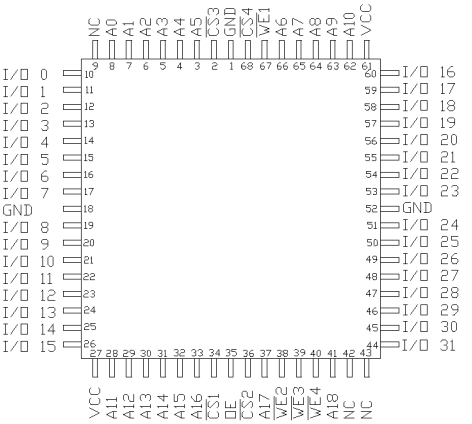
The Austin Semiconductor, Inc. AS8S512K32 is a 16 Megabit CMOS SRAM Module organized as 512Kx32 bits. The AS8S512K32 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

This military temperature grade product is ideally suited for military and space applications.

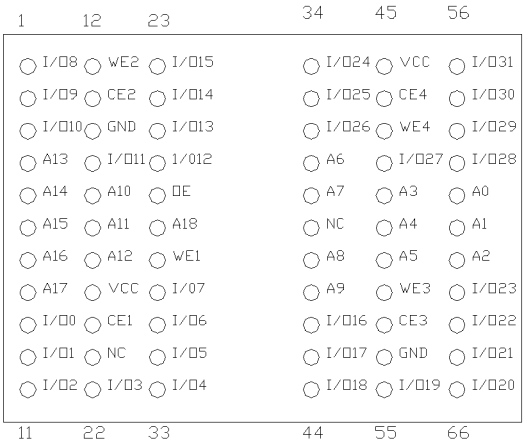


PIN ASSIGNMENT
(Top View)

68 Lead CQFP (Q)



66 Lead PGA (P)



TRUTH TABLE

MODE	OE\	CE\	WE\	I/O	POWER
Read	L	L	H	D_{OUT}	ACTIVE
Write	X	L	L	D_{IN}	ACTIVE
Standby	X	H	X	High Z	STANDBY

For more products and information please visit our web site at
www.austinsemiconductor.com

ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-.5V to +7V
Storage Temperature.....-65°C to +150°C
Short Circuit Output Current(per I/O).....20mA
Voltage on Any Pin Relative to Vss.....-.5V to Vcc+1V
Maximum Junction Temperature**.....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (logic 1) Voltage		V_{IH}	2.2	V_{CC}+.5	V	1
Input Low (logic 1) Voltage		V_{IL}	-0.5	0.8	V	1,2
Input Leakage Current $_{ADD,OE}$	0V<V_{IN}<V_{CC}	I_{LI1}	-10	10	µA	
Input Leakage Current $_{WE, CE}$		I_{LI2}	-10	10	µA	
Output Leakage Current $_{I/O}$	Output(s) Disabled 0V<V_{OUT}<V_{CC}	ILO	-10	10	µA	
Output High Voltage	I_{OH} = 4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX							
DESCRIPTION	CONDITIONS	SYMBOL	-17	-20	-25	-35	-45	-55	UNITS	NOTES
Power Supply Current: Operating	CE\<VIL; VCC = MAX f = MAX = 1/ tRC (MIN) Outputs Open	Icc	700	650	600	570	570	550	mA	3,13
Power Supply Current: Standby	CE\>VIH; VCC = MAX f = MAX = 1/ tRC (MIN) Outputs Open	I_{SBT1}	240	240	190	190	150	150	mA	3, 13
CMOS Standby	VIN = VCC - 0.2V, or VSS +0.2V VCC=Max; f = 0Hz	I_{SBT2}	80	80	80	80	80	80	mA	

CAPACITANCE (V_{IN} = 0V, f = 1MHz, T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS
C_{ADD}	A0 - A18 Capacitance	50	pF
C_{OE}	OE\ Capacitance	50	pF
C_{WE}, C_{CE}	WE\ and CE\ Capacitance	20	pF
C_{IO}	I/O 0- I/O 31 Capacitance	20	pF

NOTE:
1. This parameter is sampled.
2. 32 bit configuration.

AC TEST CONDITIONS

Test Specifications

Input pulse levels.....Vss to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figure 1

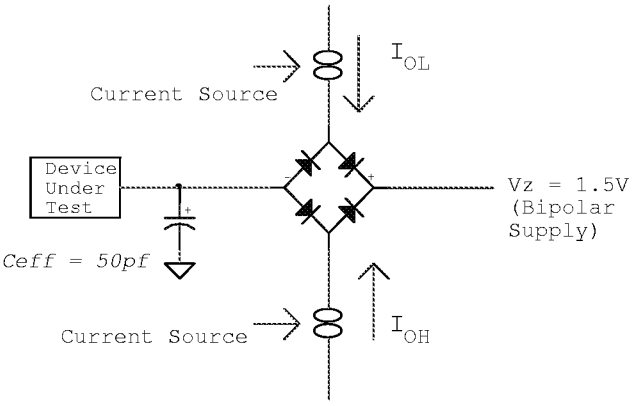


Figure 1

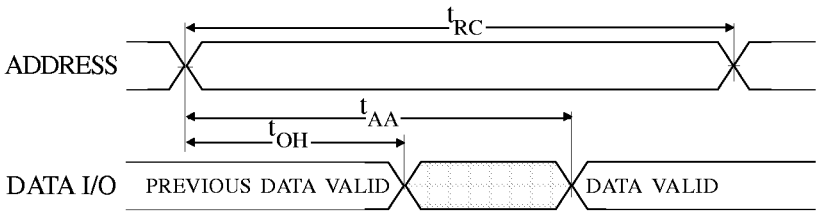
NOTES:
Vz is programable from -2V to + 7V.
I_{OL} and I_{OH} programmable from 0 to 16 mA.
Vz is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

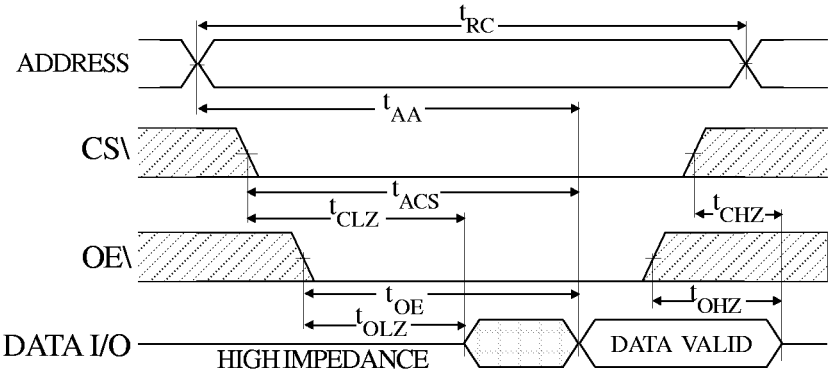
(NOTES 5) (-55°C≤T_A≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION	SYMBOL	-17		-20		-25		-35		-45		-55		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE															
READ cycle time	^tRC	17		20		25		35		45		55		ns	
Address access time	^tAA		17		20		25		35		45		55	ns	
Chip enable access time	^tACE		17		20		25		35		45		55	ns	
Output hold from address change	^tOH	2		2		2		2		2		2		ns	
Chip enable to output in Low-Z	^tLZCE	2		2		2		2		2		2		ns	4,6,7
Chip enable to output in High-Z	^tHZCE		9		10		12		15		20		20	ns	4,6,7
Output enable access time	^tAOE		9		10		12		15		20		20	ns	
Output enable to output in Low-Z	^tLZOE	0		0		0		0		0		0		ns	4,6
Output disable to output in High-Z	^tHZOE		12		12		12		15		20		20	ns	4,6
WRITE CYCLE															
WRITE cycle time	^tWC	17		20		25		35		45		55		ns	
Chip enable to end of write	^tCW	15		15		17		20		25		25		ns	
Address valid to end of write	^tAW	15		15		17		20		25		25		ns	
Address setup time	^tAS	2		2		2		2		2		2		ns	
Address hold from end of write	^tAH	1		1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	15		15		17		20		25		25		ns	
WRITE pulse width	$^tWP2$	15		15		17		20		25		25		ns	
Data setup time	^tDS	12		10		12		15		20		20		ns	
Data hold time	^tDH	0		0		0		0		0		0		ns	
Write disable to output in Low-z	^tLZWE	2		2		2		2		2		2		ns	4,6,7
Write enable to output in High-Z	^tHZWE		9		11		13		15		15		15	ns	4,6,7

READ CYCLE NO. 1

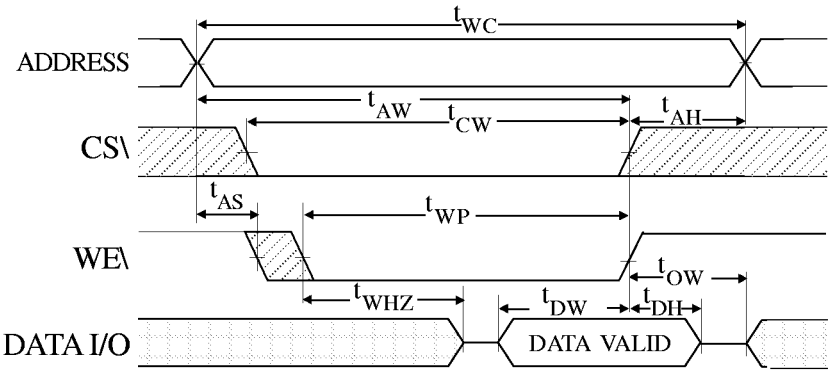


READ CYCLE NO. 2



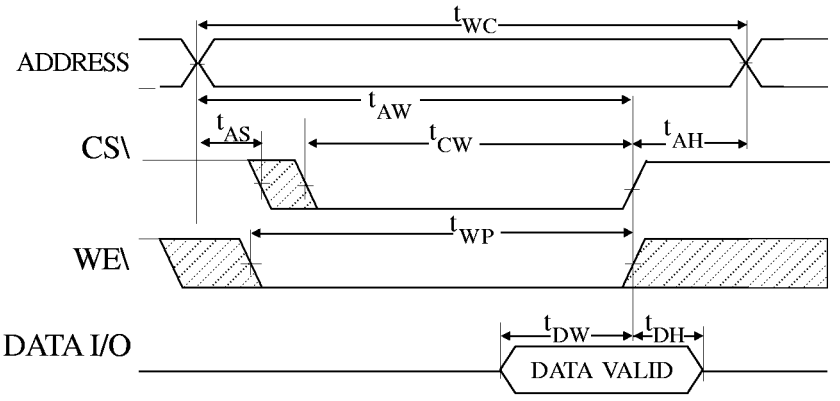
WRITE CYCLE NO. 1

(Chip Enable Controlled)



WRITE CYCLE NO. 2

(Write Enable Controlled)



NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates.

$$\text{unloaded, and f= } \frac{1}{t_{RC(MIN)}} \text{ Hz}$$

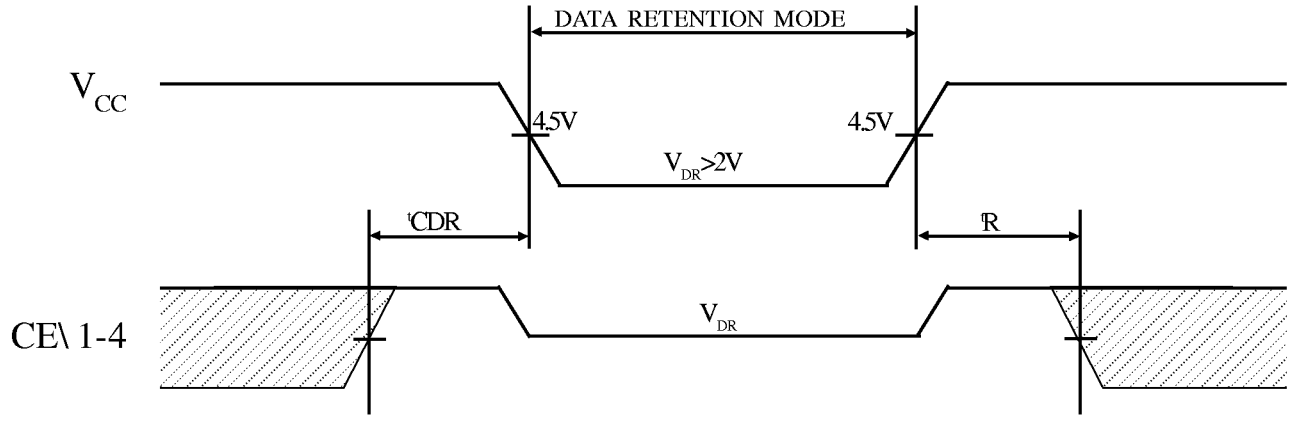
The specified value applies with the outputs

4. This parameter guaranteed but not tested.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L= 5pF as in Fig. 2. Transition is measured +/- 200 mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCE}, is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. t_{RC} = READ cycle time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.
13. I_{CC} is for 32 bit mode.

LOW POWER CHARACTERISTICS

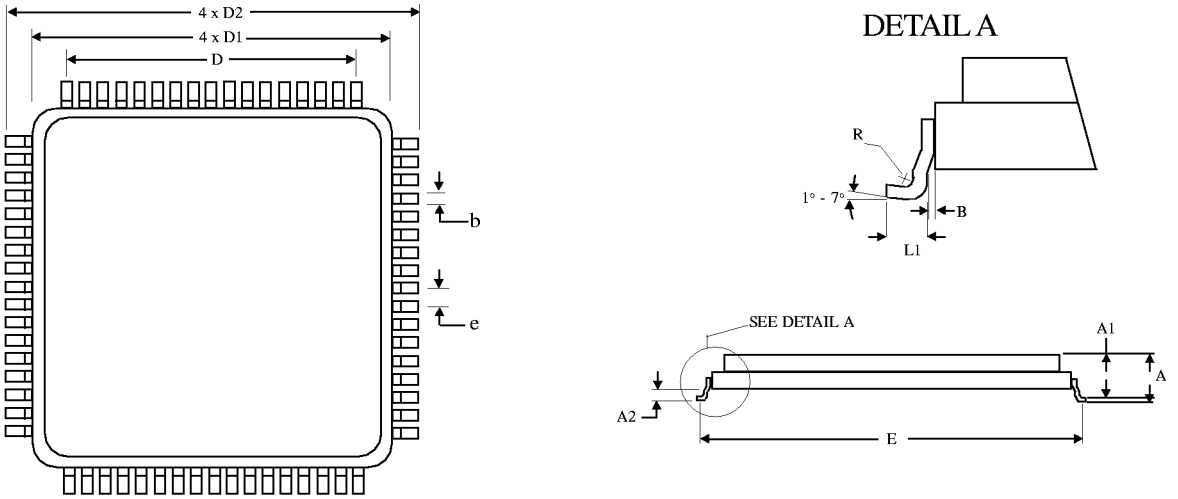
DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		V	
Data Retention Current	All Inputs @ Vcc ± 0.2V or Vss ± 0.2V, CE\ = Vcc ± 0.2V	V_{CC} = 2V	I_{CCDR}		20	mA	
		V_{CC} = 3V	I_{CCDR}		28	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0		ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

LOW V_{CC} DATA RETENTION WAVEFORM



MECHANICAL DEFINITIONS*

ASI Case #702 (Package Designator Q)
SMD 5962-94611, Case Outline M

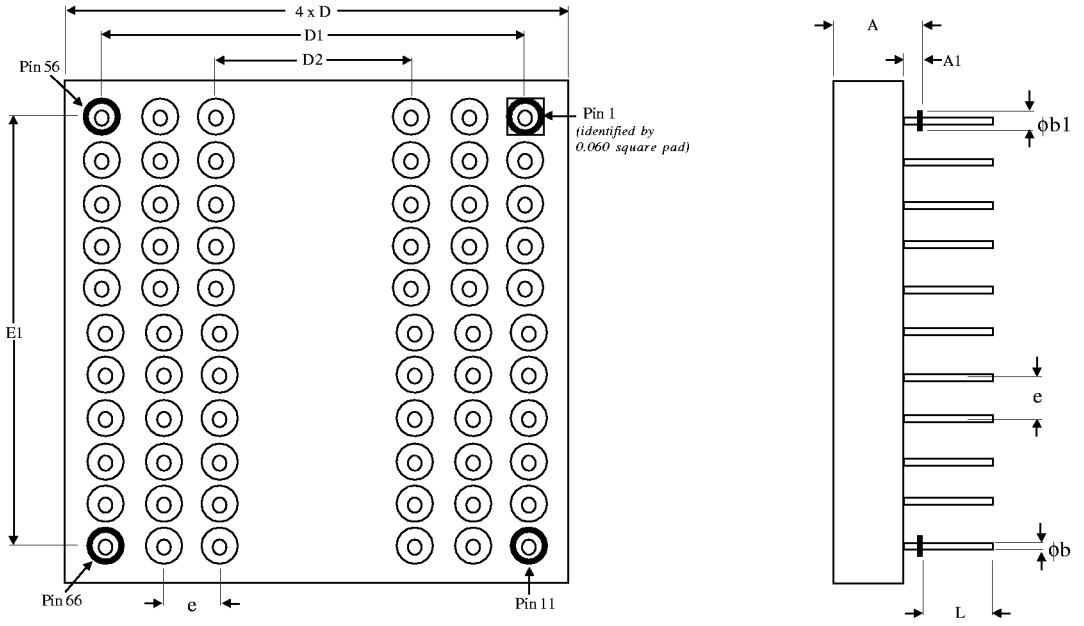


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.000	0.020
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.005	---
L1	0.035	0.045

**All measurements are in inches.*

MECHANICAL DEFINITIONS*

ASI Case #904 (Package Designator P)
SMD 5962-94611, Case Outline T



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.144	0.181
A1	0.025	0.035
ϕb	0.016	0.020
ϕb1	0.045	0.055
D	1.065	1.085
D1/E1	1.000 TYP	
D2	0.600 TYP	
e	0.100 TYP	
L	0.145	0.155

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS8S512K32Q-25/XT

Device Number	Package Type	Speed ns	Process
AS8S512K32	Q	-17	/*
AS8S512K32	Q	-20	/*
AS8S512K32	Q	-25	/*
AS8S512K32	Q	-35	/*
AS8S512K32	Q	-45	/*
AS8S512K32	Q	-55	/*

EXAMPLE: AS8S512K32P-25/XT

Device Number	Package Type	Speed ns	Process
AS8S512K32	P	-17	/*
AS8S512K32	P	-20	/*
AS8S512K32	P	-25	/*
AS8S512K32	P	-35	/*
AS8S512K32	P	-45	/*
AS8S512K32	P	-55	/*

*AVAILABLE PROCESSES

CT = Commercial Temperature Range	0°C to +70°C
IT = Industrial Temperature Range	-40°C to +85°C
AT = Automotive Temperature Range	-40°C to +125°C
XT = Extended Temperature Range	-55°C to +125°C
833C = Full Military Processing	-55°C to +125°C