VX1138/VX1136

HIGH QUALITY PROGRESSIVE VIDEO PROCESSOR AND TIMING CONTROLLER

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1 OVERVIEW

1.1 DESCRIPTION

VX1138 is a progressive video processor IC, consists of video processor, 3-D deinterlacer, picture enhancement engine, the scaling engine specially designed for video apps, T-con for LCD panel timing control. It receives digitized interlaced video stream (BT. 656 or bt. 601) from video decoder or MPEG video decoder. It also can receive RGB 24-bit video input. VX1138 can perform high quality picture enhancement such as video noise reduction, sharpening, black-level extension, and Gamma correction, and converts it into non-interlaced formats for direct display on progressive devices, such as LCD displays, DTV, projectors, or PC monitors. Its output resolution covers 320x240, 640x480, 720x480 800x480, 800x600, 1024x768, 1280x720, 1280x1024, 1600x1200, 1920x1080. VX1138 provides theater quality progressive scan video with VXIS's innovated *Motion Adaptive-3D Deinterlace Algorithm*, 3-2 pull down with automatic film mode detection, *Edge Preserving Pixel Interpolation*, frame-rate conversion, synchronization regeneration, and automatic source mode detection. The font-based on-screen-display (OSD), and universal programmable timing control makes it become a highly integrated, most cost-efficient LCD video processor.

1.2 APPLICATION

- Portable DVD
- Car TV
- Small/middle size LCD TV
- photoframe
- surveillance
- Multimedia panel

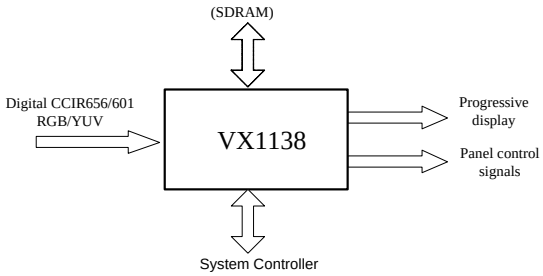


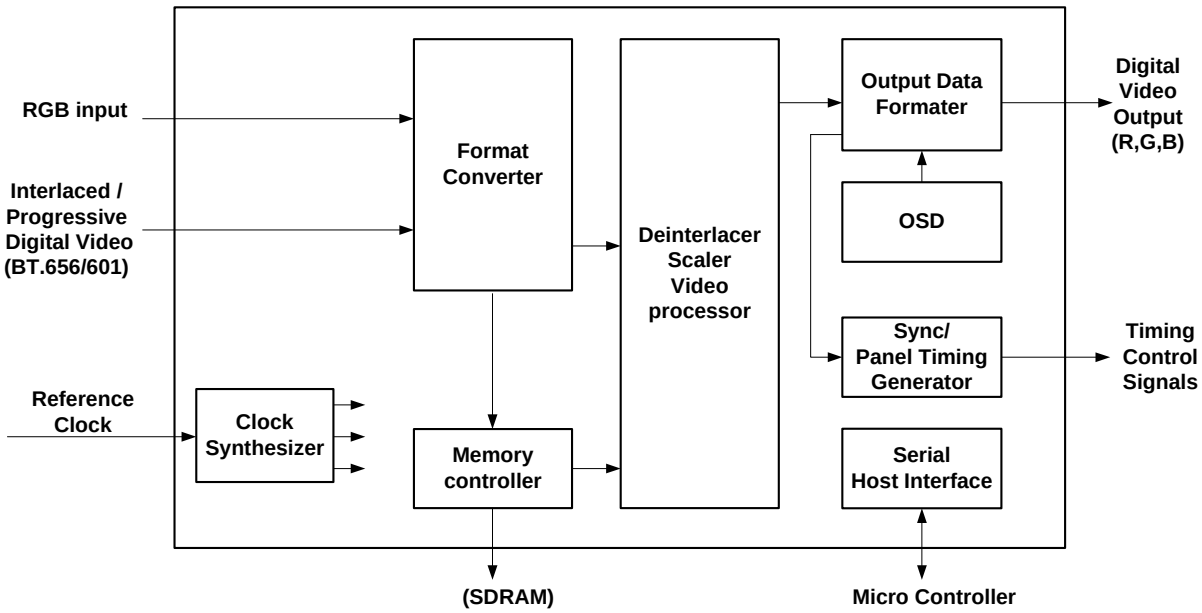
Figure 1.1 Interface for VX1138

1.3 FEATURES

- Support Various Digital Video Input Formats
  - 8-bit interlace ITU-R BT.656
  - 8-bit progressive 656
  - 8-Bit ITU-R BT.601 + Horizontal Sync + Vertical Sync
  - 8-bit Bayer format CCD input, up to 1280x1024
  - 24-bit RGB/YUV progressive input
  - 16-bit Y/UV input
- Support Various Digital Video Output Formats
  - 24/18/16-Bit RGB + Horizontal Sync + Vertical Sync
  - 24/18/16-Bit 4:4:4 YUV + Horizontal Sync + Vertical Sync
  - 16-Bit 4:2:2 YUV + Horizontal Sync + Vertical Sync
  - 8-bit YUV progressive BT.656
- Frame rate up-conversion to 60 Hz for PAL & SECAM
- Motion-Adaptive 3D(with SDRAM) or 2D(without SDRAM) Deinterlace
- Edge-Preserving Pixel Interpolation
- Automatic Video Source Detection
- Embedded Scaling Engine, Supporting Output Resolution 320x240, 640x480, 720x480 800x480, 800x600, 1024x768, 1280x720, 1280x1024, 1600x1200, 1920x1080, …..
- Programmable Zoom/Shrink Scale with Anamorphic / Panoramic /4:3 / 16:9 Zoom Support
- Brightness, Contrast, Saturation, and Hue Adjustment
- Color Transient Improvement, Adaptive Black-Level Extension, Skin Tone Enhancement.
- Video Noise Reduction
- Frequency Directive Picture Sharpening
- 3-Channel 10-Bit Build-In Color gamma Look-Up Table for Video Fine-Tune
- Host Interface Compatible with Two-Wire IIC, Serial Interface
- OSD with 128 Build-in and 64 Programmable Font and Attribute Table, 16 Colors at same Time from 16,777,216-Color Template, Blinking, and Blending
- R/G/B output port swap & rotation control
- R/G/B input port swap & rotation control
- 8 pins of programmable panel timing control signals
- One 20 MHz crystal, or from CCIR input clock or from RGB input clock as internal reference clock
- 1.8V / 3.3V power supply with 5V tolerant digital I/O

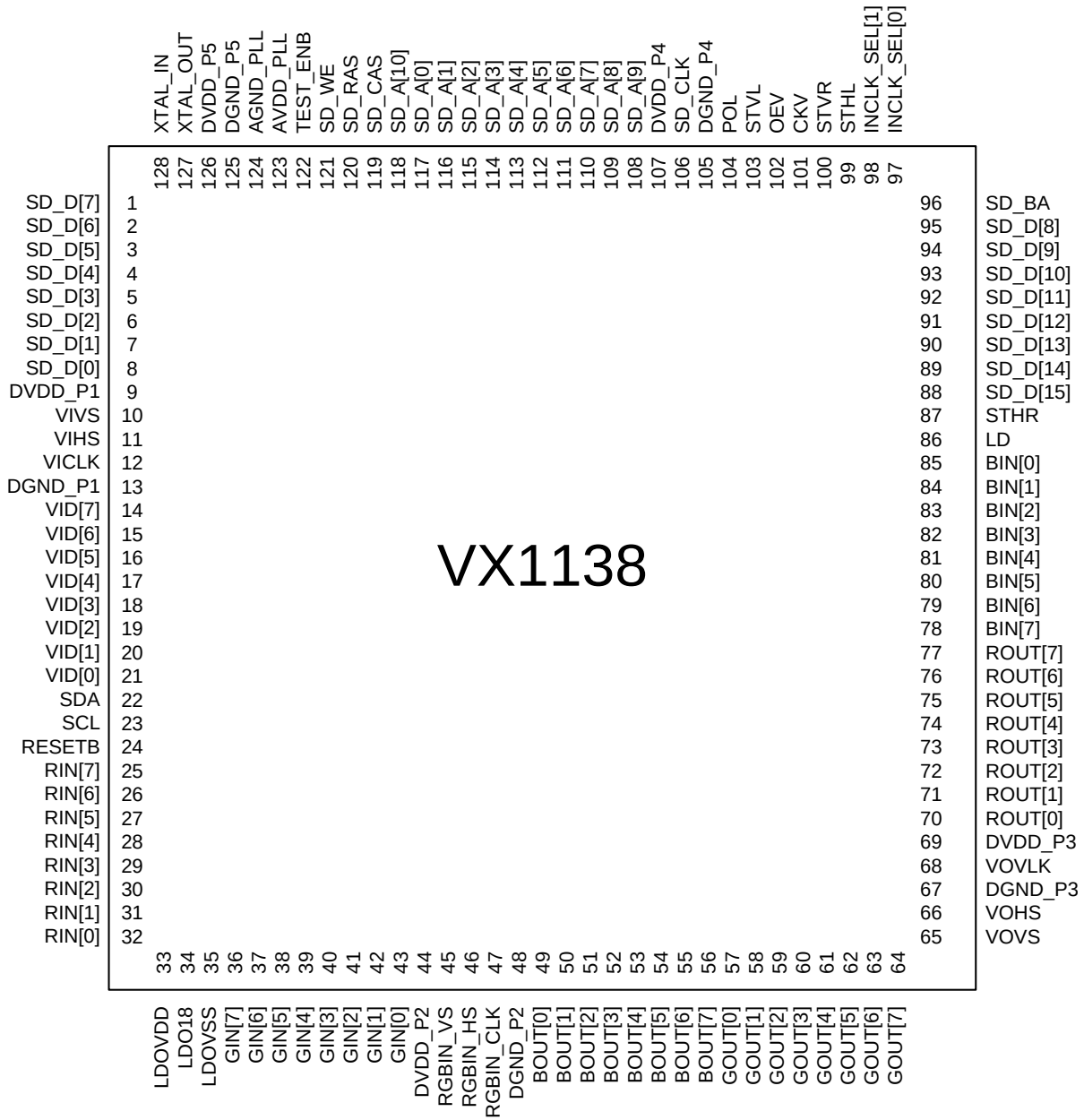
1.4 BLOCK DIAGRAM

1.4.1 BLOCK DIAGRAM OF VX1138

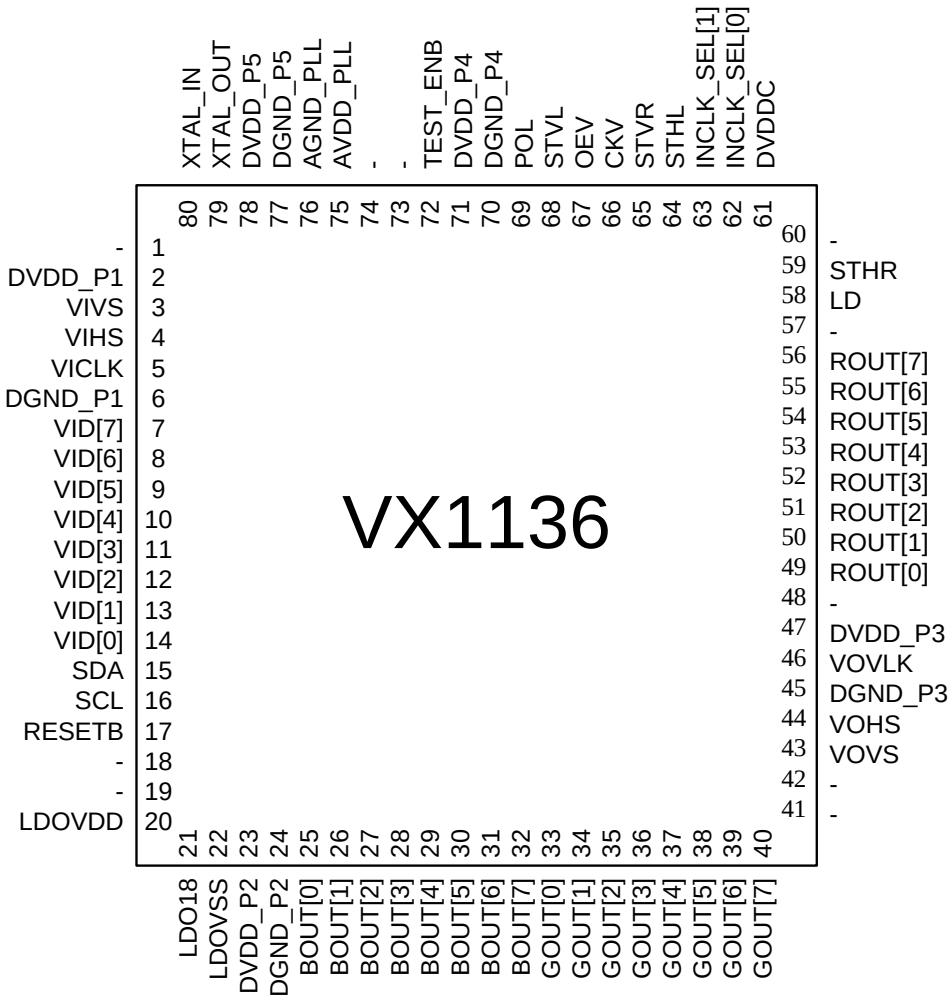


1.5 PINOUT DIAGRAM

1.5.1 PINOUT DIAGRAM OF VX1138



1.5.2 PINOUT DIAGRAM OF VX1136



1.6 PIN ASSIGNMENT

1.6.1 PIN ASSIGNMENT OF VX1138

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name_	Pin #	Pin Name
1	SD_D[7]	33	LDO_VDD	65	VOVS	97	INCLK_SEL[0]
2	SD_D[6]	34	LDO_V18	66	VOHS	98	INCLK_SEL[1]
3	SD_D[5]	35	LDO_VSS	67	DGND_P	99	STHL
4	SD_D[4]	36	GIN[7]	68	VOCLK	100	STVR
5	SD_D[3]	37	GIN[6]	69	DVDD_P	101	CKV
6	SD_D[2]	38	GIN[5]	70	ROUT[0]	102	OEV
7	SD_D[1]	39	GIN[4]	71	ROUT[1]	103	STVL
8	SD_D[0]	40	GIN[3]	72	ROUT[2]	104	POL
9	DVDD_P	41	GIN[2]	73	ROUT[3]	105	DGND_P
10	VIVS	42	GIN[1]	74	ROUT[4]	106	SD_CLK
11	VIHS	43	GIN[0]	75	ROUT[5]	107	DVDD_P
12	VICLK	44	DVDD_P	76	ROUT[6]	108	SD_A[9]
13	DGND_P	45	RGBIN_VS	77	ROUT[7]	109	SD_A[8]
14	VID[7]	46	RGBIN_HS	78	BIN[0]	110	SD_A[7]
15	VID[6]	47	RGBIN_CLK	79	BIN[1]	111	SD_A[6]
16	VID[5]	48	DGND_P	80	BIN[2]	112	SD_A[5]
17	VID[4]	49	BOUT[0]	81	BIN[3]	113	SD_A[4]
18	VID[3]	50	BOUT[1]	82	BIN[4]	114	SD_A[3]
19	VID[2]	51	BOUT[2]	83	BIN[5]	115	SD_A[2]
20	VID[1]	52	BOUT[3]	84	BIN[6]	116	SD_A[1]
21	VID[0]	53	BOUT[4]	85	BIN[7]	117	SD_A[0]
22	SDA	54	BOUT[5]	86	LD	118	SD_A[10]
23	SCL	55	BOUT[6]	87	STHR	119	SD_CAS
24	RESETB	56	BOUT[7]	88	SD_D[15]	120	SD_RAS
25	RIN[7]	57	GOUT[0]	89	SD_D[14]	121	SD_WE
26	RIN[6]	58	GOUT[1]	90	SD_D[13]	122	TEST_ENB
27	RIN[5]	59	GOUT[2]	91	SD_D[12]	123	AVDD_C
28	RIN[4]	60	GOUT[3]	92	SD_D[11]	124	AGND_C
29	RIN[3]	61	GOUT[4]	93	SD_D[10]	125	DGND_P
30	RIN[2]	62	GOUT[5]	94	SD_D[9]	126	DVDD_P
31	RIN[1]	63	GOUT[6]	95	SD_D[8]	127	XTAL_OUT
32	RIN[0]	64	GOUT[7]	96	SD_BA	128	XTAL_IN

1.6.2 PIN ASSIGNMENT OF VX1136

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name_	Pin #	Pin Name
1	-	21	LDO18	41	-	61	DVDD_C
2	DVDD_P	22	LDOVSS	42	-	62	INCLK_SEL[0]
3	VIVS	23	DVDD_P	43	VOVS	63	INCLK_SEL[1]
4	VIHS	24	DGND_P	44	VOHS	64	POLSTHL
5	VICLK	25	BOUT[0]	45	DGND_P	65	STVR
6	DGND_P	26	BOUT [1]	46	VOCLK	66	CKV
7	VID[7]	27	BOUT [2]	47	DVDD_P	67	OEV
8	VID[6]	28	BOUT [3]	48	-	68	STVL
9	VID[5]	29	BOUT [4]	49	ROUT[0]	69	POL
10	VID[4]	30	BOUT [5]	50	ROUT[1]	70	DGND_P
11	VID[3]	31	BOUT [6]	51	ROUT[2]	71	DVDD_P
12	VID[2]	32	BOUT [7]	52	ROUT[3]	72	TEST_ENB
13	VID[1]	33	GOUT [0]	53	ROUT[4]	73	-
14	VID[0]	34	GOUT [1]	54	ROUT[5]	74	-
15	SDA	35	GOUT [2]	55	ROUT[6]	75	AGND_C
16	SCL	36	GOUT [3]	56	ROUT[7]	76	AGND_C
17	RESETB	37	GOUT [4]	57	-	77	DGND_P
18	-	38	GOUT [5]	58	LD	78	DVDD_P
19	-	39	GOUT [6]	59	STHR	79	XTAL_OUT
20	LDOVDD	40	GOUT [7]	60	-	80	XTAL_IN

1.7 PIN DESCRIPTION

Video Input Pins

Name	Type	Description	Notes
VID [7:0]	I	Digital Video Input Data(BT 656/601)	
VIHS	I	Digital Video Input Horizontal Synchronization	
VIVS	I	Digital Video Input Vertical Synchronization	
VICLK	I	Digital Video Input Clock	
RIN[7:0]	I	Red input data	
GIN[7:0]	I	Green input data	
BIN[7:0]	I	Blue input data	
RGBIN_VS	I	RGB input vertical synchronization	
RGBIN_HS	I	RGB input horizontal synchronization	
RGBIN_CLK	I	RGB input clock	

Video Output Pins

Name	Type	Description	Notes
ROUT [7:0]	O_{TS1}	R/V/Pr Digital Video Output	
GOUT [7:0]	O_{TS1}	G/Y/BT656 Digital Video Output	
BOUT [7:0]	O_{TS1}	B/U/Pb Digital Video Output	
VOHS / GPO1	O_1	Video Output Horizontal Synchronization / GPO1	
VOVS / GPO0	O_1	Video Output Vertical Synchronization / GPO0	
VOCLK	O_2	Video Output Clock / BT656 Output Clock	
STHR	I/O_1	Horizontal start pulse output	
STHL / GPO1	I/O_1	Horizontal start pulse output GPO1	
STVR	I/O_1	Vertical start pulse output	
STVL / GPO0	I/O_1	Vertical start pulse output GPO0	
POL	I/O_1	Polarity inversion control	
LD	I/O_1	Latch control for source driver	
CKV	I/O_1	Shift clock for gate driver	
OEV / GPO2	I/O_1	Output Enable signal for gate driver GPO2	

External SDRAM I/O Pins

Name	Type	Description	Notes
SDRAM_D [15:0]	I/O_1	SDRAM Data Bus	
SDRAM_A [10:0]	O_{T1}	SDRAM Address Bus	
SDRAM_CLK	O_{T2}	SDRAM Clock	
SDRAM _RAS	O_{T1}	SDRAM Row Address Strobe (Active Low)	
SDRAM _CAS	O_{T1}	SDRAM Column Address Strobe (Active Low)	
SDRAM _WE	O_{T1}	SDRAM Write Enable (Active Low)	
SDRAM_BA	O_{T1}	SDRAM Bank	

Miscellaneous I/O Pins

Name	Type	Description	Notes

/RESETB	I_S	Chip Reset (Active Low)
XTAL_OUT	XO	Crystal Output
XTAL_IN	XI	Crystal Input
SDA	I/O_1	Host Interface Serial Data / Address
SCL	I_S	Host Interface Serial Clock
/TEST_ENB	I_{PU}	Test Mode Enable (Active Low)
INCLK_SEL[1:0]	I	reference clock select for internal PLL

Power Pins

Name	Type	Description	Notes
AVDD_C	P_{18}	Analog 1.8V Supply For PLL CORE	Qty: 2
AGND_C	G	Analog Ground For PLL CORE	Qty: 2
DVDD_P	P_{33}	Digital 3.3V Supply For I/O	Qty: 6
DGND_C	G	Digital Ground For CORE	Qty: 7
LDOVDD	P_{33}	3.3V power for LDO	Qty: 1
LDOVSS	G	LDO ground	Qty: 1
LDO18	P_{18}	1.8V output from LDO	Qty: 1

1.8 PACKAGE

- 1138 128-Pin LQFP
- 1136 80-Pin LQFP

2 VIDEO I/O PIN ASSIGNMENT

2.1 DIGITAL VIDEO INPUT ASSIGNMENT

The VX1138 digital video interface is compatible with extensive digital video input and output standard formats mostly used by current video transmission methods. As for input, VX1138 directly supports interlaced 8-bit YUV with (ITU-R BT.656) or without (ITU-R BT.601) embedded synchronization, It also supports progressive 8-bit YUV input and 16-bit Y/UV, 24-bit YUV, 24-bit RGB input.

The pin arrangement for each format is defined in *Table 2.1.*

Table 2.1 Digital Video Input Pin Assignment

Pin Name	I/O Type	Digital Input			
		8-bit YUV	16-bit YUV	24-bit YUV	24-bit RGB
VID [7]	**I**	YUV [7]	Y[7]		
VID [6]	**I**	YUV [6]	Y[6]		
VID [5]	**I**	YUV [5]	Y[5]		
VID [4]	**I**	YUV [4]	Y[4]		
VID [3]	**I**	YUV [3]	Y[3]		
VID [2]	**I**	YUV [2]	Y[2]		
VID [1]	**I**	YUV [1]	Y[1]		
VID [0]	**I**	YUV [0]	Y[0]		
RIN [7]	**I**	-	UV[7]	V[7]	R[7]
RIN [6]	**I**	-	UV[6]	V[6]	R[6]
RIN [5]	**I**	-	UV[5]	V[5]	R[5]
RIN [4]	**I**	-	UV[4]	V[4]	R[4]
RIN [3]	**I**	-	UV[3]	Y[3]	R[3]
RIN [2]	**I**	-	UV[2]	V[2]	R[2]
RIN [1]	**I**	-	UV[1]	V[1]	R[1]
RIN [0]	**I**	-	UV[0]	V[0]	R[0]
GIN [7]	**I**	-		Y[7]	G[7]
GIN [6]	**I**	-		Y[6]	G[6]
GIN [5]	**I**	-		Y[5]	G[5]
GIN [4]	**I**	-		Y[4]	G[4]
GIN [3]	**I**	-		Y[3]	G[3]
GIN [2]	**I**	-		Y[2]	G[2]
GIN [1]	**I**	-		Y[1]	G[1]
GIN [0]	**I**	-		Y[0]	G[0]
BIN [7]	**I**	-		U[7]	B[7]
BIN [6]	**I**	-		U[6]	B[6]
BIN [5]	**I**	-		U[5]	B[5]
BIN [4]	**I**	-		U[4]	B[4]
BIN [3]	**I**	-		U[3]	B[3]
BIN [2]	**I**	-		U[2]	B[2]
BIN [1]	**I**	-		U[1]	B[1]
BIN [0]	**I**	-		U[0]	B[0]

2.2 DIGITAL VIDEO OUTPUT ASSIGNMENT

As for output, VX1138 sends progressive video data out with 24/18/16-bit 4:4:4 RGB/YUV digital formats or 16-bit 4:2:2 YUV format or 8-bit YUV format through pins DR_V, DG_Y, and DB_U. The pin assignment for each format is defined in *Table 2.2*

Table 2.2 Digital Video Output Pin Assignment

Pin Name	I/O Type	Digital Output				
		8-bit YUV	16-bit 4:2:2 YUV	16-bit RGB565 / YUV	18-bit RGB666 / YUV	24-bit RGB / YUV
ROUT [7]	**O**	-	UV [7]	R/Pr/V [4]	R/Pr/V [5]	R/Pr/V [7]
ROUT [6]	**O**	-	UV [6]	R/Pr/V [3]	R/Pr/V [4]	R/Pr/V [6]
ROUT [5]	**O**	-	UV [5]	R/Pr/V [2]	R/Pr/V [3]	R/Pr/V [5]
ROUT [4]	**O**	-	UV [4]	R/Pr/V [1]	R/Pr/V [2]	R/Pr/V [4]
ROUT [3]	**O**	-	UV [3]	R/Pr/V [0]	R/Pr/V [1]	R/Pr/V [3]
ROUT [2]	**O**	-	UV [2]	-	R/Pr/V [0]	R/Pr/V [2]
ROUT [1]	**O**	-	UV [1]	-	-	R/Pr/V [1]
ROUT [0]	**O**	-	UV [0]	-	-	R/Pr/V [0]
GOUT [7]	**O**	YUV[7]	Y [7]	G/Y [5]	G/Y [5]	G/Y [7]
GOUT [6]	**O**	YUV[6]	Y [6]	G/Y [4]	G/Y [4]	G/Y [6]
GOUT [5]	**O**	YUV[5]	Y [5]	G/Y [3]	G/Y [3]	G/Y [5]
GOUT [4]	**O**	YUV[4]	Y [4]	G/Y [2]	G/Y [2]	G/Y [4]
GOUT [3]	**O**	YUV[3]	Y [3]	G/Y [1]	G/Y [1]	G/Y [3]
GOUT [2]	**O**	YUV[2]	Y [2]	G/Y [0]	G/Y [0]	G/Y [2]
GOUT [1]	**O**	YUV[1]	Y [1]	-	-	G/Y [1]
GOUT [0]	**O**	YUV[0]	Y [0]	-	-	G/Y [0]
BOUT [7]	**O**	-		B/Pb/U [4]	B/Pb/U [5]	B/Pb/U [7]
BOUT [6]	**O**	-		B/Pb/U [3]	B/Pb/U [4]	B/Pb/U [6]
BOUT [5]	**O**	-		B/Pb/U [2]	B/Pb/U [3]	B/Pb/U [5]
BOUT [4]	**O**	-		B/Pb/U [1]	B/Pb/U [2]	B/Pb/U [4]
BOUT [3]	**O**	-		B/Pb/U [0]	B/Pb/U [1]	B/Pb/U [3]
BOUT [2]	**O**	-		-	B/Pb/U [0]	B/Pb/U [2]
BOUT [1]	**O**	-		-	-	B/Pb/U [1]
BOUT [0]	**O**	-		-	-	B/Pb/U [0]

3 CLOCK SYSTEM

3.1 REFERENCE CLOCK SETTING FOR PLL INPUT CLOCK

All the clocks required for vx1138 can be generated from internal PLL. The reference input clock for PLL comes from video input clock(VICLK or RGBIN_CLK) or external Crystal, depends on user's requirement. This can be set by pin ICLK_SEL[1:0]. When the value is set to 2'b00, the default value, the system auto detect the existed clock, according to the order VICLK, RGBINCLK, XTAL_IN. when the value is set to 2'b01, the reference clock comes from pin VICLK. When the value is set to 2'b10, the reference clock comes from RGBIN_CLK. When the value is set to 2'b11, it comes from external crystal pin XTAL_IN. Table 3.1 list the reference clock setting for PLL.

Table 3.1 PLL input Reference Clock Configuration

INCLK_SEL	00	01	10	11
Ref_clock	Auto_detect	VICLK	RGBINCLK	XTALIN
AUTO_DETECT is detected by the order VICLK, RGBINCLK, XTALIN REF_CLOCK is used for internal PLL reference input clock and iic clock				

4 HOST INTERFACE

The VX1138 host interface uses two-wire IIC compatible interface protocol, one for clock, and one for multiplexed data/address. Input pin SCL is used for host clock input while input/output pin SDA is for multiplexed host data and address signal. VX1138 requires 2 chip address to control the video decoder and progressive video processor parts. When write to the progressive video processor part(deinterlace,scaler,..), the Chip Write Address is 0x32, and Chip Read Address is 0x33.

Once chip write and read addresses are configured, the host command byte sequence can be transfer to VX1138 via the serial interface. The byte sequence consists of a CHIP ADDRESS, a REGISTER ADDRESS, followed by a number of DATA BYTES. The CHIP ADDRESS and REGISTER ADDRESS must be always provided by the host, usually a micro-controller, and the DATA BYTES are provides by host for host-writings and by VX1138 for host-readings.

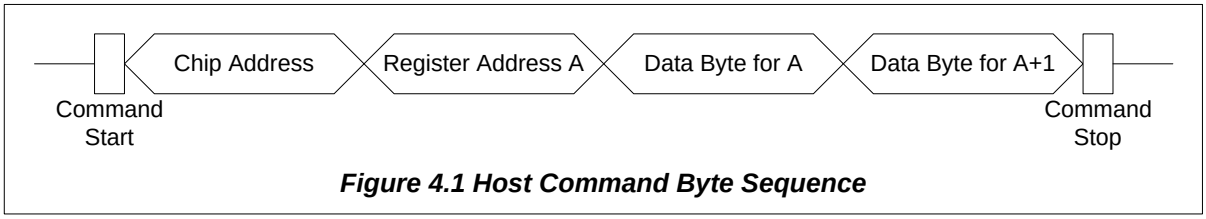


Figure 4.1 Host Command Byte Sequence

As shown above, the first DATA BYTE following REGISTER ADDRESS A is assigned or read to/from register address A, the DATA BYTE behind will be assigned/read to/from register address A+1, and so on. So for large host-writings such as chip initialization, only the initial register address needs to be specified once to complete whole host writing operations. In this manner user can save a lot of host command cycles in complicated applications.

5 HARDWARE AND SOFTWARE RESET

VX1138 can be reset to initial stage in two ways. One is through the hardware pin, RESETB; by asserting RESETB pin to ground voltage, entire chip will be reset to its initial states. The other way is through the host interface by writing to register RST1 (01h). Writing value 5Ah to RST1, called software reset, will generate an internal reset pulse signal similar to RESETB to initialize the entire chip.

Similar to writing 5Ah to RST1, writing A5h to RST1 will reset entire chip *except* control registers programmed by host interface. The use of A5h writing often occurs after initial register programming or mid-state register changes to assure the chip working from the initial state.

6 VIDEO INPUT SELECTION

The VX1138 accepts 6 types of digital video formats as input data stream, it can be set by changing the value of register bits INFMT [2:0]. Following Table 6.1 shows VX1138's acceptable digital video input formats. For their pin assignment, please review *CHAPTER 2 DIGITAL VIDEO I/O PIN ASSIGNMENT*.

Table 6.1 Digital Video Input Format Selection

INFMT [2:0]	Digital Video Input Format
000	8-Bit ITU-R BT.656
001	8-Bit ITU-R BT.601 Digital Video Data With external H_sync and V_sync input
010	16-bit Y/UV 4:2:2 data with external sync pin
011	16/18/24-bit Y/U/V 4:4:4 progressive data
110	8-bit CCD Bayer format input (up to 1280 pel/line)
111	24-bit RGB progressive input

If the input data of above format is progressive, set the register bit PG_IN to 1.

The VX1138 supports all NTSC, PAL, SECAM, and square pixel video standard. For each standard the number of lines per field and pixels per line vary according to their specifications. These standards are summarized as follows.

Table 6.2 Video input standard

Input format	Horizontal Total Pixels Per Line	Vertical Total Lines Per Frame	Frame Rate
NTSC	858	525	60
PAL/SECAM	864	625	50

It can automatically detect the digital video format by setting the AUTO_NP on. The digital video source also can be forced to NTSC,PAL,SECAM by disabling AUTO_NP, and then manually set register bit SET_NP to 1 for PAL/SECAM, or 0 for NTSC. To enter the square pixel mode, user needs to enable the register bit SQ_EN. The NTSC/PAL/SECAM auto-detection function also works under square pixel mode.

For ITU-R BT.656 format, the UV byte could be unsigned signal, which is in the range from 0 to 255, or signed 2's compliment signal, which is in the range from –128 to 127. Set the register bit UVFMT to define above two types of UV data for VX1138.

If the digital video input format (INFMT) is 001, 011, the additional synchronization signals VIHS and VIVS must be used along with the digital video input data. The VIVS pin depending on the register INSYN could be configured as one of four types of vertical synchronization signals, equaled VSYNC, non-equaled VSYNC, equaled FIELD, and non-equaled FIELD. The “Equaled” signal means the vertical synchronization duration is in the same length for EVEN and ODD field. The “Non-Equaled” signal means the vertical synchronization duration is longer for ODD field than EVEN field.

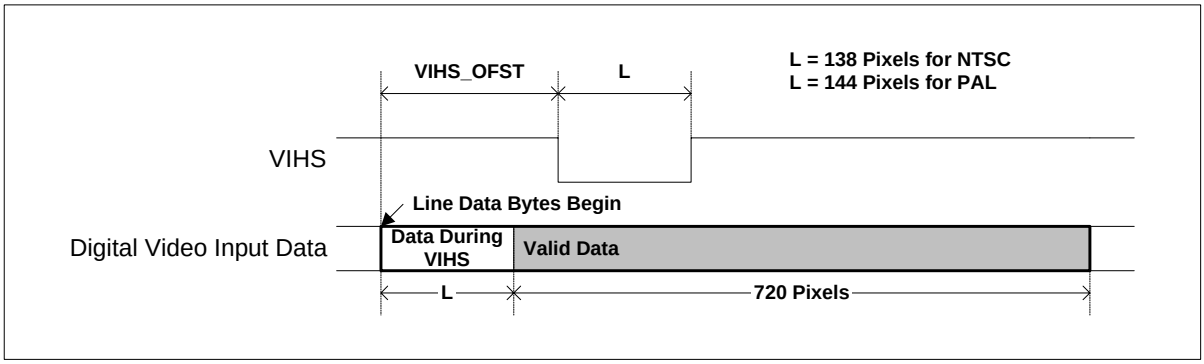


Figure 6.1 Digital Video Input Signals

Shown in above figure, the VX1138 takes 720 pixels in each horizontal line as the active data. In NTSC system, the number of total pixels in each line is 858. This results in that the length of the horizontal synchronization period is 138 pixels and during this period of time, the bytes in the data channel will be ignored, therefore. Register VIHS_OFST is used to fine-tune the screen position of valid data period. Its range is from -127 to 127 and default value is 0.

For some specific applications, the number of pixels in each horizontal line is not the same as NTSC or PAL/SECAM systems, such as sub-carrier frequency domain video data. To compensate this difference, the VX1138 has an option to manually set the horizontal length. To enable this feature, the register MIL_EN must be enabled first, then user can specify target number of length in pixel to register MHIL. Note that since the internal line buffer length is still limited to 720 pixels, Manually setting larger number of length will truncate more pixels in each line.

Usually the input data is latched per cycle of the video input clock. For some cases that the data should be latched every two cycles of the video input clock, such as latching 16-bit YC by 27 MHz clock, program the register VICLKF to zero.

7 RELÁCS

Relács is VXIS's intellectual invention of high-quality and low-cost scaler. It utilizes separate algorithms for up-scaling and down-scaling processes and sharing the usage of line buffers. For output resolution setting, refer to the following table for some default setting of register SMODE.

Table 7.1 Output Resolution Setting

SMODE	Output Resolution
0	No Scaling
1	Down-Scaling to VGA (640 x 480)
2	Up-Scaling to SVGA (800 x 600)
3	Up-Scaling to XGA (1024 x 768)
4	Up-Scaling to SXGA (1280 x 1024)
5	Up-Scaling to 720P (1280 x 720)
6	Up-Scaling to WSVGA (1366 x 768)
7	Up-Scaling to WVGA (1600x1200)
8	Up-Scaling to 1080P (1920x1080)
9	Up-Scaling to WVGA (800 x 480)
10~15	Manual model

8 FRAME-RATE CONVERSION

Programming frame-rate conversion in VX1138 is simple and intuitive. Since the frame-rate conversion is done in the deinterlace stage in VX1138, the frequency of deinterlace clock is the parameter to fine-tune the video output frame-rate with respect to the input videos.

9 DEINTERLACE

The VX1138's deinterlace engine computes the insertion data from three-dimension information, containing three spatial and one temporal dimensions. Without external SDRAMs (MEM_USAGE = 00b; DEINT_MDOE = 10b, only for digital video input mode), the deinterlacer can performs Edge-Preserving Pixel Interpolation capable of detecting from 90-degree to 14-degree edge for most cost-effective application. With the aid of optional external SDRAMs as frame memory (MEM_USAGE = 01b; DEINT_MDOE = 00b), the VX1138 performs not only above Edge-Preserving Pixel Interpolation but also VXIS's most advanced Motion-Adaptive 3-D De-Interlace, which will lead theater quality video scheme in the conventional HDTV or monitor set.

10 COLOR ENHANCEMENT

10.1 CONTRAST, BRIGHTNESS, COLOR, AND HUE ADJUSTMENT

The VX1138 supports essential color adjustment through the registers, CONTRAST, BRIGHTNESS, COLOR, and HUE. Among those, the CONTRAST and the BRIGHTNESS can also be adjusted independently in R / G / B manner by the registers, R_CONTRAST, G_CONTRAST, B_CONTRAST, R_BRIGHTNESS, G_BRIGHTNESS, and B_BRIGHTNESS.

10.2 BLACK-LEVEL EXTENSION (BLE)

Basic idea of black level extension is to enhance the contrast of the luminance in the dark potion of the picture. As the result, the average luminance in the dark potion will be extended to darker level non-linearly while the luminance in bright potion remains unchanged. The advantage of this function is to make the object more solid, apparent, and noticeable to the viewers. The BLE function works adaptively, depending on the average luminance of the picture.

10.3 VIDEO NOISE REDUCTION (VNR)

The VX1138 contains video noise reduction (VNR) engine specifically removing Gaussian noise and mid-band interception noise, which commonly occurs in video transmission channels. *Figure 10.3.1* shows the block diagram of VX1138's VNR engine. VNR function is enabled from the register VNR.

10.4 SHARPNESS

The VX1138 offers three peaking filters for different frequency response in horizontal sharpness engine. The gain for each filter is adjustable from 0 to 14 dB and individually controlled with registers, PEAK_ADJ1, PEAK_ADJ2, and PEAK_ADJ3 (*Figure 10.4.1*). For peaking filter 1, 2, and 3, each respectively amplifies 1/2, 1/4, and 1/6 of sampling frequency (27 MHz). Following the three peaking filters is a clipping filter to suppress video gain after peaking filters and reduce noise. The clipping filter is adjustable with the registers PEAK_CLIP_MIN and PEAK_CLIP_MAX. If the input value (summed

gain) of the clipping filter is smaller than PEAK_CLIP_MIN, the output value of the clipping filter is clipped to zero. If the input value is between PEAK_CLIP_MIN and PEAK_CLIP_MAX, the output value of the clipping filter is linearly (input value - PEAK_CLIP_MIN). If the input value is larger than PEAK_CLIP_MAX, the output value of the clipping filter is clipped to (PEAK_CLIP_MIN - PEAK_CLIP_MAX).

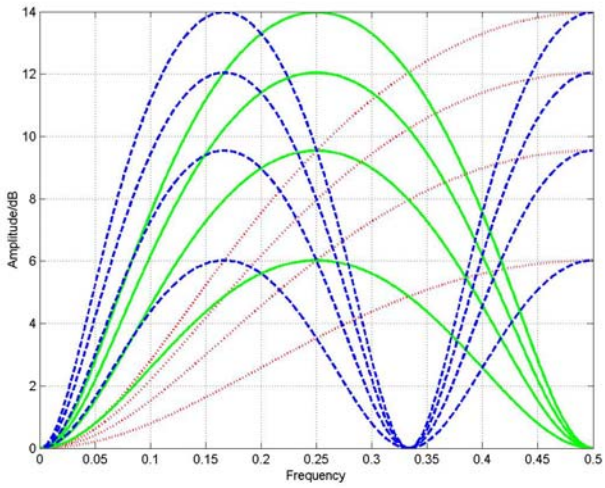


Figure 10.4.1 Frequency Response for Peaking Filters

10.5 COLOR-TRANSIENT IMPROVEMENT (CTI)

For most video solutions, video content in chrominance domain are often with less care due to human eye's neglect of color variations. Therefore, we sometimes found that the picture is implicitly dirty and foggy especially when we observing the video patterns or color-bars. The color-transient improvement (CTI) engine in VX1138 is made to recover this imperfectness of video presentation and perform sharp and keen edges for every objects and overall clearer video to the viewers.

10.6 COLOR LOOK-UP TABLE (CLUT) AND GAMMA CORRECTION

The VX1138 provides method to finely manipulate video sequence, color look-up table (CLUT). CLUT is made of three embedded SRAMs and requires initial SRAM programming with continuous-write scheme of host interface. Register CLUT_MODE enable the usage of CLUT.

10.6.1 CLUT

Widely used in many applications, the VX1138 equips a build-in 3-channel 10-bit color look-up table (CLUT). The CLUT contains three 256 x 10-bit SRAMs, one for each of R/Pr, G/Y, and B/Pb channels. For each channel, the SRAM acts as an one-to-one mapping array and reads 8-bit data as index, and maps into 10-bit data as SRAM data output. By manipulating every single cell of SRAMs, user can make neat changes of the color mapping for each single level of 256 color levels in each channels. Using the CLUT, all the picture/video related adjustments such as color adjustment, gamma, and color temperature can be accomplished with specifically programmed mapping data. CLUT_MODE and the datawidth register CLUT_WIDTH, must be set before using the CLUT.

Programming the CLUT is intuitive through the continuous-write registers. First, program the destination SRAM to one or all of the R/Pr, G/Y, B/Pb channels with the register CW_DEST. Next, write the initial 8-bit address to register CW_INIT_ADDR. Then, in sequence write the data into the register CW_DATA, and the internal host interface controller will automatically write this data into the designated SRAM after a short period of time, and increment the address by 1 after each internal SRAM writing. If the CLUT data width is set to 10-bit, then the internal automatic SRAM writing operation will take place at every two host writing of CW_DATA (*Figure 10.6.1.2*).

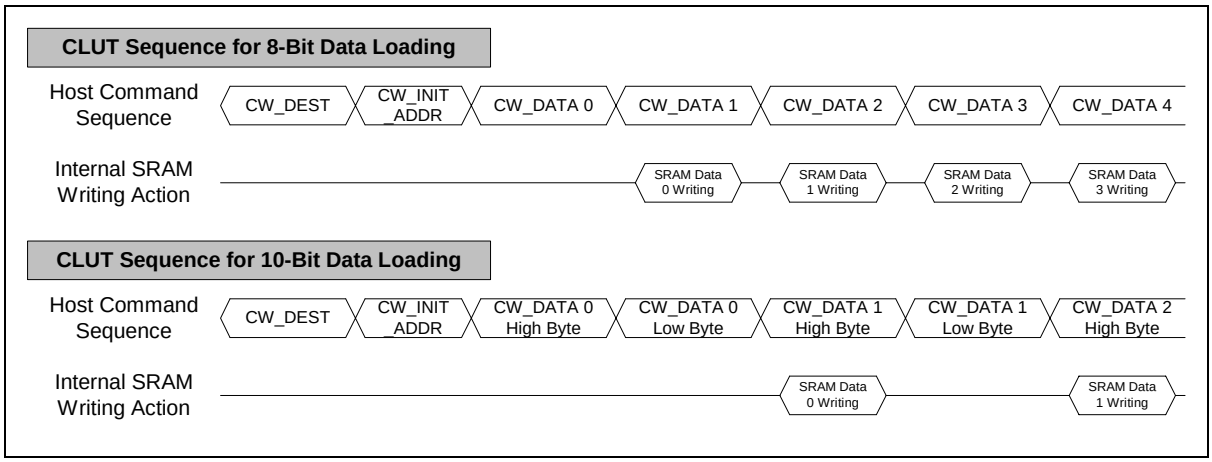


Figure 8.6.1.2 CLUT Programming Sequence Through Host Interface

Note that the CLUT always maps the video in the color domain of analog output port. This means when the analog output port is set to RGB, CLUT mapping is in RGB domain, and when the analog output is set to YPbPr or YUV, CLUT mapping is in YPbPr or YUV domain. Also, as shown in *Figure 10.6.1.3* that the value stored in the SRAM can be in 10-bit range (CLUT_WIDTH = 1), or in 8-bit range (CLUT_WIDTH = 0) in RGB or YUV domain mappings. But note that due to synchronization insertion to Y channel, in YPbPr domain CLUT only supports 8-bit mappings.

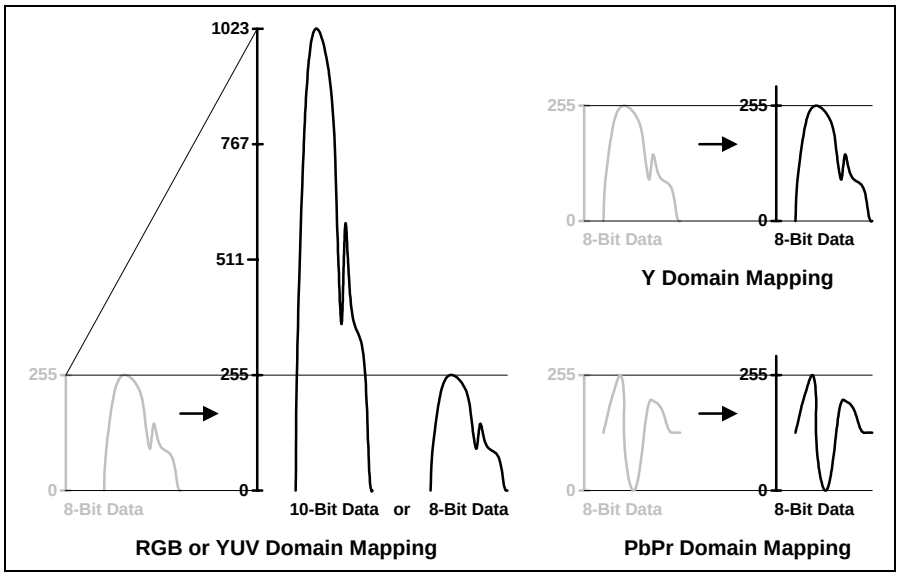


Figure 10.6.1.3 CLUT Mappin

11 VIDEO OUTPUT SECTION

11.1 PROGRESSIVE VIDEO OUTPUT SETTING

The VX1138 generates variety of digital video outputs formats. It supports digital output in 24/18/16-bit RGB, 4:4:4 YPbPr (with embedded horizontal and vertical synchronization on Y), 4:4:4 YUV (with additional HSYNC and VSYNC pins), or 16-bit 4:2:2 YUV formats. For digital video I/O pin assignment, please see "Chapter *2 DIGITAL VIDEO I/O PIN ASSIGNMENT*". Format selection of progressive digital output ports is done through setting of register OFMT. For 8-bit CCIR656 data output, the output format is set to YUV 4:4:4 format (OFMT=3).

Table 11.1.1 Progressive Video Output Format

	OFMT	Output Format
Digital Port	0	3-Channel RGB (df.)
	1	3-Channel 4:4:4 YPbPr (with embedded horizontal and vertical synchronization on Y
	2	2-Channel 4:2:2 YUV (with additional HSYNC and VSYNC pins)
	3	3-Channel 4:4:4 YUV (with additional HSYNC and VSYNC pins)

11.2 DITHERING

When the output format is determined, there is a dithering option provided in 4:4:4 RGB / YPbPr / YUV digital video output formats. For users who are limited to accept 24/18/16-bit digital videos, two approaches can be selected, either simply truncate the 24-bit output data by connecting partial bits of digital video output, or dither the 24-bit output data by setting register DITHER (*Table 11.2.1*). The dithering algorithm used in the VX1138 is by applying error diffusion calculation to the data and will effectively reduce the boundary effect in low-resolution displays.

Table 11.2.1 Dithering Options

DITHER	Dithering Option (G/Y : B/Pb/U : R/Pr/V)
0	Disable
1	Dithering to 18-bits (6-bits : 6-bits : 6-bits)
2	Dithering to 24-bits (8-bits : 8-bits : 8-bits)
3	Dithering to 16-bits (6-bits : 5-bits : 5-bits)

11.3 CLAMPING

The VX1138 has an option to set the digital video output level in ITU-R BT.601 range, ITU-R BT.656 range, or simply in 0-255 8-bit full range. For ITU-R BT.601 standard, luminance channel (Y) is in the range of 16-235, and chrominance channel (UV) is in the range of 16-240. For ITU-R BT.656 standard, luminance (Y) and chrominance channel (UV) are in the range of 1-254. See the register CLAMP for details.

11.4 VIDEO OUTPUT TIMING

For digital video output, all the digital video output datas are valid at the falling edge of the video output clock VOCLK.

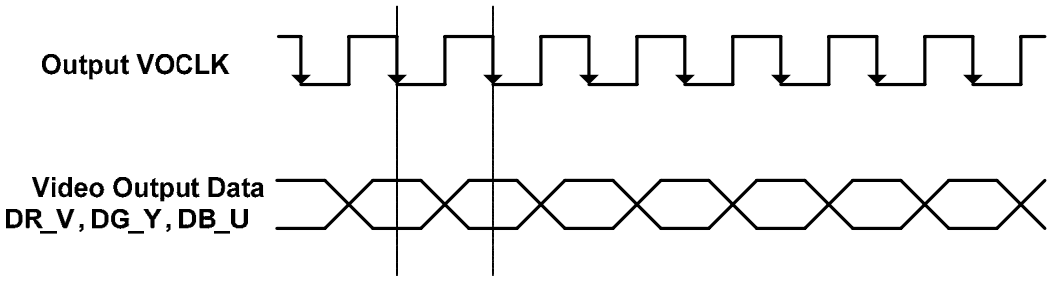


Figure 11.4.1 Video Output Timing

11.5 VIDEO OUTPUT SYNCHRONIZATIONS

All the video output synchronization signals, HSYNC, VSYNC, or GCSYNC, of VX1138 are adjustable with respect to output format, frequency, and resolutions. Basically the horizontal synchronization (HSYNC) asserts on every horizontal line's boundary; vertical synchronization (VSYNC) asserts on every frame's boundary; and general composite synchronization (GCSYNC) acts as the combination of horizontal and vertical synchronizations (*Figure 11.5.1*).

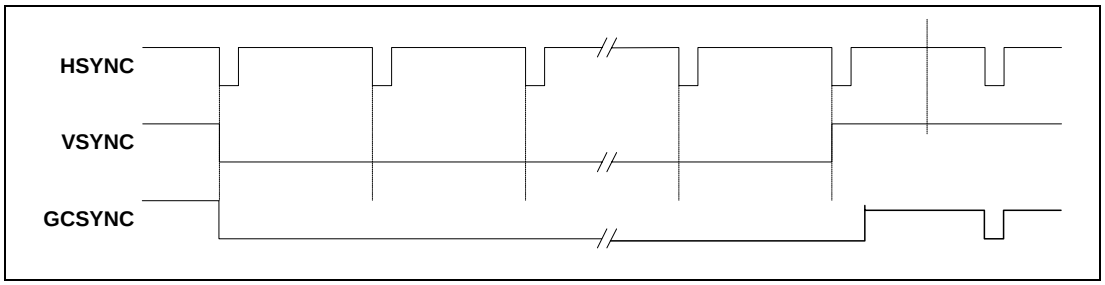


Figure 11.5.1 Video Output Synchronizations

The adjustment of synchronization-width of HSYNC and VSYNC is through the registers HS_WIDTH and VS_WIDTH. The actual length of synchronization-width of HSYNC is HS_WIDTH in pixels, and VSYNC is (1 + VS_WIDTH) in lines.

HSYNC and VSYNC are always available at pins. GCSYNC is shared with HSYNC and switched by the register VOHS_SEL

11.6 VIDEO OUTPUT DISPLAY

Two essential elements, screen shifting and masking, control the VX1138 video output display. The screen shifting function is activated by changing the horizontal shifting register HSHIFT, and vertical shifting register VSHIFT. Setting larger value of HSHIFT moves the picture rightward; and setting larger value of VSHIFT moves the picture downward. Also, the screen masking function is activated by setting the registers BOTTOM_MASK, TOP_MASK, LEFT_MASK, and RIGHT_MASK. The VX1138's output display region with its synchronization and control parameters (screen shifting and screen masking) is summerized in *Figure 11.6.1*.

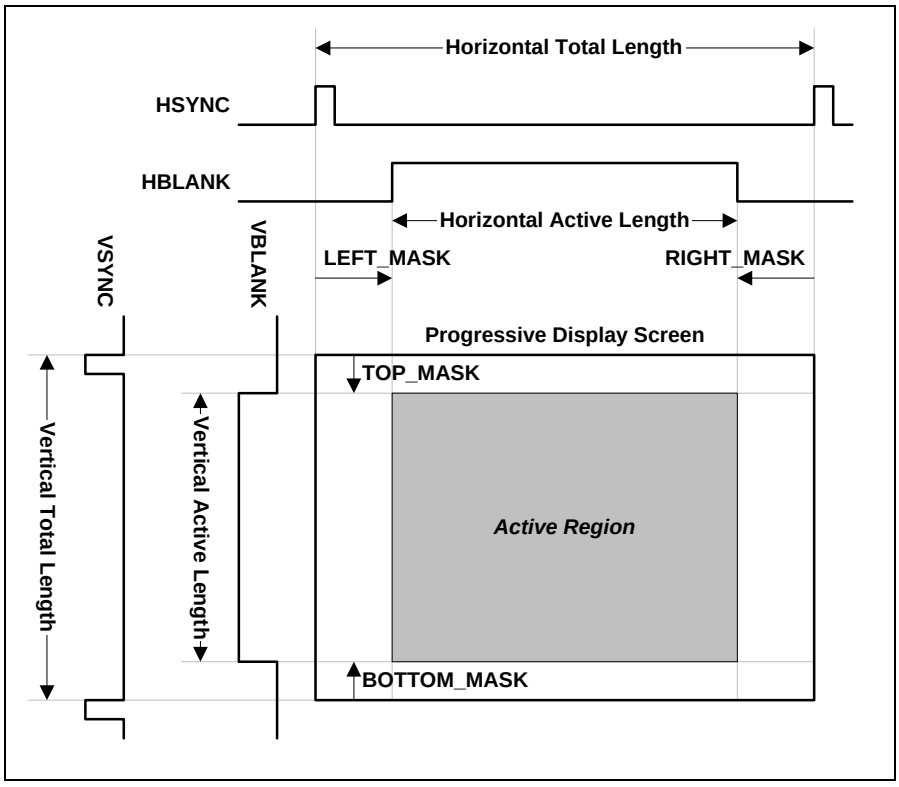


Figure 11.6.1 Output Display Region

12 ON-SCREEN-DISPLAY (OSD)

12.1 OSD INTRODUCTIONS

The VX1138 integrates VXIS's font-attribute-based on-screen display (OSD) unit, which can display a total of up to 256 characters in a single screen, with each font in 16 pixels x 20 pixels format. The embedded font Random-Access-Memory (RAM) and Read-Only-Memory (ROM) let user select characters from up to 192 fonts, 128 build-in and 64 programmable fonts. The attribute bits programming let user designate arbitrary spectacular menu, closed caption, even games from 16,777,216 colors, blinking, *Italic* font, underline font, and many artistic features.

12.2 OSD DISPLAY BLOCKS

The build-in OSD system divides the screen display into three basic sections, the title, content, and bottom blocks, and the user can customize the size and position for each display block by host commands (*Figure 12.2.1*).

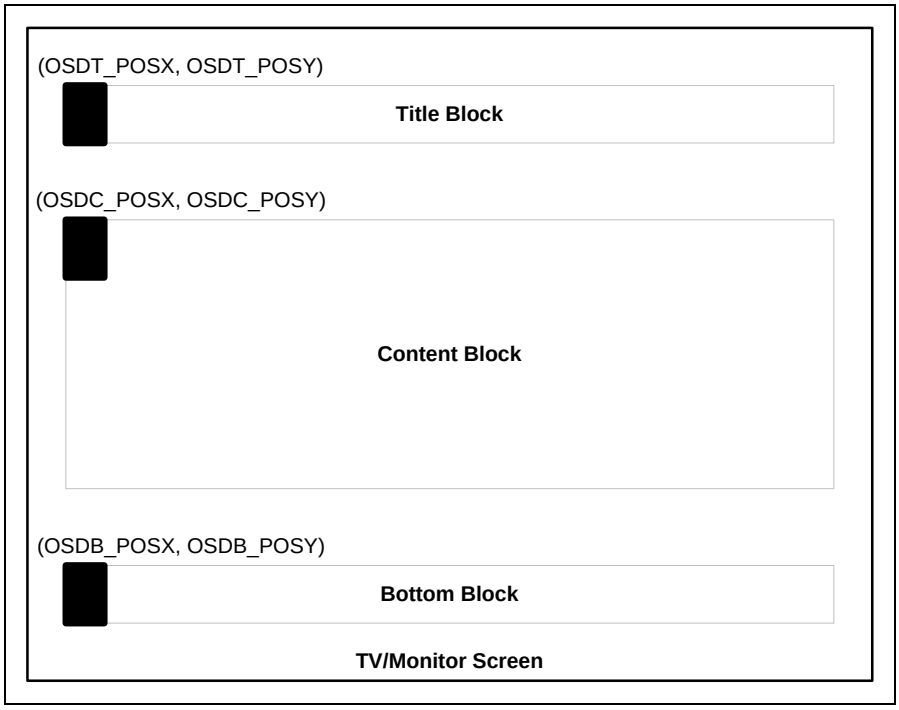


Figure 12.2.1 OSD Display Blocks

The title and bottom blocks are restricted to display one line of text commonly for header or page notes;

and the content block displays multiple lines of text for main OSD information. The sizes and the positions for each individual block are adjustable through registers (*Table 12.2.1*). Each displaying block cannot be overlapped with others. For details of the register setting, check OSD section in register description chapter.

Table 12.2.1 Position and Size Registers

Register		Description
OSDT_POSX	OSDT_POSY	Position registers for title block
OSDC_POSX	OSDC_POSY	Position registers for content block
OSDB_POSX	OSDB_POSY	Position registers for bottom block
OSDT_SIZEX	N/A	Size registers for title block
OSDC_SIZEX	OSDC_SIZEY	Size registers for content block
OSDB_SIZEX	N/A	Size registers for bottom block

12.3 OSD OPERATIONS

The VX1138's OSD unit is font-based entry. All information that is going to be shown in the screen must be translated into fonts, which is in 16 pixel x 20 pixel resolution each, then put into the screen.

There are two types of OSD memories embedded in VX1138. One is called the "font memory", which stores all the fonts currently being used on the screen. The font memory consists of one 128-font ROM (2560 x 16-bit) for commonly used fixed fonts, and one 64-fonts RAM (1280 x 16-bit) for user-programmable fonts (*Table 12.3.1*). If utilizing maximum amount of the memory, there are up to 192 fonts can be repeatly shown in the single page.

Table 12.3.1 Font Memory Table

Index (Hex)	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
Character	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
Index (Hex)	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h	1Ah	1Bh	1Ch	1Dh	1Eh	1Fh
Character	Q	R	S	T	U	V	W	X	Y	Z	a	b	c	d	e	f
Index (Hex)	20h	21h	22h	23h	24h	25h	26h	27h	28h	29h	2Ah	2Bh	2Ch	2Dh	2Eh	2Fh
Character	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v
Index (Hex)	30h	31h	32h	33h	34h	35h	36h	37h	38h	39h	3Ah	3Bh	3Ch	3Dh	3Eh	3Fh
Character	w	x	y	z	á	à	â	ç	é	è	ê	í	î	Ñ	ñ	ó

Index (Hex)	40h	41h	42h	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh
Character	ô	ú	û	!	,	.	;	:	'	"	#	%	&	@	/	(
Index (Hex)	50h	51h	52h	53h	54h	55h	56h	57h	58h	59h	5Ah	5Bh	5Ch	5Dh	5Eh	5Fh
Character	)	[	]	+	−	÷	<	=	>	?	°	¢	$	£	®	™
Index (Hex)	60h	61h	62h	63h	64h	65h	66h	67h	68h	69h	6Ah	6Bh	6Ch	6Dh	6Eh	6Fh
Character	½	¿	0	1	2	3	4	5	6	7	8	9	♪			■
Index (Hex)	70h	71h	72h	73h	74h	75h	76h	77h	78h	79h	7Ah	7Bh	7Ch	7Dh	7Eh	7Fh
Character	▔	▏	▎	▍	▌	▋	▊	▉	▉	^	v	▔	_	▕	▕	□
Index (Hex)	80h	81h	82h	83h	84h	85h	86h	87h	88h	89h	8Ah	8Bh	8Ch	8Dh	8Eh	8Fh
Character	User-Programmable Fonts															
Index (Hex)	90h	91h	92h	93h	94h	95h	96h	97h	98h	99h	9Ah	9Bh	9Ch	9Dh	9Eh	9Fh
Character	User-Programmable Fonts															
Index (Hex)	A0h	A1h	A2h	A3h	A4h	A5h	A6h	A7h	A8h	A9h	AAh	ABh	ACh	ADh	AEh	AFh
Character	User-Programmable Fonts															
Index (Hex)	B0h	B1h	B2h	B3h	B4h	B5h	B6h	B7h	B8h	B9h	BAh	BBh	BCh	BDh	BEh	BFh
Character	User-Programmable Fonts															
Index (Hex)	C0h	C1h	C2h	C3h	C4h	C5h	C6h	C7h	C8h							
Character	CR	2B	3B	4B	5B	6B	7B	8B	9B							

CR: Character Return / Line Feed

nB: Number of Space Characters

Another type of memory is called the “command memory”, which stores the sequence and the attribute of the font that is appearing on the screen. The command memory consists of two 256 x 8-bit RAMs in two modes (*Table 12.3.2*). In COLR mode, the command memory stores 256 font indexes with 8-bit attributes of blinking, and sixteen colors for foreground and background; and in CCAP mode, the command memory stores 256 font indexes each with 8-bits attributes of blinking, *Italic* font option, underline font option, eight colors for foreground, and four colors for background.

Table 12.3.2 Command Memory Configuration

Register CCMODE	Description	Note
0	COLR Mode	Stores 256 font indexes with attribute for color support
1	CCAP Mode	Stores 256 font indexes with attribute for closed caption support

To generate OSD in either mode, the command memory needs to be well programmed. It is divided into title, content, and bottom sections of which initial address pointed by the registers OSDT_MADR,

OSDC_MADR, and OSDB_MADR (*Figure 12.3.1*). From the initial address in each section, fill in the indexes of fonts in designated sequence, and the font will appear on the screen consecutively at the next frame. Sections allocated in the command memory can be overlaped with others.

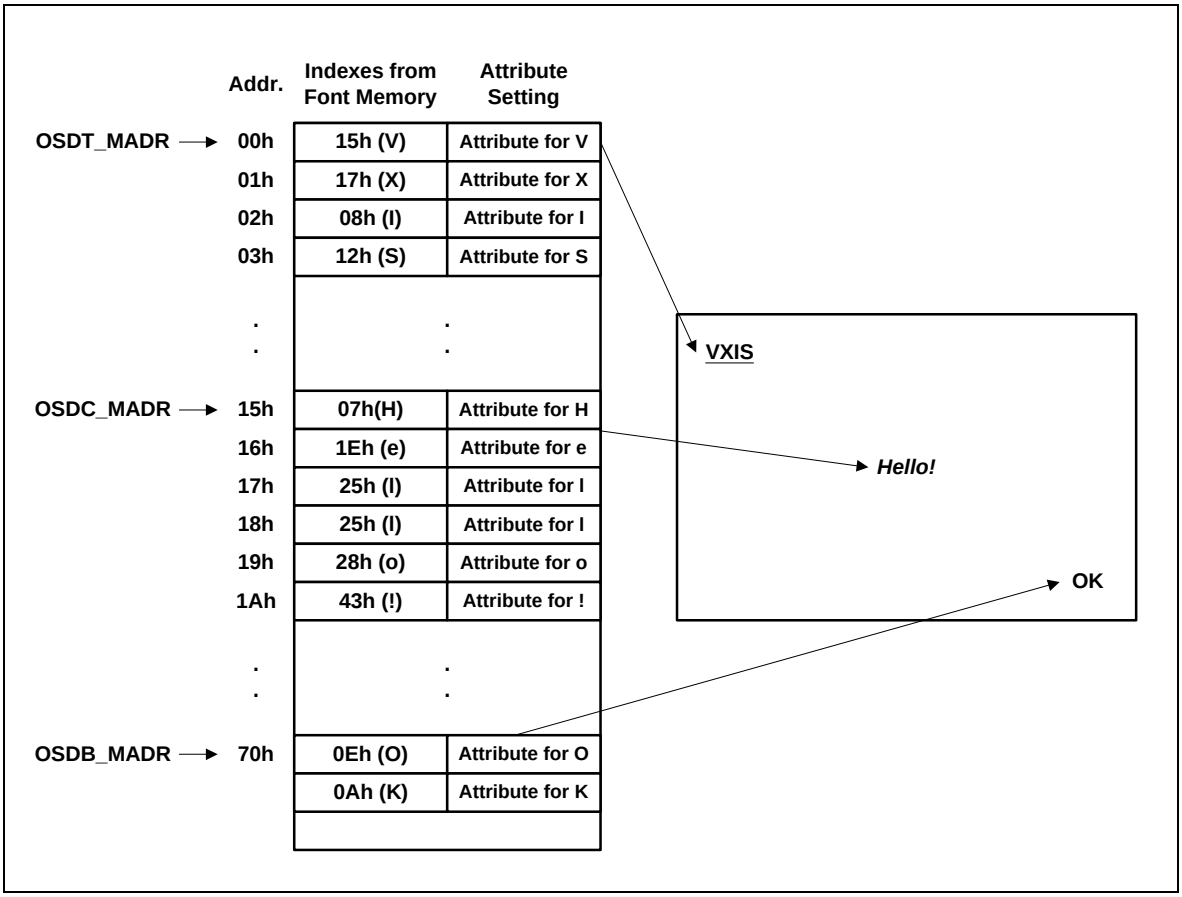


Figure 12.3.1 OSD Command Memory

12.4 OSD ATTRIBUTE SETTING

Each font displayed on the screen has its own 8-bit attributes for blinkings, colors, and special font formats. They are slightly different in CLOR mode and CCAP mode (*Table 12.4.1*).

Table 12.4.1 Attribute Bits Table

Bit	CLOR Mode	CCAP Mode
7	Blinking On	
6	BG Palette Color Index [2]	*Italic* Font On
5	BG Palette Color Index [1]	BG Color Index [1]

4	BG Palette Color Index [0]	BG Color Index [0]
3	FG Palette Color Index [3]	Underline Font On
2	FG Palette Color Index [2]	FG Palette Color Index [2]
1	FG Palette Color Index [1]	FG Palette Color Index [1]
0	FG Palette Color Index [0]	FG Palette Color Index [0]

There are sixteen blinking-rate options from 0.5 Hz to 7.5 Hz defined in the register, OSD_BLINK. The blinking-rate relates to the OSD_BLINK according to the following equation.

$$\text{OSD Blinking Rate} = \frac{30}{\text{OSD\_BLINK} \times 4}\ \text{Hz}$$

The OSD unit has sixteen build-in color palettes each can be fine adjusted from 24-bit color space (16,777,216 colors). Color palette programming can be achieved through the registers, OSD_CP_INDEX, OSD_CP_R, OSD_CP_G, and OSD_CP_B. In CLOR mode, the foreground color of each font is chosen from the color palette index 0 to 15 (FG Palette Color Index [3:0]); the background color from index 8 to 15 (BG Palette Color Index [2:0]). As in CCAP mode, the foreground color of each font is chosen from the color palette index 0 to 7 (FG Palette Color Index [2:0]); the background color of each font is chosen from the registers CCAP_BG0, CCAP_BG1, CCAP_BG2, and CCAP_BG3 with index (BG Color Index [1:0]). For CCAP_BG settings check *Table 12.4.2*.

Table 12.4.2 CCAP_BG Color Setting

CCAP_BG Bits	Color	CCAP_BG Bits	Color
0000	Black	1000	Transparent
0001	Blue	1001	Royal Blue
0010	Green	1010	Medium Aquamarine
0011	Aqua	1011	Light Green
0100	Red	1100	Orange
0101	Fuchsia	1101	Hot Pink
0110	Yellow	1110	Silver
0111	White	1111	Gray

The register, TRAN_INDEX, assigns the color palette index in which stands for transparent color.

12.5 OSD MASKING AND ALPHA-BLENDING

The VX1138's OSD unit provides special masking function in the content displaying block. This is mainly for the scrolling function during closed caption displaying. The registers, OSDC_MASK_L, OSDC_MASK_R, OSDC_MASK_T, and OSDC_MASK_B define the boundary location for the four sides of the masking blocks.

The VX1138's OSD unit also support whole screen OSD alpha-blending with the source video. The blending factor, OSD_ALPHA, is programmable in registers and follows below equation.

$$\text{OSD Displaying Color} = \frac{\text{Video Color} \times \text{OSD\_ALPHA} + \text{OSD Color} \times (4 - \text{OSD\_ALPHA})}{4}$$

12.6 OSD MEMORY ACCESS

To configure the command memory and the user-programmable font memory, the VX1138 provides two methods by accessing registers. One method is through the direct memory accessing registers OSD_ADDR, OSD_DATA, and OSD_ATRI for command memory, and registers OSD_FONT_ADDR, OSD_FONT_DATA for user-programmable font memory. The other method is through the continuous writing mechanism with Continuous-Write Registers, CW_DEST, CW_INIT_ADDR, and CW_DATA.

12.6.1 DIRECT MEMORY ACCESS

To directly change the content of the command memory, simply put the address in register OSD_ADDR and the data in registers OSD_DATA and OSD_ATRI. The OSD unit will send the data into the command memory right after the register writing operation of register OSD_DATA and OSD_ATRI. Similarily, to directly change the content of the user-programmable font memory, user simply puts the address in the register OSD_FONT_ADDR and the data in the register OSD_FONT_DATA from high byte to low byte. The OSD unit will send the data into the user-programmable font memory right after the writing operation of low byte of OSD_FONT_DATA.

12.6.2 CONTINUOUS WRITE MEMORY ACCESS

For large amount of data writing operation such as font memory writing or full screen display change, the VX1138 provides continuous writing mechanism to save host access time and efforts. To use the Continuous-Write Registers, set the destination register, CW_DEST, and the initial address register,

CW_INIT_ADDR, consecutively, then write the data register, CW_DATA, repeatly. The continuous-writing mechanism will put data into the destination memory immediately after CW_DATA writing. For 16-bit data writing such as user-programmalbe font memory, the internal memory data writing will occur after every other CW_DATA writing (high byte prior to low byte). For example, to store a plus sign, "+", into the user-programmalbe font memory, the writing sequence are as *Table 12.6.2.1*.

Table 12.6.2.1 Host Writing Sequence for Bitmap

Host Command	Address	Data
Write	CW_DEST	010
Write	CW_INIT_ADDR	00_0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0011_1111
Write	CW_DATA	1111_1100
Write	CW_DATA	0011_1111
Write	CW_DATA	1111_1100
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0001
Write	CW_DATA	1000_0000
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000

Host Command	Address	Data
Write	CW_DATA	0000_0000
Write	CW_DATA	0000_0000

13 MEMORY INTERFACE

The external SDRAM interface of VX1138 provides the connection to standard Synchronous Dynamic Random-Access Memory (SDRAM) device. The interface supports 1M x 16 bit SDRAMs, supporting speed at least of -7 and CAS latency of 2. The memory-usage register, MEM_USAGE, configures SDRAM model being used, and partial functions may be inactivated between models (*Table 13.1*). See *Figure 13.1* for SDRAM connection diagram.

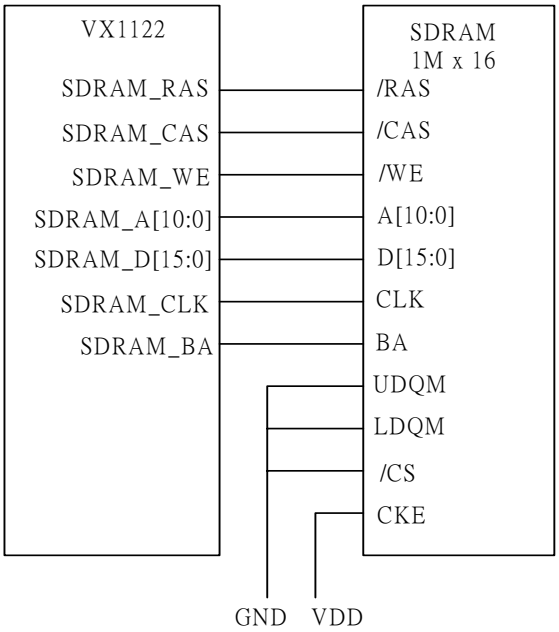


Figure 13.1 SDRAM Connection Diagram

14 TIMING CONTROLLER

The controlling signals applied to panel are generated by timing controller. STHR/L, POL, LD and VOCLK are controlling signals for source. Register LR (REG0xC0.1) set left-scan or right-scan by enable one of STHR/L. STVL/R, CKV and OEV are controlling signals for gate driver.

15 REGISTER DESCRIPTION

15.1 PROGRESSIVE VIDEO PROCESSOR REGISTER (CHIP ADDRESS = 0X32)

15.1.1 REGISTER MAP

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
01	RST1	00	RESET / CLEAR							
03	RST3	F1	DEI_ON	RELX_ON	MCLK_ON	OSD_ON	D2OCLK	GPO1_EN	GPO0_EN	ACLK_ON
04	GBL0	1C		DCLK_INV	GPO1_SEL			GPO0_SEL		
05	GBL1	01	TCON_EN	VOHS_SEL	-	CLKDSRC		GPO2_SEL		
10	IN0	20	NTSCPAL	VICLKP	AUTO_NP	SET_NP	VICLKF	SQ_EN	UVFMT	-
11	IN1	00	INFMT			INSYN		VIHSP	-	VIVSP/ VIFDP
12	IN2	00	VIHS_OFST[7:0]							
13	IN3	03	V4_UV_INV	INFIELD_INV	-	MIL_EN	MHIL [11:8]			
14	IN4	5A	MHIL [7:0]							
15	IN5	8A	MHSL							
16	IN6	00	VIVS_OFST[7:0]							
17	IN7	00	PG_IN	PASS_DEINT	VIVS_OFST[10:8]			VIHS_OFST[10:8]		
18	IN8	28	VSYNC_LEN					MVIL [10:8]		
19	IN9	00	MVIL [7:0]							
1A	INA	00	INFC_PAT		MVIAL [10:8]			MHIAL [10:8]		
1B	INB	00	MHIAL [7:0]							
1C	INC	00	MVIAL [7:0]							
1D	IND	00	NO_VIDEO	AUTO_BLUE	ICLK_DETECT		IN_PATT_EN	IN_PATT_MODE		
1E	INE	00	-		R_INV	G_INV	B_INV	RGBIN_MUX		
20	DEI0	00	-		DEINT_MODE		-	-	-	-
31	PADJ01	80	BRIGHTNESS							
32	PADJ02	80	CONTRAST							
33	PADJ03	80	SATURATION							
34	PADJ04	A0	CTIEXT	CTI_Y	HUE					
35	PADJ05	18	BKXON	BKXAUTO	YDELAY [2:0]			CTI_C	VNR	UVINV
36	PADJ06	46	BKXLVL							
37	PADJ07	64	BKXMAX							
38	PADJ08	00	BKXTPIN							
39	PADJ09	FF	BKXSLP							
3A	PADJ0A	00	BKXPCONT							
3B	PADJ0B	80	R_BRIGHTNESS							
3C	PADJ0C	80	G_BRIGHTNESS							
3D	PADJ0D	80	B_BRIGHTNESS							
3E	PADJ0E	80	R_CONTRAST							
3F	PADJ0F	80	G_CONTRAST							
40	PADJ10	80	B_CONTRAST							
41	PADJ11	60	-	CMUX_INV	SKIN_ADJ					
42	PADJ12	5F	R_LEVEL							
43	PADJ13	37	G_LEVEL							
44	PADJ14	14	B_LEVEL							
45	PADJ15	00	-				PADJ_PATT_EN	PADJ_PATT_MODE		

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
48	PEAK01	20	PEAK_EN	PEAK_CLIP_MIN						
49	PEAK02	00	-		PEAK_ADJ1					
4A	PEAK03	00	-		PEAK_ADJ2					
4B	PEAK04	00	-		PEAK_ADJ3					
4C	PEAK06	7F	-	PEAK_CLIP_MAX						
50	OSD00	20	OSD_BLINK				OSD_ALPHA			
51	OSD01	20	-		POSD	CCMODE	OSD_X2	OSDT_EN	OSDC_EN	OSDB_EN
52	OSD02	00	OSDT_MADR							
53	OSD03	04	-		OSDT_SIZEX					
54	OSD04	00	-		OSDT_POSX [9:8]		-		OSDT_POSY [9:8]	
55	OSD05	A0	OSDT_POSX [7:0]							
56	OSD06	40	OSDT_POSY [7:0]							
57	OSD07	04	OSDC_MADR							
58	OSD08	10	-		OSDC_SIZEX					
59	OSD09	08	-			OSDC_SIZEY				
5A	OSD0A	10	-		OSDC_POSX [9:8]		-	-	OSDC_POSY [9:8]	
5B	OSD0B	00	OSDC_POSX [7:0]							
5C	OSD0C	68	OSDC_POSY [7:0]							
5D	OSD0D	84	OSDB_MADR							
5E	OSD0E	08	-		OSDB_SIZEX					
5F	OSD0F	21	-		OSDB_POSX [9:8]		-	-	OSDB_POSY [9:8]	
60	OSD10	20	OSDB_POSX [7:0]							
61	OSD11	B0	OSDB_POSY [7:0]							
62	OSD12	33	OSDC_MASK_L [9:8]		OSDC_MASK_R [9:8]		OSDC_MASK_T [9:8]		OSDC_MASK_B [9:8]	
63	OSD13	01	OSDC_MASK_L [7:0]							
64	OSD14	FF	OSDC_MASK_R [7:0]							
65	OSD15	01	OSDC_MASK_T [7:0]							
66	OSD16	FF	OSDC_MASK_B [7:0]							
67	OSD17	89	CCAP_BG0				CCAP_BG1			
68	OSD18	AB	CCAP_BG2				CCAP_BG3			
69	OSD19	28	TRAN_INDEX				OSD_CP_INDEX			
6A	OSD1A	6E	OSD_CP_R							
6B	OSD1B	6E	OSD_CP_G							
6C	OSD1C	6E	OSD_CP_B							
6D	OSD1D	00	OSD_ADDR							
6E	OSD1E	00	OSD_DATA							
6F	OSD1F	00	OSD_ATRI							
70	OSD20	00	-					OSD_FONT_ADDR [10:8]		
71	OSD21	00	OSD_FONT_ADDR [7:0]							
72	OSD22	00	OSD_FONT_DATA [15:8]							
73	OSD23	00	OSD_FONT_DATA [7:0]							
75	OS00	FF	PWM0_H [15:8]							
76	OS01	FF	PWM0_H [7:0]							
77	OS02	FF	PWM1_H [15:8]							
78	OS03	FF	PWM1_H [7:0]							
79	OS04	FF	PWM0_L [15:8]							
7A	OS05	FF	PWM0_L [7:0]							
7B	OS06	FF	PWM1_L [15:8]							
7C	OS07	FF	PWM1_L [7:0]							

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
7D	OS08	F0	OS_PAT_VALUE							
7E	OS09	00	-	-		OS_PAT_EN	-	ROUT_OFF	GOUT_OFF	BOUT_OFF
7F	OS0A	00	HBLANK_OFST [4]	.	POUT_B_INV	POUT_G_INV	POUT_R_INV	POUT_RGB_MUX.		
80	OS0B	71	HBLANK_OFST[3:0]				CBLANK_EN	-	-	
81	OS0C	01	OCLKP	DOUT_OFF	VOCLKP	HSYNCP	HBLANKP	VSYNCP	VBLANKP	VOVALIDP
82	OS0D	00	OUV_INV	OFMT		CSYNC_EN	CLAMP		DITHER	
83	OS0E	10	VS_WIDTH							
84	OS0F	00	HSHIFT[7:0]							
85	OS10	00	VSHIFT[7:0]							
86	OS11	00	BOTTOM_MASK[7:0]							
87	OS12	00	TOP_MASK[7:0]							
88	OS13	00	LEFT_MASK[7:0]							
89	OS14	00	RIGHT_MASK[7:0]							
8A	OS15	00	P656_EN	CLUT_WIDTH	-	CLUT_MODE	FRM_MODE		OTRI	VOE_EN
8B	OS16	50	YSYNC_LVL							
8C	OS17	00	HS_WIDTH[8]	-	-					
8D	OS18	20	HS_WIDTH[7:0]							
8E	OS19	90	HSHIFT[10:8]			VSHIFT[10:8]			BOTTOM_MASK[9:8]	
8F	OS1A	00	TOP_MASK[9:8]		LEFT_MASK[9:8]		RIGHT_MASK[9:8]		-	-
91	MC1	00	FSTOP					-		
92	MC2	E8	MC_EN	DI_EN	-	-	-	-	-	-
A0	SC0	18	SMODE					-		
A1	SC1	70	H_ACT [7:0]							
A2	SC2	1F	H_TOTAL[7:0]							
A3	SC3	43	H_TOTAL[11:8]				H_ACT[11:8]			
A4	SC4	66	HORIZONTAL_SF							
A5	SC5	63	VERTICAL_SF[15:8]							
A6	SC6	1E	VERTICAL_SF[7:0]							
A7	SC7	02	-			-	-	-	SCLK_P	SYNC_INV
AA	SCA	80	UP_SCALE	-			-			
C0	TC0	00	OEN_MODE		STV_MODE		STV_DEL		UD	LR
C1	TC1	00	POL_ALT[11:8]				STH_START[11:8]			
C2	TC2	FC	STH_START[7:0]							
C3	TC3	08	POL_ALT[7:0]							
C4	TC4	00	LD_START[11:8]				LD_END[11:8]			
C5	TC5	0A	LD_START[7:0]							
C6	TC6	10	LD_END[7:0]							
C7	TC7	00	CKV_START[11:8]				CKV_END[11:8]			
C8	TC8	11	CKV_START[7:0]							
C9	TC9	50	CKV_END[7:0]							
CA	TC0A	00	STV_START[11:8]				STV_END[11:8]			
CB	TC0B	10	STV_START[7:0]							
CC	TC0C	30	STV_END[7:0]							
CD	TC0D	1C	STV_ON							
CE	TC0E	31	OEV_START[11:8]				OEV_END[11:8]			
CF	TC0F	E8	OEV_START[7:0]							
D0	TC10	2C	OEV_END[7:0]							

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
D1	TC11	00	-							POL_MODE
D2	TC12	00	-	OEV_P	CKV_P	STV_P	-	POL_P	LD_P	STH_P
D3	SYC0	AE	VSYNC_DEL[7:0]							
D4	SYC1	01	VD_SYN_EN	FIELD_INV	-				VSYNC_DEL[9:8]	
E0(R)	CCD0	D4	HTOTAL[10:8]			H_ACTIVE[9:8]				
E1(R)	CCD1	00	V_TOTAL[10:8]							
E2(R)	CCD2	B3	H_TOTAL[7:0]							
E3(R)	CCD3	9F	H_ACTIVE[7:0]							
E4(R)	CCD4	00	V_TOTAL[7:0]							
E5(R)	INFC11	32	HSIN_LENGTH[11:8]				HSIN_ACT[11:8]			
E6(R)	INFC12	5A	HSIN_LENGTH[7:0]							
E7(R)	INFC13	D0	HSIN_ACT[7:0]							
E8(R)	INFC14	00	-	VSIN_LENGTH[10:8]			-	VSIN_ACT[10:8]		
E9(R)	INFC15	16	VSIN_LENGTH[7:0]							
EA(R)	INFC16	01	VSIN_ACT[7:0]							
F0	PT0	30	PAT_EN	GEN_SYNC	PT_VPOL	PT_HPOL	PAT_MODE			
F1	PT1	43	PT_HLEN[11:8]				PT_HACT[11:8]			
F2	PT2	1F	PT_HLEN[7:0]							
F3	PT3	1F	PT_HACT[7:0]							
F4	PT4	22	PT_VLEN[11:8]				PT_VACT[11:8]			
F5	PT5	73	PT_VLEN[7:0]							
F6	PT6	53	PT_VACT[7:0]							
F7	PT7	80	PT_RGBVAL[7:0]							
F8	PT8	01	-		PT_INCVAL					
F9	PT9	01	PT_INTLEN							
FD	CW1	00	-	CW_DEST			-	CW_INIT_ADDR[10:8]		
FE	CW2	00	CW_INIT_ADDR [7:0]							
FF	CW3	00	CW_DATA							

15.1.2.1 GLOBAL REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
01	RST1	-	RESET / CLEAR							
02	RST2	02	-		-		OCLK_DIV			
03	RST3	F1	DEI_ON	RELX_ON	MCLK_ON	OSD_ON	D2OCLK	GPO1_EN	GPO0_EN	ACLK_ON

RESET Software reset all circuits by writing 5Ah

CLEAR Software reset all circuits other than registers by writing A5h

OCLK_DIV Output clock = (PLL2 output clock) / (OCLK_DIV[3:0]+1)

DEI_ON Deinterlace block enable

RELX_ON Scaler block enable

MCLK_ON Memory clock enable

OSD_ON OSD block enable

D2OCLK Set OCLK = DLCK

GPO1_EN GPO1_enable

GPO0_EN GPO0_enable

ACLK_ON All PLL clocks enable

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
04	GBL0	1C	-	DVLK_INV	GPO1_SEL			GPO0_SEL		
05	GBL1	01	TCON_EN	VOHS_SEL	-	-		GPO2_SEL		

DCLK_INV Inverse dclk

GPO1_SEL, GPO2_SEL
GPO0_SEL General-purpose output pin function selection. For configuration details see Table 15.2.1.1.

Table 15.2.1.1 GPO_SEL and GPO signal

GPO2_SEL	GPO2	GPO1_SEL	GPO1	GPO0_SEL	GPO0
0	HBLANK	**0**	HBLANK	**0 (df.)**	HBLANK
1(df.)	GCSYNC	**1**	GCSYNC	**1**	GCSYNC
2	VBLANK	**2**	VBLANK	**2**	VBLANK
3	PWM0	**3(df.)**	PWM0	**3**	PWM0
4	PWM1	**4**	PWM1	**4(df.)**	PWM1
5	VOVALID	**5**	VOVALID	**5**	VOVALID
6	0	**6**	0	**6**	0
7	1	**7**	1	**7**	1

TCON_EN Enable the Timing Controller function, and I/O pins

VOHS_SEL Select the output hsync type

0 : general horizontal sync

1 : Composite horizontal sync, depend on GPO2_SEL

15.1.2.2 INPUT FORMAT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10	IN0	20	NTCPAL	VICLKP	AUTO_NP	SET_NP	VICLKF	SQ_EN	UVFMT	-
11	IN1	00	INFMT			INSYN		VIHSP	-	VIVSP/ VIFDP
12	IN2	00	VIHS_OFST [7:0]							
13	IN3	03	V4_UV_IN V	INFIELD_I NV	-	MIL_EN	MHIL[11:8]			
14	IN4	5A	MHIL[7:0]							
15	IN5	8A	MHSL							
16	IN6	00	VIVS_OFST [7:0]							
17	IN7	00	PG_IN	PASS_DEI NT	VIVS_OFST [10:8]			VIHS_OFST [10:8]		
18	IN8	28	VSYNC_LEN					MVIL[10:8]		
19	IN9	00	MVIL[7:0]							
1A	INA	00	INFC_PAT		MVIAL[10:8]			MHIAL[10:8]		
1B	INB	00	MHIAL[7:0]							
1C	INC	00	MVIAL[7:0]							
1D	IND	00	NO_VIDEO	AUTO_BLUE	ICLK_DETECT		INFC_PATT _EN	INFC_PATT_MODE		
1E	INE	00	-	-	R_INV	G_INV	B_INV	RGBIN_MUX		

NTSCPAL

0 Input video is in NTSC format (read only)

1 Input video is in PAL format (read only)

VICLKP	0	Normal (df.)
	1	Inverse VICLK pin polarity
AUTO_NP	0	Manually setting input video standard from register SET_NP
	1	Auto-detecting input video standard (df.)
SET_NP	0	Manually setting input standard to NTSC (df.)
	1	Manually setting input standard to PAL
VICLKF	0	VICLK is 2x input data rate
	1	VICLK is 1x input data rate (df.)
SQ_EN	0	Non-square-pixel mode (df.)
	1	Square-pixel mode
UVFMT	0	Un-sign (df.)
	1	Sign
INFMT[2:0]	Video input format	
	0	8-bit ITU-R BT.656
	1	8-bit YUV + VIHS/VIVS/VIFIELD : ITU-R BT.601
	2	16-bit Y/UV + VIHS + VIVS
	3	24-bit YUV progressive input
	6	CCD bayer format input
	7	24-bit RGB progressive input
INSYN[1:0]	Video input synchronization format	
	0	Equaled VIVS (262.5 VIHSs per VIVS) (df.)
	1	Non-equaled VIVS (262/263 VIHSs per VIVS)
	2	Equaled VIFIELD (262.5 VIHSs per VIFIELD)
	3	Non-equaled VIFIELD (262/263 VIHSs per VIFIELD)
VIHSP	Pin VIHS polarity	
VIVSP / VIFDP	Pin VIVS / VIFD polarity	

VIHS_OFST[10:0]	Offset for screening valid video input data in each line
VIVS_OFST[10:0]	Offset for screening valid video input lines in each field
V4_UV_INV	Inverse input video U/V data
INFIELD_INV	Inverse the input filed signal
MIL_EN	Manually setting length of input signal enable
MHIL[11:0]	Manually setting period of VIHS value
MHSL[7:0]	Manually setting sync-length of VIHS value (Interlace Only)
MHIAL[10:0]	Manually setting active-length of VIHS value (Progressive only)
MVIL[10:0]	Manually setting period of VIVS value
MVIAL[10:0]	Manually setting active-length of VIVS value
INFC_PAT[1:0]	input format color pattern select 0 Normal 1 Y only 2 C only 3 Blue screen
NO_VIDEO	No Video signal input, when there exist VICLK, read only.
AUTO_BLUE	Auto set to blue screen, when NO_VIDEO detected.
ICLK_DETECT[1:0]	The auto_detect input clock result : 0 No input clock found 1 VICLK detected 2 RGBINCLK detected 3 XTALIN detected

PG_IN Input signal is progressive not interlace

PASS_DEINT Pass the deinterlace block, used for progressive input

INFC_PATT_EN Enable the input pattern generation

INFC_PATT_MODE[3:0] Select the input pattern generation type

0 gray frame
1 increase 1 each 1 clock vertical bar
2 increase 1 every 2 clock vertial bar
3 increase 1 every 4 clock vertial bar
4 increase 1 every 8 clockl vertial bar
5 color bar

R_INV Invert the RIN[7:0] input pin order to [0:7]

G_INV Invert the GIN[7:0] input pin order to [0:7]

B_INV Invert the BIN[7:0] input pin order to [0:7]

RGBIN_MUX[2:0] Swap the RIN,GIN,BIN input data bus.

RGBIN_MUX	R	G	B
0	R	G	B
1	R	B	G
2	G	R	B
3	G	B	R
4	B	R	G
5	B	G	R
6	R	R	R
7	G	G	G

15.1.2.3 DEINTERLACE REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
20	DEI0	00	-		DEINT_MODE		-	-	-	-

DEINT_MODE Deinterlace operating mode

0 Motion-adaptive 3D deinterlace mode

1 Inter-field interpolation mode

2 Intra Edge-preserving pixel interpolation mode

3 Reserved

15.1.2.4 PICTURE ADJUSTMENT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
31	PADJ01	80	BRIGHTNESS							
32	PADJ02	80	CONTRAST							
33	PADJ03	80	SATURATION							
34	PADJ04	A0	CTIEXT	CTI_Y	HUE					
35	PADJ05	18	BKXON	BKXAUTO	YDELAY [2:0]			CTI_C	VNR	UVINV

BRIGHTNESS Brightness adjustment

CONTRAST Contrast adjustment

SATURATION Saturation adjustment

HUE Hue adjustment

YDELAY[2:0] Offset between Y and C, for engineering usage

CTIEXT CTI mode select

CTI_Y Color transient improvement (CTI) enable for Y

CTI_C Color transient improvement (CTI) enable for C

VNR Video noise reduction (VNR) enable

UVINV UV inversion

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
35	PADJ05	18	BKXON	BKXAUTO	YDELAY [2:0]			CEN	VNR	UVINV
36	PADJ06	46	BKXLVL							
37	PADJ07	64	BKXMAX							
38	PADJ08	00	BKXTPIN							
39	PADJ09	FF	BKXSLP							
3A (R)	PADJ0A	00	BKXPCONT							

BKXON Black-level extension (BLE) enable

BKXAUTO
0 Manually setting black-level extension
1 Automatically setting black-level extension

BKXLVL Black-level threshold. Luminance below the value is considered as black.

BKXMAX The maximum location of adaptive turnaround point

BKXTPIN Parameter for manually setting black-level extension

BKXSLP The slope of the transform function in BLE section

BKXPCONT Readout parameter for manually setting black-level extension

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
3B	PADJ0B	80	R_BRIGHTNESS							
3C	PADJ0C	80	G_BRIGHTNESS							
3D	PADJ0D	80	B_BRIGHTNESS							
3E	PADJ0E	80	R_CONTRAST							
3F	PADJ0F	80	G_CONTRAST							
40	PADJ10	80	B_CONTRAST							

R_BRIGHTNESS R channel output brightness adjustment

G_BRIGHTNESS G channel output brightness adjustment

B_BRIGHTNESS B channel output brightness adjustment

R_CONTRAST R channel output contrast adjustment

G_CONTRAST G channel output contrast adjustment

B_CONTRAST B channel output contrast adjustment

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
41	PADJ11	60	-	CMUX_INV	SKIN_ADJ					
42	PADJ12	5F	R_LEVEL							
43	PADJ13	37	G_LEVEL							
44	PADJ14	14	B_LEVEL							
45	PADJ15	00	-				PADJ_PATT_EN	PADJ_PATT_MODE		

CMUX_INV Skin tone Cb/Cr change

SKIN_ADJ Skin tone region enhancement level

R_LEVEL Red threshold for skin tone adjustment

G_LEVEL Green threshold for skin tone adjustment

B_LEVEL Blue threshold for skin tone adjustment

PADJ_PATT_EN Enable PADJ patten generation output

PADJ_PATT_MODE Select the PADJ pattern generation type

0 gray frame
1 increase 1 each 1 clock vertical bar
2 increase 1 every 2 clock vertial bar
3 increase 1 every 4 clock vertial bar
4 increase 1 every 8 clockl vertial bar
5 color bar

15.1.2.5 PICTURE ADJUSTMENT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
48	PEAK01	20	PEAK_EN	PEAK_CLIP_MIN						
49	PEAK02	00	-	-	PEAK_ADJ1					
4A	PEAK03	00	-	-	PEAK_ADJ2					
4B	PEAK04	00	-	-	PEAK_ADJ3					
4C	PEAK06	7F	-	PEAK_CLIP_MAX						

PEAK_EN Horizontal sharpening enable

PEAK_CLIP_MIN Clipping filter parameter

PEAK_ADJ1 Weighting of horizontal video sharpening in high-frequency

PEAK_ADJ2 Weighting of horizontal video sharpening in mid-frequency

PEAK_ADJ3 Weighting of horizontal video sharpening in low-frequency

PEAK_CLIP_MAX Clipping filter parameter

15.1.2.6 OSD REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
50	OSD00	20	OSD_BLINK				OSD_ALPHA			
51	OSD01	20	-	-	POSD	CCMODE	OSD_X2	OSDT_EN	OSDC_EN	OSDB_EN

OSD_BLINK OSD blinking rate

$$\text{OSD Blinking Rate} = \frac{30}{\text{OSD\_BLINK} \times 4}\ \text{Hz}$$

OSD_ALPHA OSD alpha-blending. See following equation.
OSD_ALPHA [3:2] for foreground; OSD_ALPHA [1:0] for background.

$$\text{OSD Displaying Color} = \frac{\text{Video Color} \times \text{OSD\_ALPHA} + \text{OSD Color} \times (4 - \text{OSD\_ALPHA})}{4}$$

POSD

0 Interlaced OSD

1 Progressive OSD

CCMODE

Command memory configuration

0 COLR Mode

1 CCAP Mode

OSD_X2

OSD font-size selection

0 Small font (16 pixel x 20 pixel)

1 Large font (32 pixel x 40 pixel)

OSDT_EN

OSD title block display enable

OSDC_EN

OSD content block display enable

OSDB_EN

OSD bar block display enable

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
52	OSD02	00	OSDT_MADR							
53	OSD03	04	-	-	OSDT_SIZEX					
54	OSD04	00	-	-	OSDT_POSX [9:8]		-	-	OSDT_POSY [9:8]	
55	OSD05	A0	OSDT_POSX [7:0]							
56	OSD06	40	OSDT_POSY [7:0]							

OSDT_MADR

OSD title block initial address in OSD command memory

OSDT_SIZEX

OSD title block horizontal length in character. Valid settings are 01h – 26h for small fonts; 01h – 13h for large fonts.

OSDT_POSX

OSD title block horizontal initial position. Incrementing by 1 reflects 1 pixels shifting rightwards. Minimum value is 03h.

OSDT_POSY

OSD title block vertical initial position. Incrementing by 1 reflects 1

lines shifting downwards. Minimum value is 01h.

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
57	OSD07	04	OSDC_MADR							
58	OSD08	10	-	-	OSDC_SIZEX					
59	OSD09	08	-	-	-	OSDC_SIZEY				
5A	OSD10	10	-	-	OSDC_POSX [9:8]		-	-	OSDC_POSY [9:8]	
5B	OSD11	00	OSDC_POSX [7:0]							
5C	OSD12	68	OSDC_POSY [7:0]							

OSDC_SIZEX OSD content block horizontal length in character

OSDC_SIZEY OSD content block vertical length in character. Valid settings are 01h – 15h for small fonts; 01h – 0Ah for large fonts.

OSDC_MADR OSD content block initial address in OSD command memory

OSDC_POSX OSD content block horizontal initial position. Incrementing by 1 reflects 1 pixels shifting rightwards. Minimum value is 03h.

OSDC_POSY OSD content block vertical initial position. Incrementing by 1 reflects 1 lines shifting downwards. Minimum value is 01h.

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
5D	OSD13	84	OSDB_MADR							
5E	OSD14	08	-	-	OSDB_SIZEX					
5F	OSD15	21			OSDB_POSX [9:8]		-	-	OSDB_POSY [9:8]	
60	OSD16	20	OSDB_POSX [7:0]							
61	OSD17	B0	OSDB_POSY [7:0]							

OSDB_SIZEX OSD bar block horizontal length in character

OSDB_MADR OSD bar block initial address in OSD command memory

OSDB_POSX OSD bar block horizontal initial position. Incrementing by 1 reflects 1 pixels shifting rightwards. Minimum value is 03h.

OSDB_POSY OSD bar block vertical initial position. Incrementing by 1 reflects 1 lines shifting downwards. Minimum value is 01h.

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
62	OSD18	33	OSDC_MASK_L [9:8]		OSDC_MASK_R [9:8]		OSDC_MASK_T [9:8]		OSDC_MASK_B [9:8]	
63	OSD19	01	OSDC_MASK_L [7:0]							
64	OSD20	FF	OSDC_MASK_R [7:0]							
65	OSD21	01	OSDC_MASK_T [7:0]							
66	OSD22	FF	OSDC_MASK_B [7:0]							

OSDC_MASK_L OSD content block masking boundary location for left-hand-side

OSDC_MASK_R OSD content block masking boundary location for right-hand-side

OSDC_MASK_T OSD content block masking boundary location for top side

OSDC_MASK_B OSD content block masking boundary location for bottom side

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
67	OSD23	89	CCAP_BG0				CCAP_BG1			
68	OSD24	AB	CCAP_BG2				CCAP_BG3			

CCAP_BG0 OSD background color 0 in CCAP mode

CCAP_BG1 OSD background color 1 in CCAP mode

CCAP_BG2 OSD background color 2 in CCAP mode

CCAP_BG3 OSD background color 3 in CCAP mode

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
69	OSD25	28	TRAN_INDEX				OSD_CP_INDEX			
6A	OSD26	6E	OSD_CP_R							
6B	OSD27	6E	OSD_CP_G							
6C	OSD28	6E	OSD_CP_B							

TRAN_INDEX Define color palette index in which stands for transparent color

OSD_CP_INDEX Specify color index in color palette

OSD_CP_R Setting color R to which index specified in OSD_CP_INDEX

OSD_CP_G Setting color G to which index specified in OSD_CP_INDEX

OSD_CP_B Setting color B to which index specified in OSD_CP_INDEX

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
6D	OSD29	00	OSD_ADDR							
6E	OSD30	00	OSD_DATA							
6F	OSD31	00	OSD_ATRI							
70	OSD32	00	-	-	-	-	-	OSD_FONT_ADDR [10:8]		
71	OSD33	00	OSD_FONT_ADDR [7:0]							
72	OSD34	00	OSD_FONT_DATA [15:8]							
73	OSD35	00	OSD_FONT_DATA [7:0]							

OSD_ADDR OSD command memory address

OSD_DATA OSD command memory data

OSD_ATRI OSD command memory attribute

OSD_FONT_ADDR OSD font memory address

OSD_FONT_DATA OSD font memory data

15.1.2.7 OUTPUT FORMAT REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
75	OS00	FF	PWM0_H [15:8]							
76	OS01	FF	PWM0_H [7:0]							
77	OS02	FF	PWM1_H [15:8]							
78	OS03	FF	PWM1_H [7:0]							
79	OS04	FF	PWM0_L [15:8]							
7A	OS05	FF	PWM0_L [7:0]							
7B	OS06	FF	PWM1_L [15:8]							
7C	OS07	FF	PWM1_L [7:0]							

PWM0_H Number of clocks in logic-1 for PWM0 signal

PWM0_L Number of clocks in logic-0 for PWM0 signal

PWM1_H Number of clocks in logic-1 for PWM1 signal

PWM1_L Number of clocks in logic-0 for PWM1 signal

PWM0 and PWM1 are available at GPO pins. See register description for GPO1_SEL, and GPO2_SEL for GPO settings.

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
7D	OS08	F0	OUT_PAT_VAL							
7E	OS09	00				OS_PAT_EN	-	ROUT_OFF	GOUT_OFF	BOUT_OFF
7F	OS0A	00	HBLANK_OFST [4]	-	OUT_B_INV	OUT_G_INV	OUT_R_INV	OUT_RGB_MUX		
80	OS0B	71	HBLANK_OFST[3:0]				CBLANK_EN	LCDPWR_EN	LCDPWR_DLY	
81	OS0C	01	OCLKP	DOUT_OFF	-	HSYNCP	HBLANKP	VSYNCP	VBLANKP	VOVALIDP
82	OS0D	00	OUV_INV	OFMT		CSYNC_EN	CLAMP		DITHER	
83	OS0E	10	VS_WIDTH							
84	OS0F	00	HSHIFT[7:0]							
85	OS10	00	VSHIFT[7:0]							
86	OS11	00	BOTTOM_MASK[7:0]							
87	OS12	00	TOP_MASK[7:0]							
88	OS13	00	LEFT_MASK[7:0]							
89	OS14	00	RIGHT_MASK[7:0]							
8A	OS15	00	P656_EN	CLUT_WIDTH	-	CLUT_MODE	FRM_MODE		OTRI	VOE_EN
8B	OS16	50	YSYNC_LVL							
8C	OS17	00	HS_WIDTH [8]	-	-					
8D	OS18	20	HS_WIDTH[7:0]							
8E	OS19	90	HSHIFT[10:8]			VSHIFT[10:8]			BOTTON_MASK[9:8]	
8F	OS1A	00	TOP_MASK[9:8]		LEFT_MASK[9:8]		RIGHT_MASK[9:8]		-	-

OUT_PAT_VAL Output pattern value : P

OUT_PAT_EN Enable output internal building RGB pattern

OUT_PAT_MODE RGB building pattern mode select

OUT_PAT_MODE	R	G	B
0	0	0	0

1	0	0	P
2	0	P	0
3	0	P	P
4	P	0	0
5	P	0	P
6	P	P	0
7	P	P	P

OUT_RGB_MUX RGB output pin mux select

OUT_RGB_MUX	R	G	B
0	R	G	B
1	B	G	R
2	G	R	B
3	B	R	G
4	G	B	R
5	R	B	G
6	G	G	G
7	R	R	R

ROUT_OFF Set the ROUT value to 0

GOUT_OFF Set the GOUT value to 0

BOUT_OFF Set the BOUT value to 0

OUT_R_INV Inverse the DR[7:0] output pin 7~0 to 0~7

OUT_G_INV Inverse the DG[7:0] output pin 7~0 to 0~7

OUT_B_INV Inverse the DB[7:0] output pin 7~0 to 0~7

CBLANK_EN CBLANK on pin HBLANK enable

HBLANK_OFST[4:0] HBLANK offset value, df=7

LCDPWR_EN LCD power-on delay enable

LCDPWR_DLY LCD power-on delay adjustment

0 32 horizontal lines (0.5 ~ 1 ms)

1 65 horizontal lines (1 ~ 2 ms)

2 130 horizontal lines (2 ~ 4 ms)

3 260 horizontal lines (4 ~ 8 ms)

OCLKP Internal Output clock polarity

DOUT_OFF Digital video output disable

HSYNCP Pin HSYNC polarity

HBLANKP HBLANK (on GPO pin) polarity

VSYNCP Pin VSYNC polarity

VBLANKP VBLANK (on GPO pin) polarity

VOVALIDP VOVALID (on GPO pin) polarity

OUV_INV Inverse the Cb/Cr value

OFMT Progressive video output format; see *Table 15.2.5.1.*

Table 15.2.5.1

	OFMT	Output Format
Digital Port	0	3-Channel RGB
	1	3-Channel 4:4:4 YPbPr (with embedded horizontal and vertical synchronization on Y
	2	2-Channel 4:2:2 YUV (with additional HSYNC and VSYNC pins)
	3	3-Channel 4:4:4 YUV (with additional HSYNC and VSYNC pins)

CSYNC_EN Enable the composite sync on hsync

CLAMP Video output data clamping control

0 Disable. Video output is in the range of 0 – 255.

1 Video output is in the range of 16 – 235 (Y), 16 – 240 (UV)

2 Video output is in the range of 1 – 254.

3 Reserved

DITHER Video output data dithering control; see *Table 17.2.5.2*.

Table 17.2.5.2

DITHER	Dithering Option (G/Y:B/Pb/U:R/Pr/V)	DITHER	Dithering Option (G/Y:B/Pb/U:R/Pr/V)
0	Disable	**2**	Dithering to 24-bits (8-bits : 8-bits : 8-bits)
1	Dithering to 18-bits (6-bits : 6-bits : 6-bits)	**3**	Dithering to 16-bits (6-bits : 5-bits : 5-bits)

HS_WIDTH[8:0] Width of video output horizontal synchronization

Actual synchronization-width = 13 + (HS_WIDTH x 4) in pixels

VS_WIDTH[7:0] Width of video output vertical synchronization

Actual synchronization-width = 1 + VS_WIDTH in lines

HSHIFT[10:0] Video output horizontal shifting

VSHIFT[10:0] Video output vertical shifting

BOTTOM_MASK[9:0] Number of lines masked from the bottom of a frame

TOP_MASK[9:0] Number of lines masked from the top of a frame

LEFT_MASK[9:0] Number of pixels masked from the left-hand-side of a frame

RIGHT_MASK[9:0] Number of pixels masked from the right-hand-side of a frame

CLUT_WIDTH Color Look-Up Table (CLUT) data-width selection

0 8-bit

1 10-bit

CLUT_MODE

0 No CLUT

1 Using 3-channel RAM as CLUT

P656_EN Enable progressive 656 output

FRM_MODE Output frame frequency mode
00 frame_rate
01 frame_rate/2
02 frame_rate/4

OTRI Video outputs high impedance enable
When OTRI is on, the digital video outputs, DR_V, DG_Y, DB_U, EXV, HSYNC, VSYNC, HBLANK, VBLANK, VOVALID, GPO0, GPO1, GPO2, and VOCLK, are forced high impedence.

YSYNC_LVL The depth of Y synchronization in YPbPr output mode

VAL_STEP The step size of pattern value

15.1.2.8 SDRAM INTERFACE REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
91	MC1	00	FSTOP	-				-	-	-
92	MC2	E8	MC_EN	DI_EN	-	-	-			

FSTOP Stop updating frame memory

MC_EN Memory interface enable

DI_EN Memory interface 3D deinterlace port enable

15.1.2.9 RELÁCS REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
A0	SC0	18	SMODE					-		
A1	SC1	70	H_ACT [7:0]							
A2	SC2	1F	H_TOTAL[7:0]							
A3	SC3	43	H_TOTAL[11:8]				H_ACT[11:8]			
A4	SC4	66	HORIZONTAL_SF							
A5	SC5	63	VERTICAL_SF[15:8]							
A6	SC6	1E	VERTICAL_SF[7:0]							
A7	SC7	02	-					-	SCLK_P	SYNC_INV
AA	SCA	80	UP_SCALE							

SMODE Scaling mode selection

0 1x Scaling

1 Down-scaling to 60Hz VGA (640 x 480)

2 Up-Scaling to SVGA (800 x 600)

3 Up-Scaling to XGA (1024 x 768)

4 Up-Scaling to SXGA (1280 x 1024)

5 Up-Scaling to 720P (1280 x 720)

6 Up-Scaling to WSVGA (1366 x 768)

7 Up-Scaling to WVGA (1600x1200)

8 Up-Scaling to 1080P (1920x1080)

9 Up-Scaling to WVGA (800 x 480)

10 – 15 Manual setting

H_ACT[11:0] Manual setting horizontal active length

H_TOTAL[11:0] Manual setting horizontal total length

UP_SCALE horizontal and vertical up-scaling function enable

H_SF[7:0] horizontal scaling factor 1

V_SF[15:0] vertical scaling factor 1

SCLK_P SCLK polarity

SYNC_INV For scaler adjustment

15.1.2.10 TCON REGISTERS

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
C0	TC0	00	OEV_MODE		STV_MODE		STV_DEL		UD	LR
C1	TC1	00	POL_ALT[11:8]				STH_START[11:8]			
C2	TC2	FC	STH_START[7:0]							
C3	TC3	08	POL_ALT[7:0]							
C4	TC4	00	LD_START[11:8]				LD_END[11:8]			
C5	TC5	0A	LD_START[7:0]							
C6	TC6	10	LD_END[7:0]							
C7	TC7	00	CKV_START[11:8]				CKV_END[11:8]			
C8	TC8	11	CKV_START[7:0]							
C9	TC9	50	CKV_END[7:0]							
CA	TC10	00	STV_START[11:8]				STV_END[11:8]			
CB	TC11	10	STV_START[7:0]							
CC	TC12	30	STV_END[7:0]							
CD	TC13	1C	STV_ON							
CE	TC14	31	OEV_START[11:8]				OEV_END[11:8]			
CF	TC15	E8	OEV_START[7:0]							
D0	TC16	2C	OEV_END[7:0]							
D1	TC17	00	-							POL_MODE
D2	TC18	00	-	OEV_P	CKV_P	STV_P	-	POL_P	LD_P	STH_P

OEV_MODE Select OEV signal type (df. = 00)

STV_MODE Select STV pulse type (df. = 00)

STV_DLY Set delay of STV pulse in unit of a scan line (df. = 0)

UD Up/Down scan control

LR Left/Right scan control

POL_ALT POL alternates time

STH_START STHR/STHL pulse starts time

LD_START LD pulse starts time

LD_END LD pulse ends time

CKV_START CKV rising time

CKV_END	CKV falling time
STV_START	STVL/STVR pulse starts time (df. = 0)
STV_END	STVL/STVR pulse ends time (df. = 0)
STV_ON	Set the scan line on which STV pulse exist (df. = 0)
OEV_START	OEV pulse starts point
OEV_END	OEV pulse ends point
POL_MODE	0: POL alternates per 1-H trigger (df.) 1: POL alternates per 2-H trigger
OEV_P	To invert OEV pulse
CKV_P	To invert CKV pulse
STV_P	To invert STVL/STVR pulse
POL_P	To invert POL signal
LD_P	To invert LD signal
STH_P	To invert STHL/STHR pulse

15.1.2.11 SDRAM BYPASS REGISTERS

Addr.	Name	Def.	Bit Map

(Hex)		(Hex)	7	6	5	4	3	2	1	0
D3	SY0	AE	VSYNC_DEL[7:0]							
D4	SY1	01	VD_SYN_EN	VFIELD_INV	-				VSYNC_DEL[9:8]	

VSYNC_DEL[9:0] Delay of input VSYNC

VD_SYN_EN Enable bypass sdram mode

VFIELD_INV Inverse input video field signal

15.1.2.12 CCD IN READ REGISTER

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
E0	CCD0	D4	H_TOTAL[10:8]			H_ACTIVE[10:8]				
E1	CCD1	00	V_TOTAL[10:8]			-				
E2	CCD2	B3	H_TOTAL[7:0]							
E3	CCD3	9F	H_ACTIVE[7:0]							
E4	CCD4	00	V_TOTAL[7:0]							

H_TOTAL[10:0] total pixel of CCD input horizontal line

H_ACTIVE[10:0] active pixel of CCD horizontal line

V_TOTAL[10:0] total line of CCD vertical

15.1.2.13 INPUT SIGNAL SIZE REGISTER (READ)

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
E5(R)	INFC11	32	HSIN_LENGTH[11:8]				HSIN_ACT[11:8]			
E6(R)	INFC12	5A	HSIN_LENGTH[7:0]							
E7(R)	INFC13	D0	HSIN_ACT[7:0]							
E8(R)	INFC14	00	-	VSIN_LENGTH[10:8]			-	VSIN_ACT[10:8]		
E9(R)	INFC15	16	VSIN_LENGTH[7:0]							
EA(R)	INFC16	01	VSIN_ACT[7:0]							

HSIN_LENGTH[11:0] Input Horizontal line total length

HSIN_ACT[11:0] Input Horizontal line active length

VSIN_LENGTH[10:0] Input vertical total line count

VSIN_ACT[10:0] Input vertical active line count

15.1.2.14 MEDIAN FILTER CONTROL REGISTER

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
EB	MED0	00	MED_EN	MED_MODE						
EC	MED1	80	MED_TH							

MED_EN Enable median filter

MED_MODE Median filter mode select

MED_TH Threshold for median filter use

15.1.2.15 OUTPUT PATTERN GENERATION CONTROL REGISTER

Addr. (Hex)	Name	Def. (Hex)	Bit Map							
			7	6	5	4	3	2	1	0
F0	PT0	30	PAT_EN	GEN_SYNC	PT_VPOL	PT_HPOL	PAT_MODE			
F1	PT1	43	PT_HLEN[11:8]				PT_HACT[11:8]			
F2	PT2	1F	PT_HLEN[7:0]							
F3	PT3	1F	PT_HACT[7:0]							
F4	PT4	22	PT_VLEN[11:8]				PT_VACT[11:8]			
F5	PT5	73	PT_VLEN[7:0]							
F6	PT6	53	PT_VACT[7:0]							
F7	PT7	80	PT_RGBVAL[7:0]							
F8	PT8	01	-		PT_INCVAL					
F9	PT9	01	PT_INTLEN							

PAT_EN Enable Internal pattern generation

GEN_SYNC 0 use original setting for sync length

1 Use user setting register(F1~F7) value to generate

horizontal/vertical total length and sync length

PT_VPOL output vsync polarity

PT_HPOL output hsync polarity

PAT_MODE Setting the pattern mode

0 Pure color
1 Horizontal increment value line
2 Vertical increment value line
3 Boundary and center line
4 Grid line
5 Color bar of horizontal direction
6 Color bar of vertical direction

PT_HLEN[11:0] output horizontal total length

PT_HACT[11:0] output horizontal active length

PT_VLEN[11:0] output vertical total length

PT_VACT[11:0] output vertical active length

PT_RGBVAL[7:0] output pattern value

PT_INCVAL The incremental value of pattern generation

PT_INTLEN The interval length of pattern increase

15.1.2.16 CONTINUOUS WRITE REGISTERS

Addr.	Name	Def.	Bit Map

(Hex)		(Hex)	7	6	5	4	3	2	1	0
FD	CW1	00	-	CW_DEST			-	CW_INIT_ADDR [10:8]		
FE	CW2	00	CW_INIT_ADDR [7:0]							
FF	CW3	00	CW_DATA							

CW_DEST Continuous write destination selection

0 None
1 OSD command memory index
2 OSD font memory
3 CLUT R / Pr
4 CLUT G / Y
5 CLUT B / Pb
6 CLUT all
7 OSD command memory attribute

CW_INIT_ADDR Continuous write initial address

CW_DATA Continuous write data

16 ELECTRICAL CHARACTERISTICS

16.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage For Digital Core (1.8V Nominal)	V_{CCC}	-0.5	2.3	V
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	-0.5	4.0	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	-0.5	4.0	V
Input Voltage For Digital I/O (5V Tolerant)	V_{ID}	-0.5	V_{DDD} + 0.5	V
Input Voltage For Analog Core	V_{IA}	-0.5	V_{DDA} + 0.5	V
Junction Temperature	T_J	-40	125	°C
Storage Temperature	T_{STG}	-55	125	°C
Lead Temperature (Vapor Phase Soldering, 40 Seconds)	T_L	-	215	°C
Electronic Discharge	T_{ESD}	-2000	2000	V

16.2 RECOMMENDED OPERATING CONDITIONS

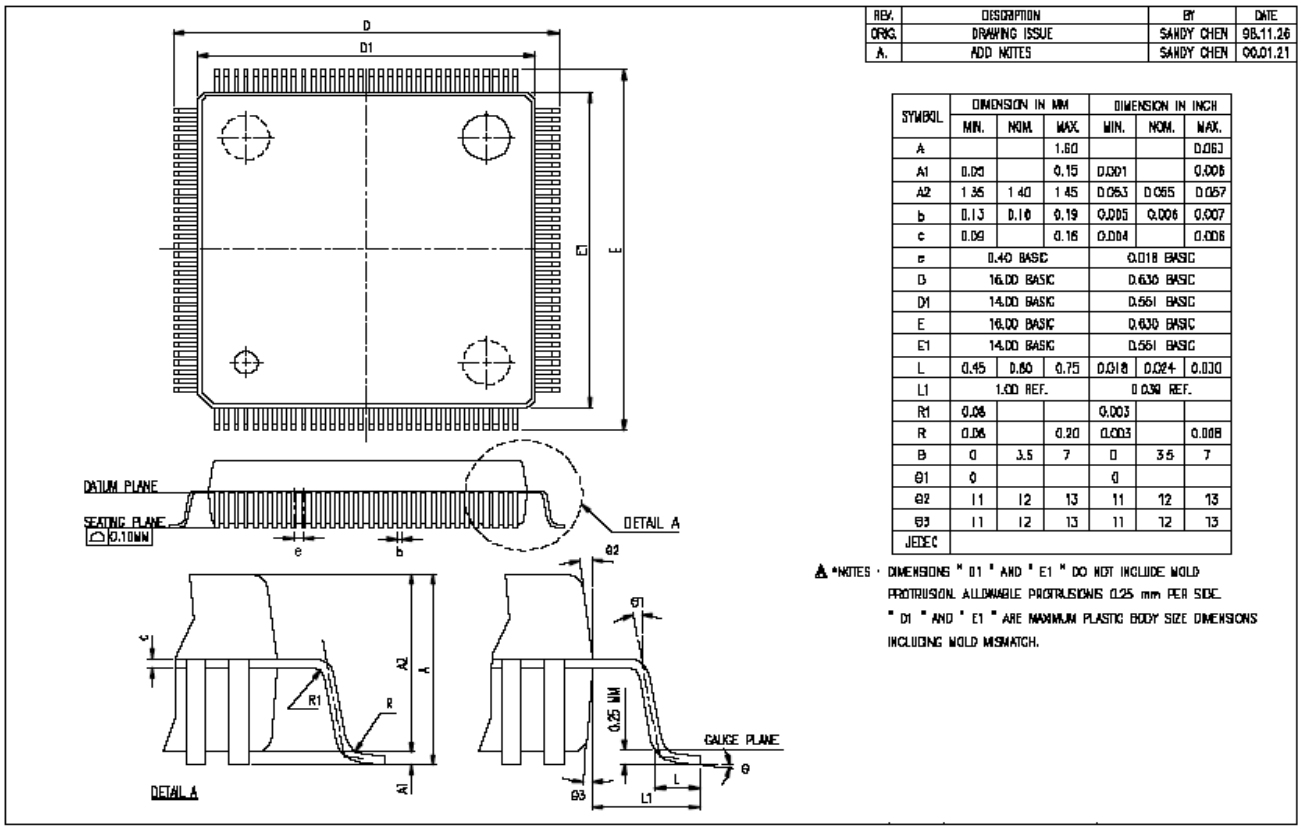
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage For Digital Core (1.8V Nominal)	V_{CCC}	1.5	1.8	2.1	V
Supply Voltage For Digital I/O (3.3V Nominal)	V_{DDD}	3.0	3.3	3.6	V
Supply Voltage For Analog Core (3.3V Nominal)	V_{DDA}	3.1	3.3	3.5	V
Ambient Operation Temperature	T_A	0	-	70	°C
Package Case Temperature	T_A	-	-	115	°C
Total Power Dissipation	P_{TOT}	-	TBA	-	W

16.3 DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input (I, I_S, I_{PU}, I_{PD})					
High Level Input Voltage	V_{IH}	0.65 V_{DDD}	-	-	V
Low Level Input Voltage	V_{IL}	-	-	0.35V_{DDD}	V
Leakage Current[1]	I_L	0	-	500	µA
Output (O_1, O_{TS1})					
High Level Output Voltage	V_{OH}	2.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.4	V
Tri-State Output Leakage Current	I_L	-25	-	25	µA
Input/TTL Output (I/O_1, I/O_2)					
High Level Input Voltage	V_{IH}	0.65 V_{DDD}	-	-	V
Low Level Input Voltage	V_{IL}	-	-	0.35V_{DDD}	V
High Level Output Voltage	V_{OH}	2.4	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.4	V
Pull-Up/Down Resistor					
Pull-Up Resistor	R_{PU}	59	74	94	Ωk
Pull-Down Resistor	R_{PD}	63	77	97	Ωk

[1] No leakage current flown when input voltage is V_{DDD} or 0. The maximum occurs at transitions.

17 PACKAGE



REV.	DESCRIPTION	BY	DATE
ORG.	DRAWING ISSUE	SANDY CHEN	98.11.26
A.	ADD NOTES	SANDY CHEN	00.01.21

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.19	0.005	0.006	0.007
c	0.09		0.16	0.004		0.006
e	0.40 BASIC			0.016 BASIC		
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.551 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC						

⚠ *NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSIONS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.