

UVC 3130
High-Speed
A/D-D/A Converter

www.DataSheet4U.com

High-Speed A/D-D/A Converter

VLSI circuit in CI technology, featuring the following circuits:

- a high-speed flash type 8-bit A/D converter
- a high-speed low-glitch 10-bit D/A converter, designed as an R-2R network with switched current sources
- various auxiliary circuits, such as reference voltage sources, preamplifier, input clamping circuit, and feed-in output amplifier

UVC 3130 has been developed for use in all applications which call for a high-speed A/D-D/A converter. For instance, the device can be used to advantage to decode television signals in Pay-TV converters or for D2-MAC converters used in direct satellite broadcast. Other promising applications can be seen in industrial electronics, e. g. in conjunction with digital signal processing. Although UVC 3130 was initially designed as high-speed codec for the video-range, it can be used with equal benefits for lower frequencies, even down to zero.

1. General Information

The above auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input, in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of that circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected. Further, the input is equipped with switches which optionally provide operation with keyed clamping or peak clamping (see also section 6.).

Also the D/A converter's reference voltage is generated on-chip, and a gated amplifier is arranged at the output of the D/A converter so that an external analog signal can be fed in instead of the signal delivered by the D/A converter.

Separate clock inputs are provided for the A/D converter and the D/A converter thus enabling the application of time compression procedures. All inputs and outputs are TTL compatible.

2. Outline Dimensions and Pin Connections

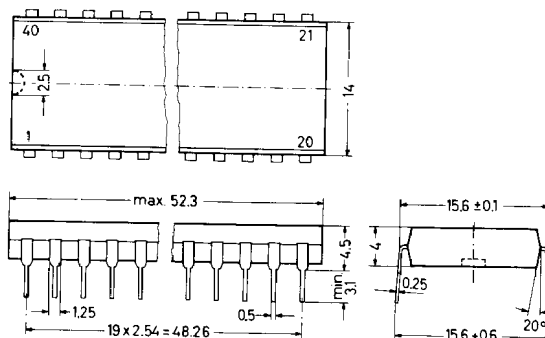


Fig. 2:
UVC 3130 in 40-pin DIP Plastic Package,
20 B 40 according to DIN 41870

Weight approx. 6 g
Dimensions in mm

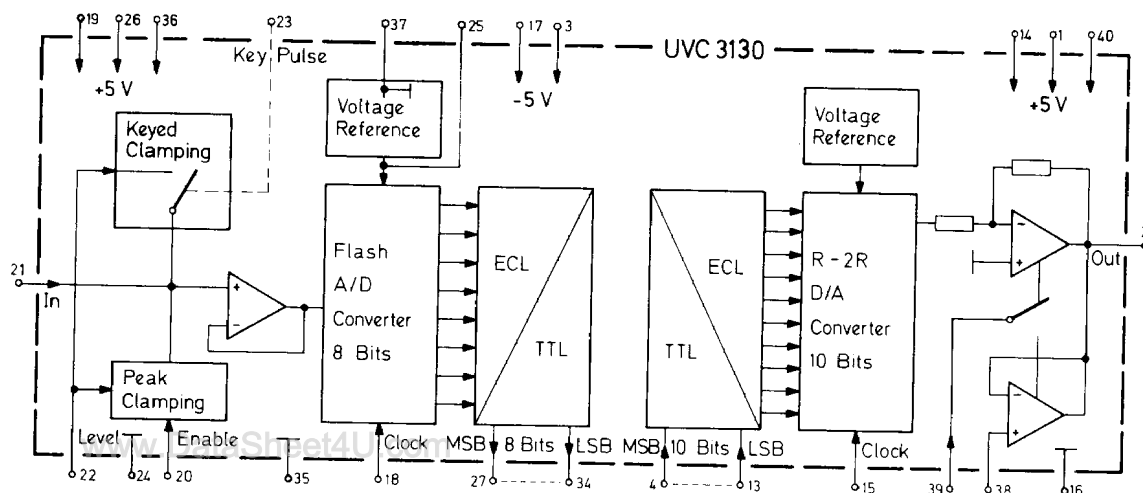
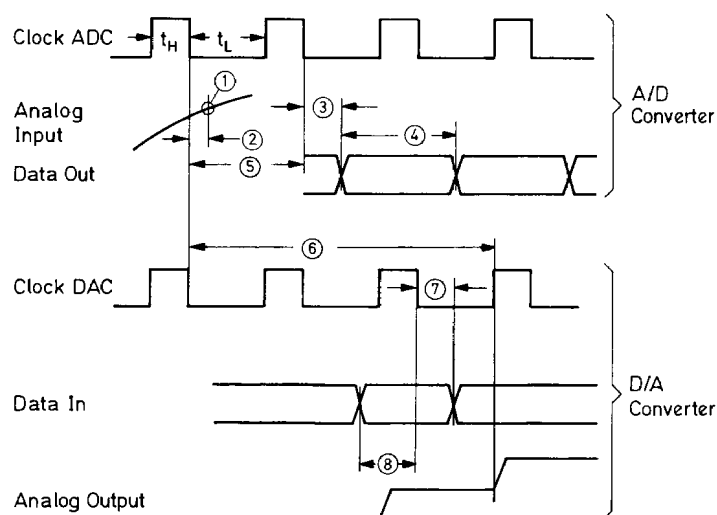


Fig. 1: UVC 3130 block diagram

Pin Connections

1	+5 V Supply D/A Converter Output Amplifier (Buffer)	21	Analog Input A/D Converter
2	Analog Output D/A Converter	22	Clamping Level Input
3	-5 V Supply D/A Converter analog	23	Key Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5 V Supply A/D Converter digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5 V Supply D/A Converter digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter	35	Digital Ground A/D Converter
16	GND D/A Converter and Clock A/D Converter	36	+5 V Supply A/D Converter analog
17	-5 V Supply A/D Converter analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter	38	External Analog Input
19	+5 V Supply Analog Input Amplifier and Voltage Reference A/D	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	+5 V Supply D/A Converter Output Amplifier (Final stage)

**Fig 3:** Timing diagram of the UVC 3130 A/D-D/A Converter

- ① Sample
- ② Aperture delay
- ③ Digital output delay
- ④ Data valid (after sample ①)
- ⑤ Transfer time A/D
- ⑥ Total transfer time A/D-D/A with common clock
- ⑦ Input register hold time
- ⑧ Input register setup time

3. Electrical Characteristics

All voltages are referred to pins 16, 24, 35 and 37.

Absolute Maximum Ratings

	Symbol	Value	Unit
Positive Supply Voltage	$+V_B$	6	V
Negative Supply Voltage	$-V_B$	6	V
Input Voltages			
Digital Inputs	V_I	$-0.5\text{ V to }(+V_B + 0.5\text{ V})$	–
Analog Input	V_I	$-1.5\text{ V to }(+V_B + 0.5\text{ V})$	–
Output Current Pin 2	I_O	± 10	mA
Ambient Operating Temperature Range	T_A	0 to +65	°C
Storage Temperature Range	T_S	–40 to +125	°C

Recommended Operating Conditions

	Symbol	Min.	Typ.	Max.	Unit
Positive Supply Voltage	+ V _B	4.75	5	5.25	V
Negative Supply Voltage	− V _B	4.75	5	5.25	V
A/D Converter					
Analog Input Voltage	V _I	0	−	2	V
Input Frequency, Analog Input	f _I	−	−	$< \frac{f_{cl}}{2}$	−
Clock Amplitude	V _{18H}	2.4 V	−	+ V _B	−
	V _{18L}	0	−	0.8	V
Clock Frequency	f ₁₈	0	−	30	MHz
Clock High Time (see Fig. 3)	t _H	10	−	−	ns
Clock Low Time (see Fig. 3)	t _L	23	−	−	ns
Clamping Level	V ₂₂	− 1	−	+ 2	V
Key Pulse	V _{23H}	2.4 V	−	+ V _B	−
	V _{23L}	0	−	0.8	V
Activation of Peak Clamping	Resistor of 20 to 60 kΩ from Pin 20 to + 5 V				
D/A Converter					
Clock Amplitude	V _{15H}	2.4 V	−	+ V _B	−
	V _{15L}	0	−	0.8	V
Clock Frequency	f ₁₅	0	−	30	MHz
Digital Input Voltages	V _{IH}	2.4 V	−	+ V _B	−
	V _{IL}	0	−	0.8	V
Analog Input Voltage at pin 38	V ₃₈	− 1	−	+ 3	V
Control Voltage for the Output Gate Amplifier					
Input Signal from Pin 21 at the Output Pin 2	V ₃₉	0	−	0.8	V
Input Signal from Pin 38 at the Output Pin 2	V ₃₉	2 V	−	+ V _B	−

Characteristics at $+V_B = 5\text{ V}$, $-V_B = 5\text{ V}$, $f_{15} = 25\text{ MHz}$, $f_{18} = 25\text{ MHz}$, $T_A = 25\text{ }^\circ\text{C}$

	Symbol	Min.	Typ.	Max.	Unit
Current Consumption	I_B	—	—	150	mA
	$-I_B$	—	—	150	mA
Power Dissipation	P_{tot}	—	—	1.5	W
Total Transfer Time A/D-D/A (⑥ in Fig. 3)	t_{tot}	—	see Fig. 3	—	—
A/D Converter					
Input Current Pin 21	I_I	—	1	—	μA
Input Impedance Pin 21 at $f = 1\text{ kHz}$	Z_I	—	20	—	$\text{M}\Omega$
at $f = 10\text{ MHz}$	Z_I	—	100	—	$\text{k}\Omega$
Input Capacitance Pin 21	C_I	—	10	—	pF
3 dB Bandwidth of the Input Amplifier	—	—	30	—	MHz
Clamping Active at	V_{23}	2.4	—	—	V
ON Resistance of the Clamping Switch Between Pins 21 and 22	R_{on}	—	300	—	Ω
Input Current of the Clamping Level Input 22	I_{22}	—	200	—	μA
Aperture Delay (② in Fig. 3)	t_{sd}	—	—	10	ns
Digital Output Delay (③ in Fig. 3)	t_{dv}	—	18	—	ns
Transfer Time (⑤ in Fig. 3)	t_{tr}	—	one Clock Period	—	—
Differential Non-Linearity	—	—	$\pm 1/2\text{ LSB}$	—	—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	8	—	—
Code of the Digital Output Signals	—	—	binary	—	—
Output Signal at $V_{21} = 0\text{ V}$	—	—	0 0 0 0 0 0 0 0	—	—
at $V_{21} = V_{\text{ref}}$	—	—	1 1 1 1 1 1 1 1	—	—
Internal Reference Voltage, accessible from outside	V_{25}	—	2.0	—	V
D/A Converter					
Input Register Hold Time (⑦ in Fig. 3)	t_{ih}	7.5	—	—	ns
Input Register Setup Time (⑧ in Fig. 3)	t_{is}	10	—	—	ns
Differential Non-Linearity (referred to 8 bit)	—	—	$\pm 1/2\text{ LSB}$	—	—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	10	—	—
Code of the Digital Input Signal	—	—	binary	—	—
Output Signal with 0 0 0 0 0 0 0 0 0 0 at the Inputs	V_2	—	0	—	V
with 1 1 1 1 1 1 1 1 1 1 at the Inputs	V_2	—	2	—	V
Output Impedance Pin 2	Z_O	—	15	—	Ω
Input Current Pin 38	I_I	—	1	—	μA
Internal Reference Voltage	V_{ref}	—	2	—	V

4. Pin Circuits

The following figures schematically show the circuitry at the various pins. × = protection diode

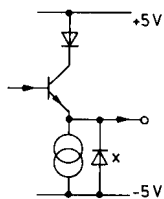


Fig. 4:
Pin 2, Output

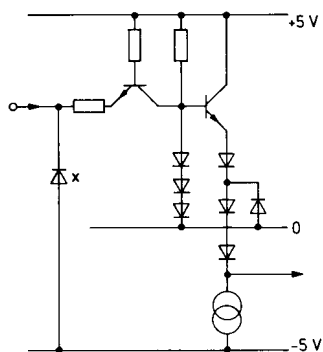


Fig. 5:
Pins 4 to 13 and 15, Inputs

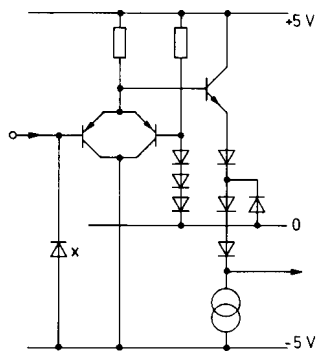


Fig. 6:
Pins 18, 23 and 39, Inputs

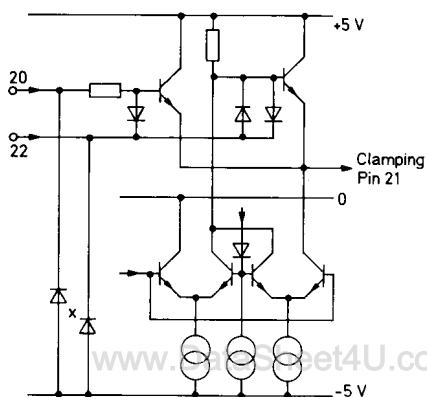


Fig. 7:
Pins 20 and 22, Inputs

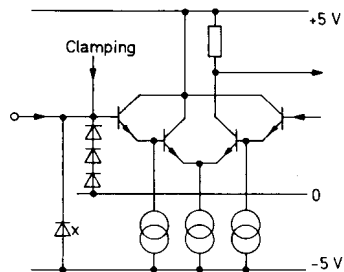


Fig. 8:
Pin 21, Input

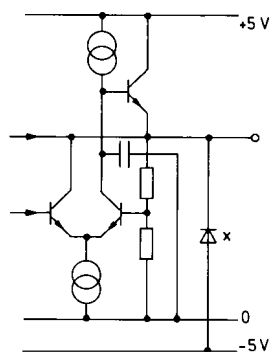


Fig. 9:
Pin 25, Reference Voltage Pin

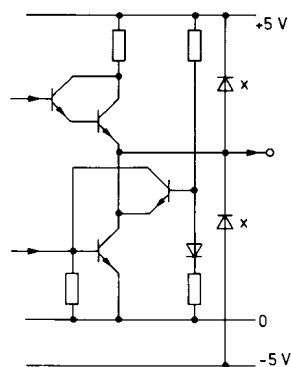


Fig. 10:
Pins 27 to 34, Outputs

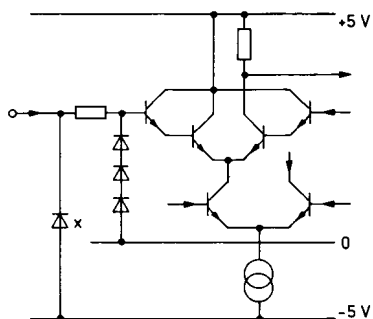


Fig. 11:
Pin 38, Input

5. Pin Descriptions

Pin 1 – +5 V Supply D/A Converter Output Amplifier

By this pin, the buffer stage of the D/A converter's analog output amplifier is powered.

Pin 2 – Analog Output D/A Converter

This pin whose diagram is shown in Fig. 4, is the output for the processed analog signal either originating from the D/A converter or from the external analog input pin 38.

Pin 3 – –5 V Supply D/A Converter Analog

This pin gets the negative supply for the analog part of the D/A converter.

Pins 4 to 13 – Digital Inputs Bit 9 to Bit 0

The diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter. Not-used inputs should be connected to ground.

Pin 14 – +5 V Supply D/A Converter Digital

This pin gets the positive supply for the digital part of the D/A converter.

Pin 15 – Clock Input D/A Converter

This pin whose diagram is shown in Fig. 5 must be supplied with the clock signal for the D/A converter.

Pin 16 – GND D/A Converter and Clock A/D Converter

This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.

Pin 17 – –5 V Supply A/D Converter Analog

This pin is the negative supply pin for the analog part of the A/D converter.

Pin 18 – Clock Input A/D Converter

The diagram of this pin is shown in Fig. 6. Pin 18 is supplied with the clock of the A/D converter.

Pin 19 – +5 V Supply Analog Input Amplifier and Voltage Reference A/D

Via this pin the analog input amplifier and the voltage reference of the A/D converter are powered.

Pin 20 – Peak Clamping Enable Input

Via pin 20 whose diagram is shown in Fig. 7, the peak clamping facility can be enabled.

Pin 21 – Analog Input A/D Converter

Fig. 8 is the diagram of this input. To pin 21 the analog signal to be converted into digital is applied.

Pin 22 – Clamping Level Input

Via this pin whose diagram is shown in Fig. 7, the input of the A/D converter is supplied with the desired clamping level.

Pin 23 – Key Pulse Input

Fig. 6 is the diagram of this input. Pin 23 must be supplied with the key pulse if keyed clamping is required.

Pin 24 – Analog Ground A/D Converter

This pin serves as ground pin for the analog part of the A/D converter. It must be connected with pin 37 as short as possible.

Pin 25 – Reference Voltage A/D Converter

This pin whose diagram is shown in Fig. 9, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to pin 37.

Pin 26 – +5 V Supply A/D Converter Digital

This pin is the positive supply pin for the digital part of the A/D converter.

Pins 27 to 34 – Digital Outputs Bit 7 to Bit 0

Fig. 10 shows the diagram of these outputs which supply the digitalized analog signal in parallel 8-bit code.

Pin 35 – Digital Ground A/D Converter

This pin is the ground connection for the digital part of the A/D converter.

Pin 36 – +5 V Supply A/D Converter Analog

This pin is the positive supply pin for the analog part of the A/D converter.

Pin 37 – Ground of Reference Voltage A/D Converter

To this pin must be connected the ground end of the decoupling capacitor which is at pin 25.

Pin 38 – External Analog Input

The diagram of this input is shown in Fig. 11. Pin 38 serves for feeding an external analog signal into the output amplifier of the UVC 3130 instead of the D/A-converted signal originating from pins 4 to 13.

Pin 39 – Output Signal Switchover Input

This pin whose diagram is shown in Fig. 6, is intended for enabling the external analog signal fed to pin 38.

Pin 40 – +5 V Supply D/A Converter Output Amplifier

By this pin, the final (power) stage of the D/A converter's analog output amplifier is powered.

6. Appendix: Application Circuits

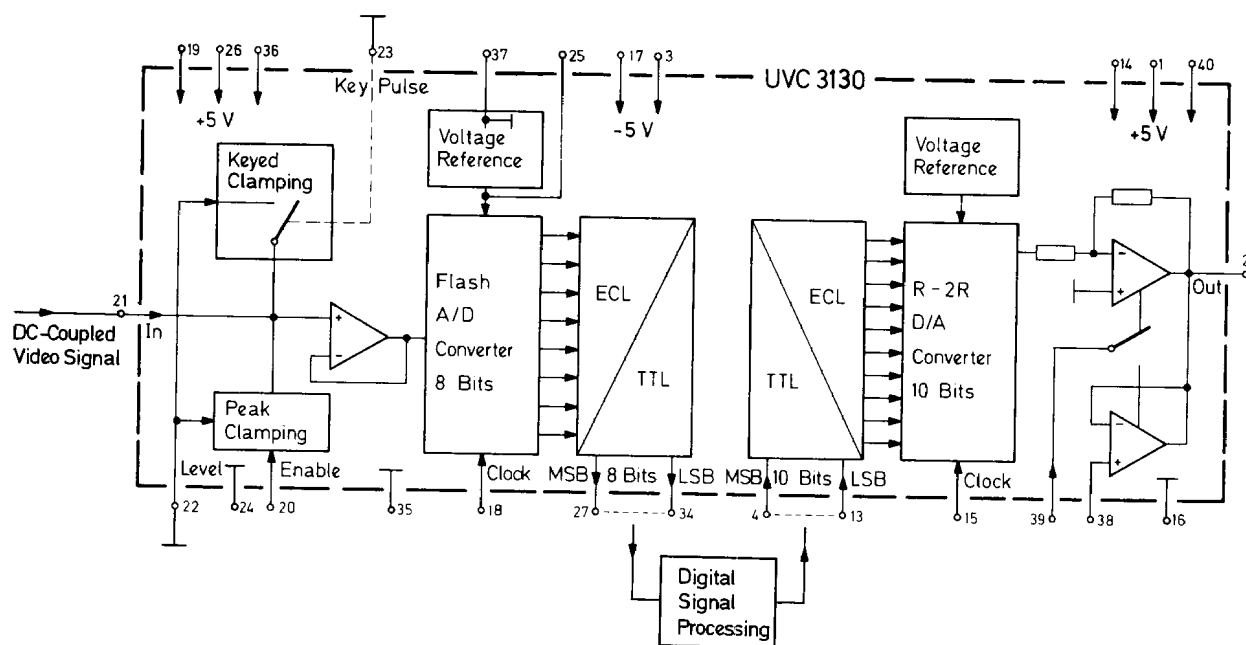


Fig. 11: Operation without clamping of the input signal
Pin 20 must not be connected.

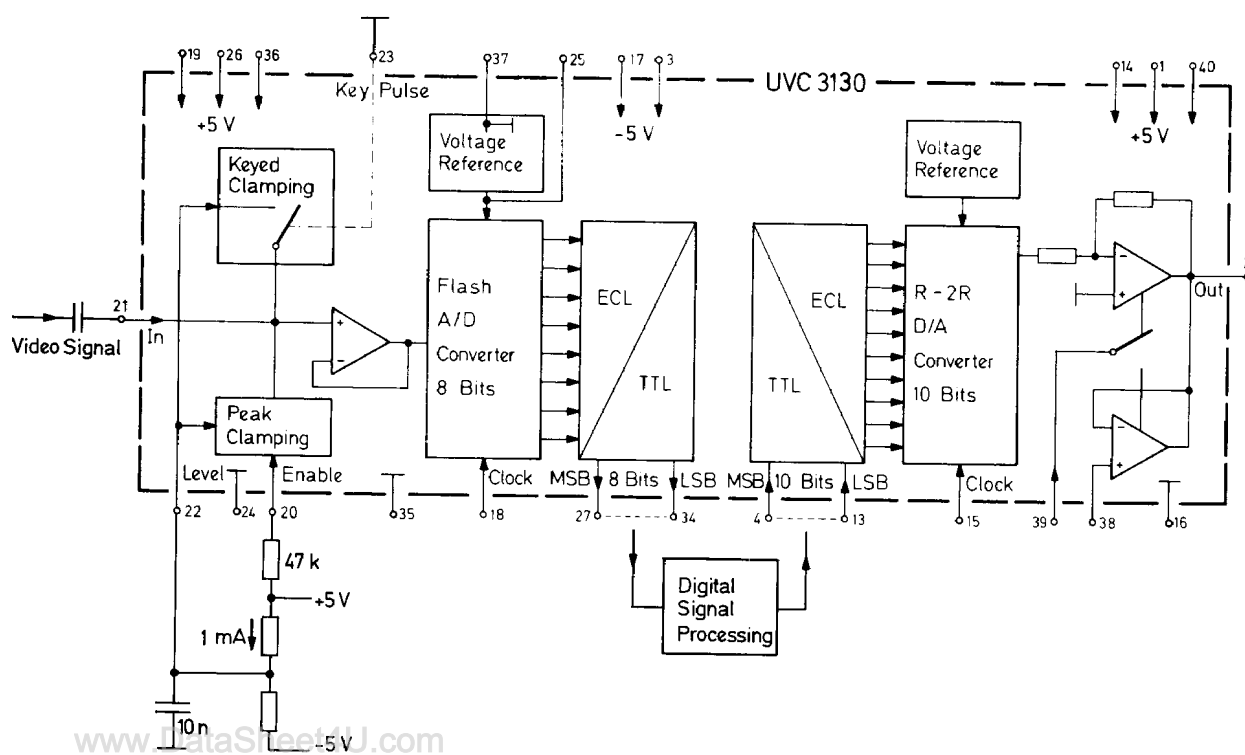


Fig. 12: Operation with peak clamping
The input signal is clamped automatically to the negative peak value. No key pulse is needed.

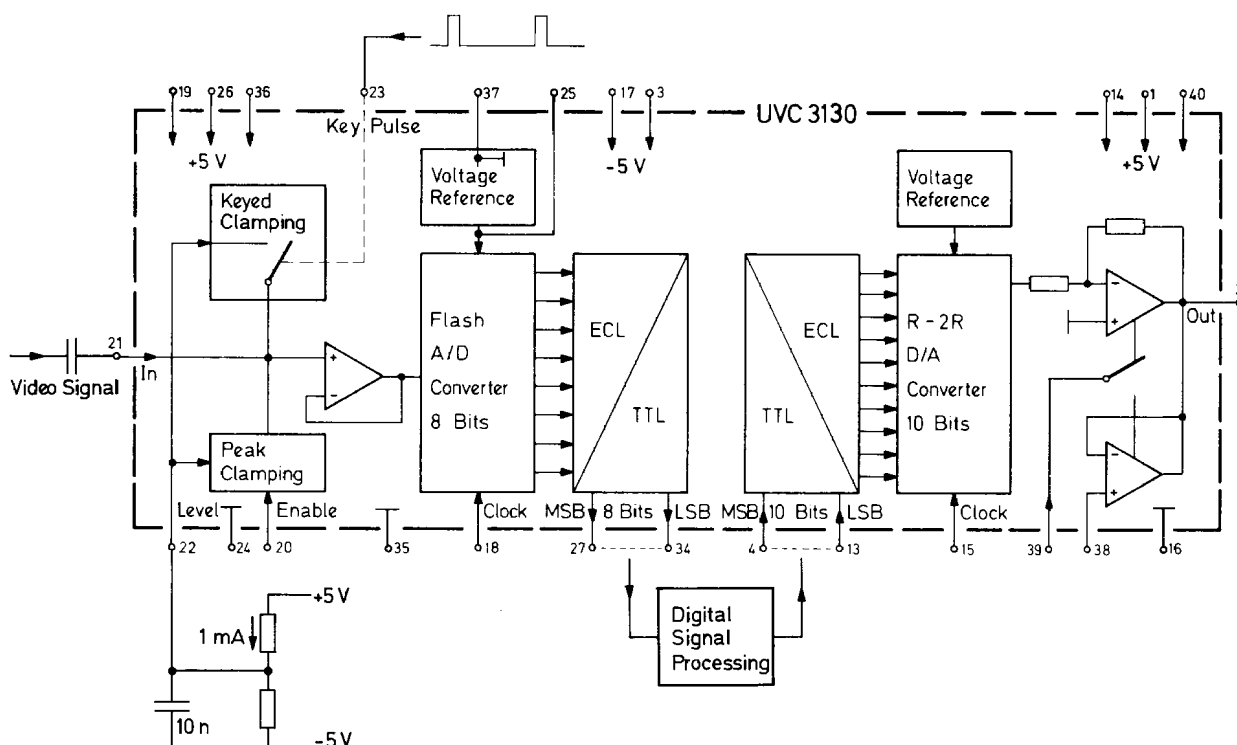


Fig. 13: Operation with keyed clamping

During the key pulse, the input signal must have that level to which it is to be clamped. Pin 20 must not be connected.

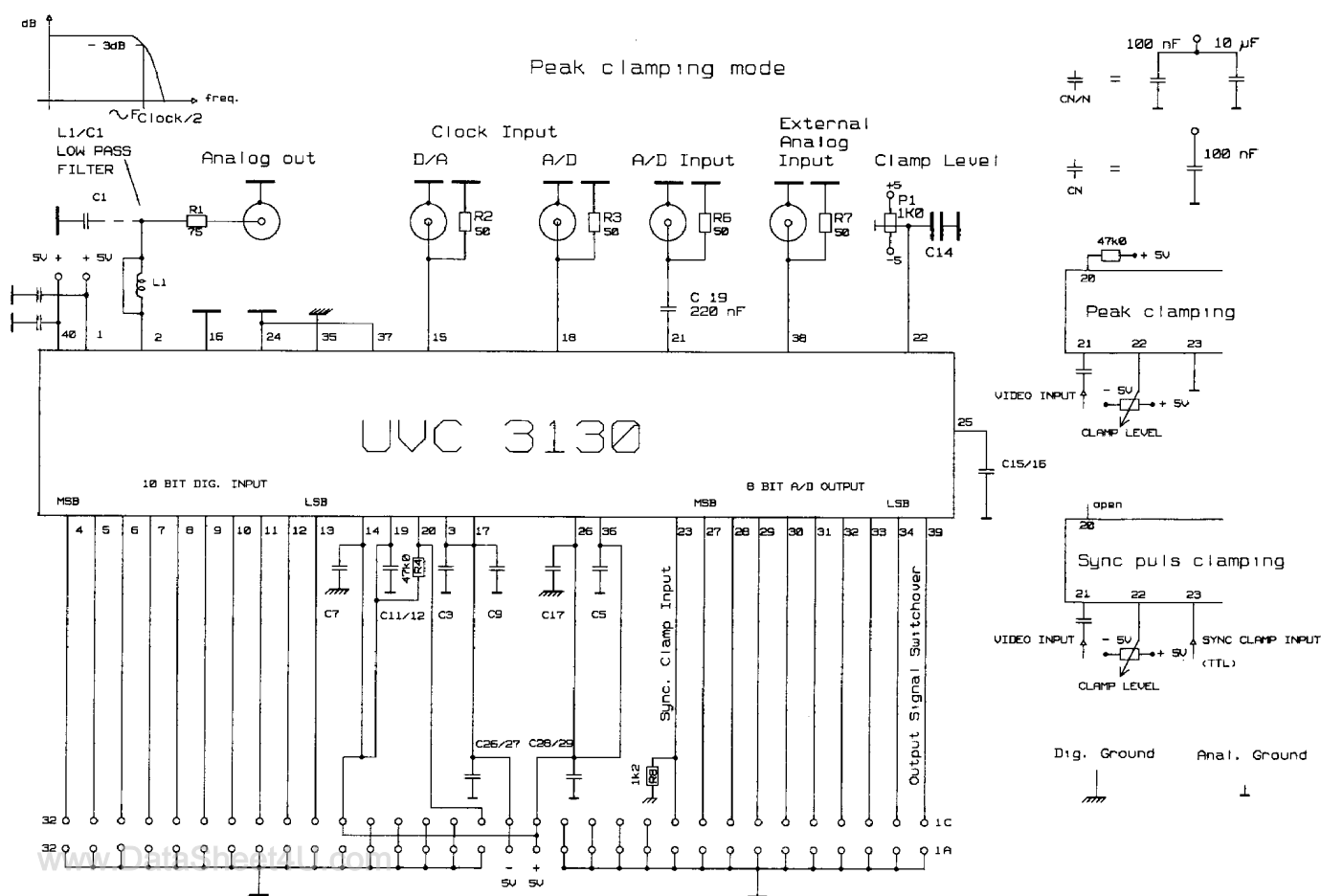


Fig. 14: Application diagram including power supply and associated decoupling elements.

**Production and
Marketing Centers:**

U.S.A.

ITT Semiconductors
55 Merrimack Street
Lawrence, MA 01843
Tel. (617) 688-1881
TWX 710-342-1357

W. Germany

INTERMETALL GmbH
P.O. Box 840
D-7800 Freiburg
Tel. (0761) 517-0
Telex 772 715

Japan

ITT Semiconductors FEL
P.O. Box 21
Shinjuku-ku
Tokyo 160-91
Tel. (03) 347 88 81-5
Telex 22 858

Reprinting is generally permitted, indicating the source. However, our consent must be obtained in all cases. Information furnished by ITT is believed to be accurate and reliable. However, no responsibility is assumed by ITT for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of ITT. The information and suggestions are given without obligation and cannot give rise to any liability; they do not indicate the availability of the components mentioned. Delivery of development samples does not imply any obligation of ITT to supply larger amounts of such units to a fixed term. To this effect, only written confirmation of orders will be binding.

www.DataSheet4U.com

Printed in W. Germany · Imprimé dans la République Fédérale d'Allemagne by Rombach GmbH Druck- und Verlagschaus, Freiburg i. Br.

Edition 1988/3 · Order No. 6251-306-1E