



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Sep.5.2006
Rev. 1.1	Revised Package Outline Dimension(TSOP-II)	Apr.12.2007
Rev. 2.0	Revised I _{CC} and I _{SB1} Revised Test Condition of I _{SB1} /I _{DR} Added E and I grade	Jun.23.2007
Rev. 2.1	Revised <u>ABSOLUTE MAXIMUM RATINGS</u> Adding PKG type : 36-ball 6mm x 8mm TFBGA Revised Test Condition of I _{CC}	Mar.31.2008
Rev. 2.2	Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available to Green package available</u> Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u>	Apr.17.2009



FEATURES

- Fast access time : 10/12/15/20/25ns
- **Very low power consumption:**
 Operating current(Normal version):
 180/160/140/80/70mA(MAX.)
 Standby current:
 12mA(MAX. for 10/12/15ns)
 5mA(MAX. for 20/25ns)
100µA(MAX. for 20/25ns LL version)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 32-pin 8mm x 20mm TSOP-I
 32-pin 8mm x 13.4mm STSOP
 44-pin 400 mil TSOP-II
 36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The LY61L5128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

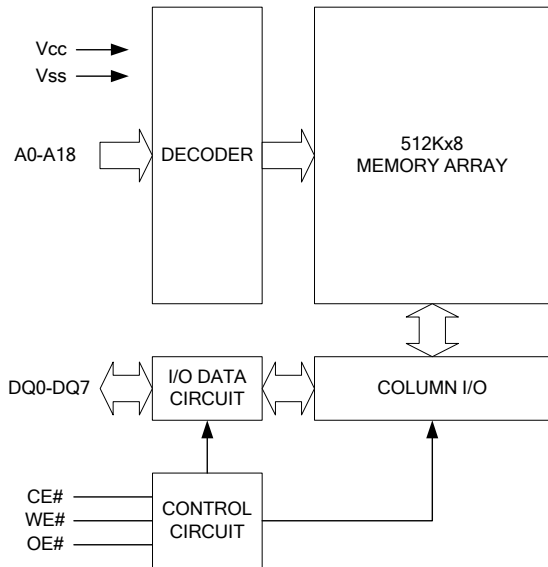
The LY61L5128 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY61L5128 operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,MAX.)	Operating(I _{CC} ,MAX.)
LY61L5128	0 ~ 70°C	3.15/3.0 ~ 3.6V	10/12/15ns	12mA	180/160/140mA
LY61L5128(E)	-20 ~ 80°C	3.15/3.0 ~ 3.6V	10/12/15ns	12mA	180/160/140mA
LY61L5128(I)	-40 ~ 85°C	3.15/3.0 ~ 3.6V	10/12/15ns	12mA	180/160/140mA
LY61L5128	0 ~ 70°C	3.0 ~ 3.6V	20/25ns	5mA	80/70mA
LY61L5128(E)	-20 ~ 80°C	3.0 ~ 3.6V	20/25ns	5mA	80/70mA
LY61L5128(I)	-40 ~ 85°C	3.0 ~ 3.6V	20/25ns	5mA	80/70mA
LY61L5128(LL)	0 ~ 70°C	3.0 ~ 3.6V	20/25ns	100µA	80/70mA
LY61L5128(LLE)	-20 ~ 80°C	3.0 ~ 3.6V	20/25ns	100µA	80/70mA
LY61L5128(LLI)	-40 ~ 85°C	3.0 ~ 3.6V	20/25ns	100µA	80/70mA

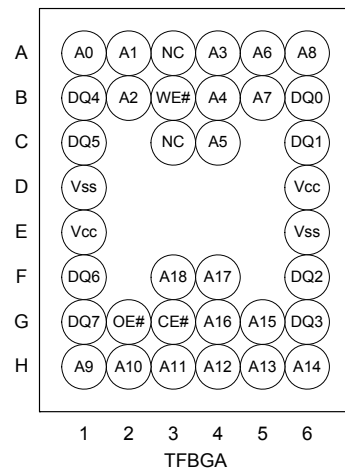
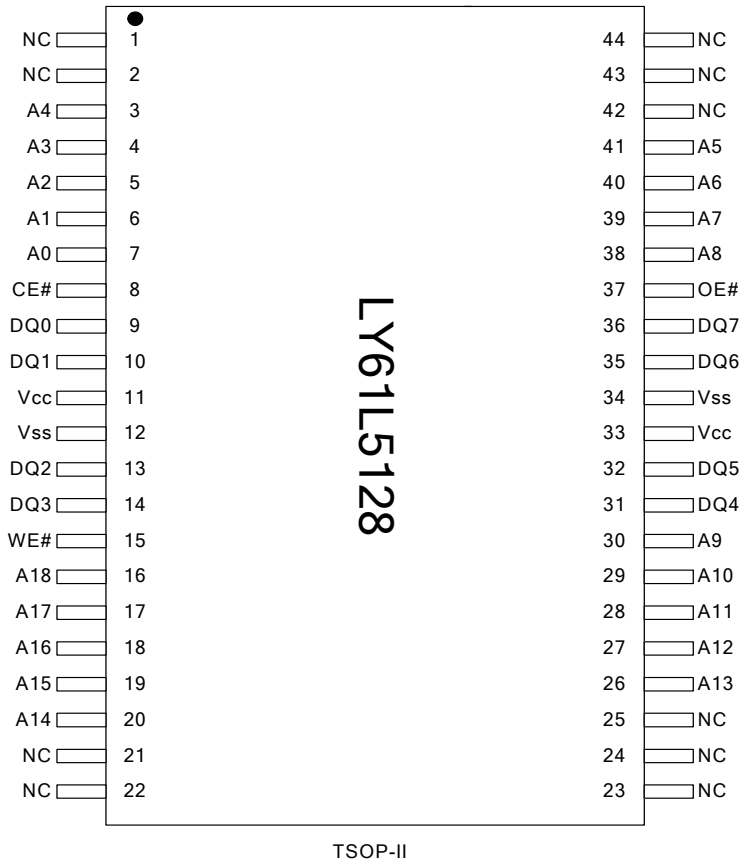
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to V _{cc} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	High-Z	I _{cc}
Read	L	L	H	D _{OUT}	I _{cc}
Write	L	X	L	D _{IN}	I _{cc}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		10/12	3.15	3.3	3.6	V
			15/20/25	3.0	3.3	3.6	V
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		-0.3	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA others at V _{IH} or V _{IL}	10	-	-	180	mA
			12	-	-	160	mA
			15	-	-	140	mA
			20	-	50	80	mA
			25	-	45	70	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V, others at 0.2V or V _{CC} - 0.2V	10/12/15	-	-	12	mA
			20/25	-	0.5	5 ⁵	mA
			20/25LL	-	20	100 ⁶	μA

Notes:

1. $V_{IH(max)} = V_{CC} + 3.0V$ for pulse width less than 10ns.
2. $V_{IL(min)} = V_{SS} - 3.0V$ for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at $V_{CC} = V_{CC(TYP.)}$ and $T_A = 25^\circ C$
5. 1mA for special request
6. 50 μ A for special request

CAPACITANCE ($T_A = 25^\circ C, f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	C_{IO}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -8mA/16mA$

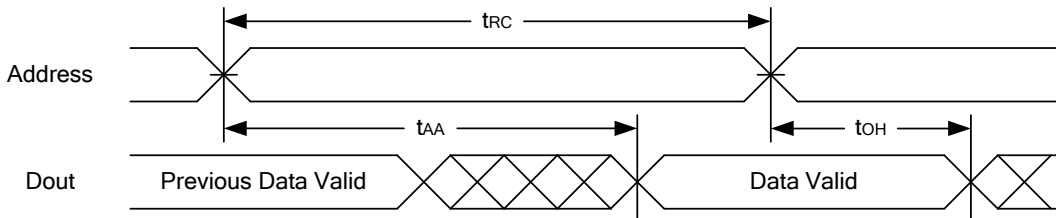
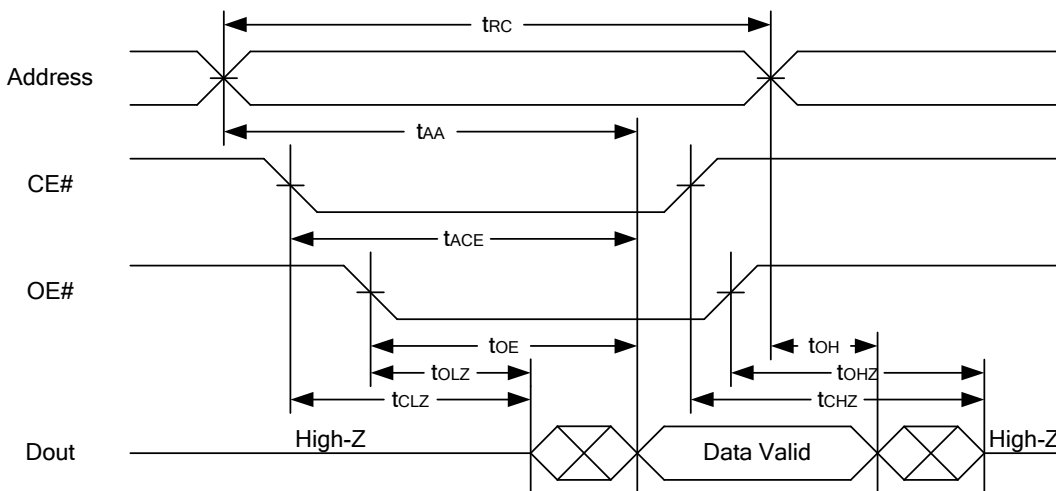
AC ELECTRICAL CHARACTERISTICS
(1) READ CYCLE

PARAMETER	SYM.	LY61L5128 -10		LY61L5128 -12		LY61L5128 -15		LY61L5128 -20		LY61L5128 -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	20	-	25	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	-	20	-	25	ns
Chip Enable Access Time	t_{ACE}	-	10	-	12	-	15	-	20	-	25	ns
Output Enable Access Time	t_{OE}	-	5	-	6	-	7	-	8	-	9	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	2	-	3	-	4	-	4	-	4	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	5	-	6	-	7	-	8	-	9	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	5	-	6	-	7	-	8	-	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	3	-	ns

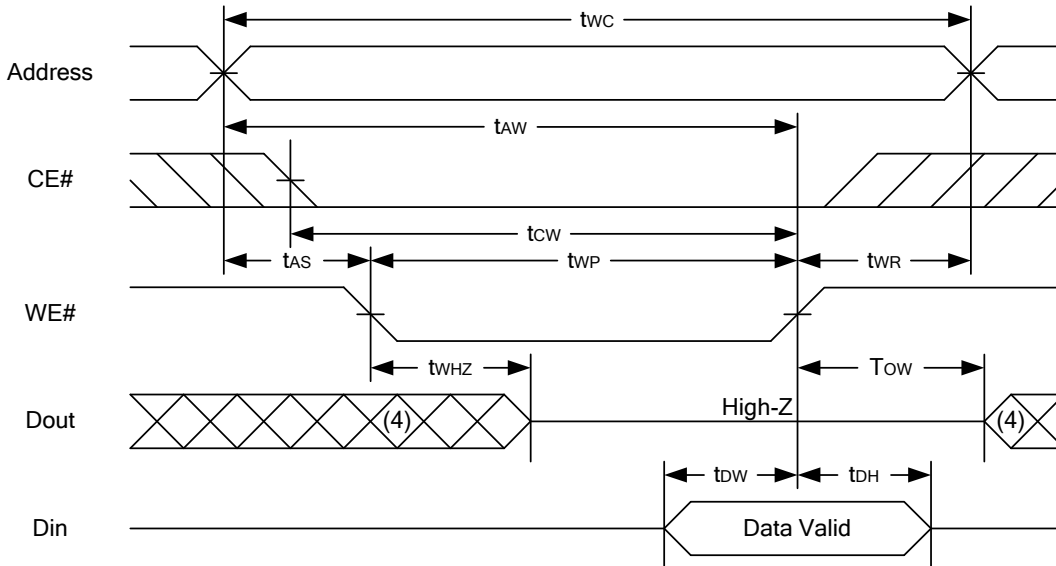
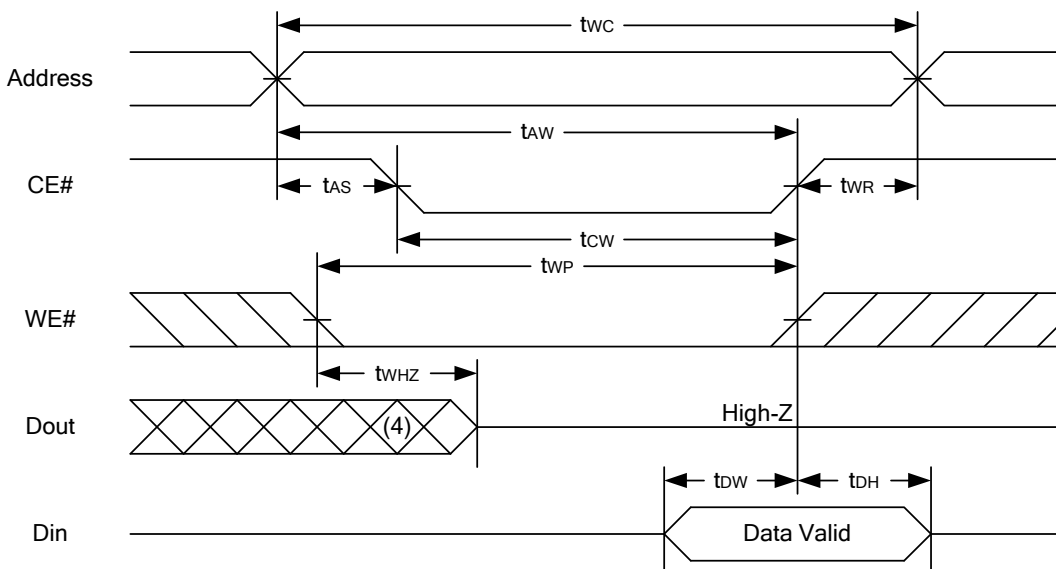
(2) WRITE CYCLE

PARAMETER	SYM.	LY61L5128 -10		LY61L5128 -12		LY61L5128 -15		LY61L5128 -20		LY61L5128 -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	20	-	25	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	16	-	20	-	ns
Chip Enable to End of Write	t_{CW}	8	-	10	-	12	-	16	-	20	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	9	-	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	9	-	10	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	3	-	4	-	5	-	6	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	6	-	7	-	8	-	9	-	10	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS
READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

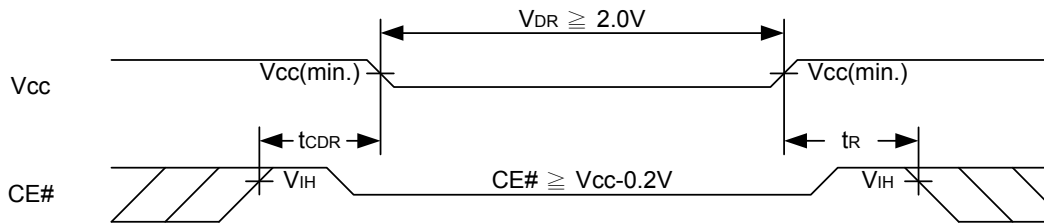
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)

Notes :

1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, twp must be greater than twhz + tdw to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tow and twhz are specified with CL = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
VCC for Data Retention	V_{DR}	$CE\# \geq V_{CC} - 0.2V$	2.0	-	3.6	V	
Data Retention Current	I_{DR}	$V_{CC} = 2.0V$	10/12/15	-	-	mA	
		$CE\# \geq V_{CC} - 0.2V$	20/25	-	0.5	1	mA
		others at 0.2V or $V_{CC} - 0.2V$	20/25LL	-	10	50	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t_R		t_{RC*}	-	-	ns	

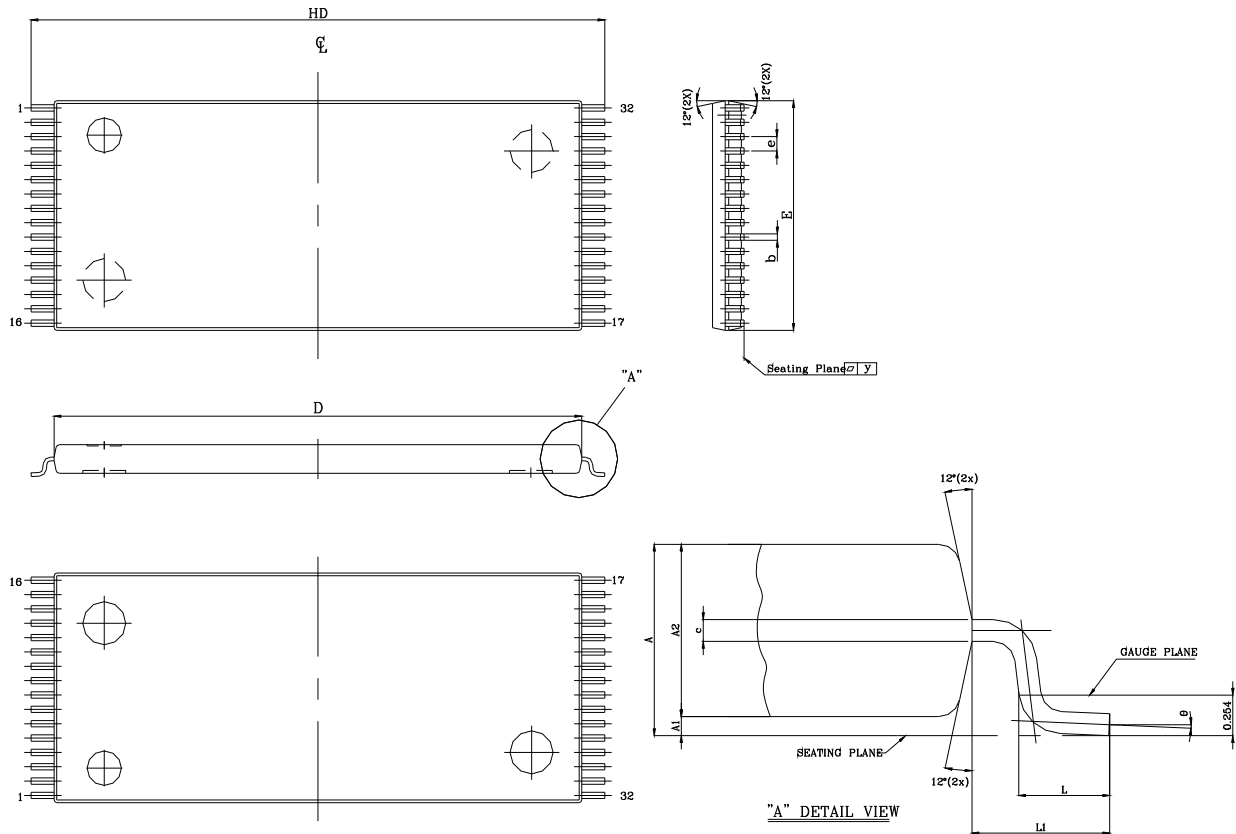
 t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM


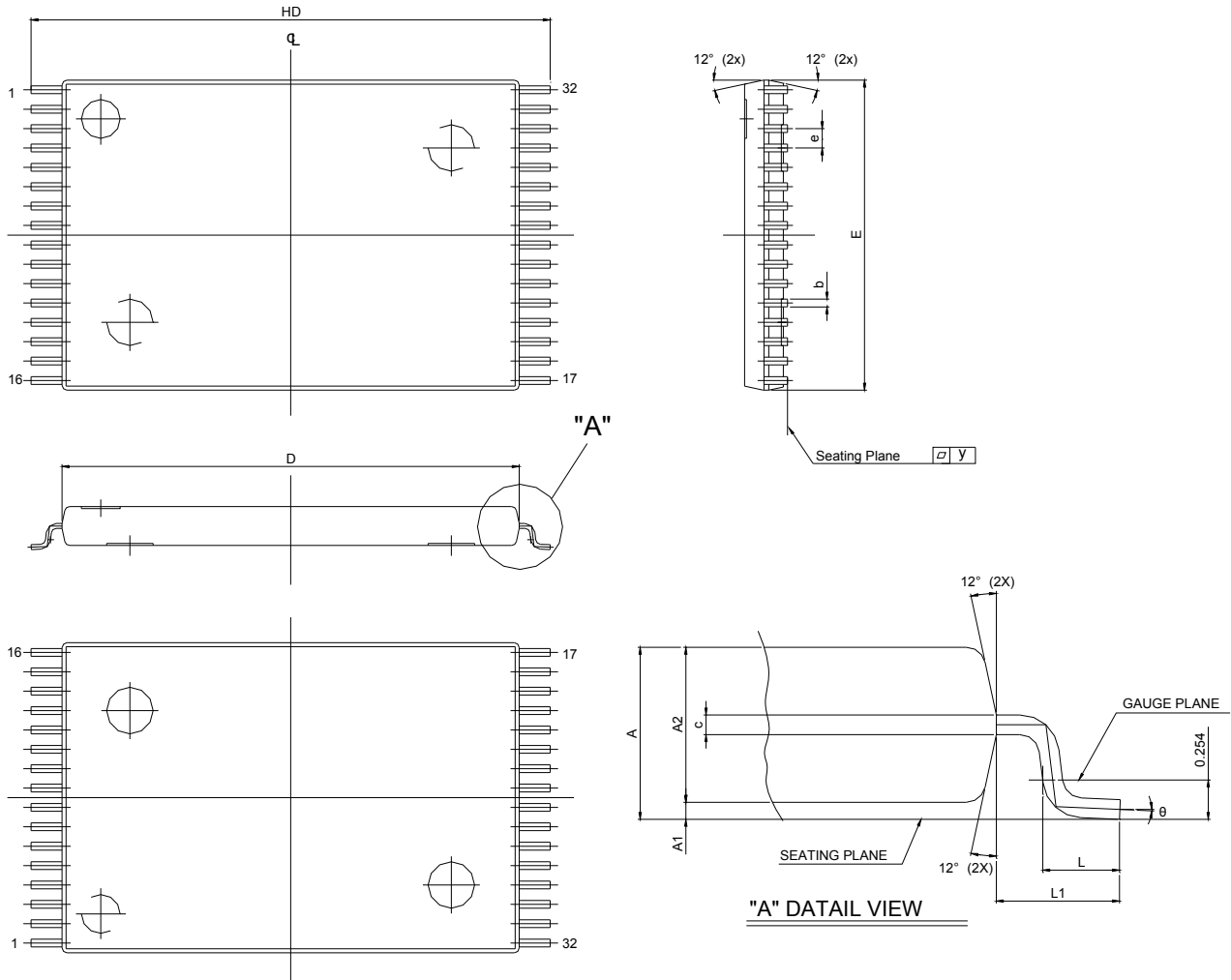


PACKAGE OUTLINE DIMENSION

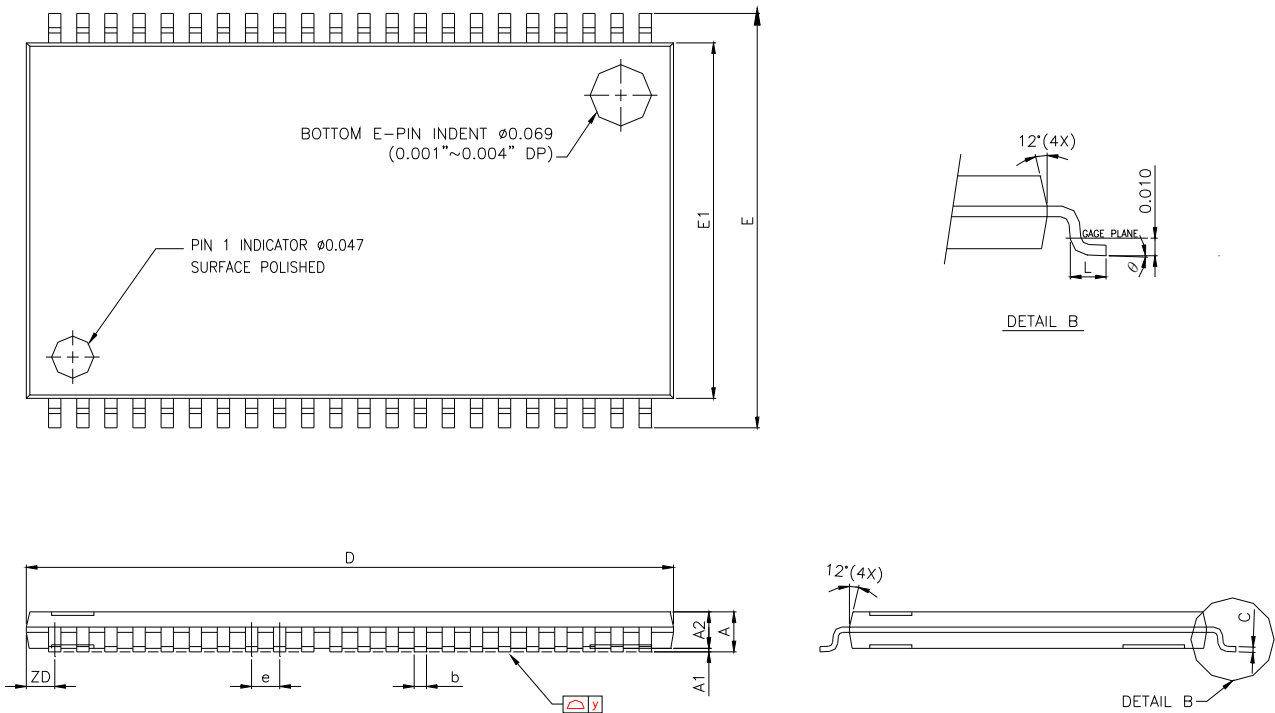
32 pin 8mm x 20mm TSOP-I Package Outline Dimension



SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 \pm 0.002	0.10 \pm 0.05
A2		0.039 \pm 0.002	1.00 \pm 0.05
b		0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c		0.005 (TYP)	0.127 (TYP)
D		0.724 \pm 0.004	18.40 \pm 0.10
E		0.315 \pm 0.004	8.00 \pm 0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 \pm 0.008	20.00 \pm 0.20
L		0.0197 \pm 0.004	0.50 \pm 0.10
L1		0.0315 \pm 0.004	0.08 \pm 0.10
y		0.003 (MAX)	0.076 (MAX)
\ominus		0 $^{\circ}$ ~ 5 $^{\circ}$	0 $^{\circ}$ ~ 5 $^{\circ}$

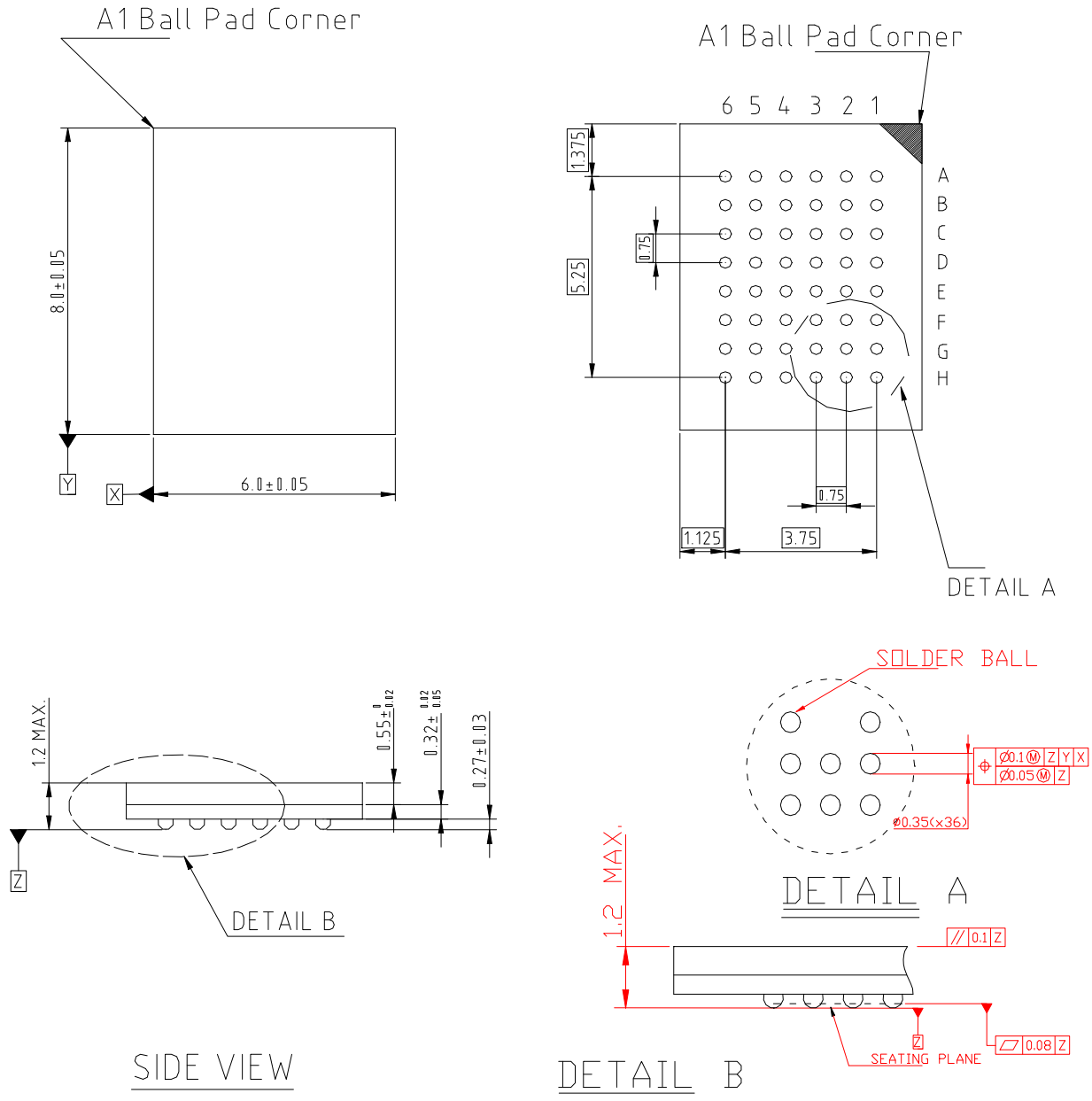
32 pin 8mm x 13.4mm STSOP Package Outline Dimension


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.005 ±0.002	0.130 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 ±0.01	0.20±0.025
c		0.005 (TYP)	0.127 (TYP)
D		0.465 ±0.004	11.80 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.8 ±0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°

44-pin 400mil TSOP- II Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

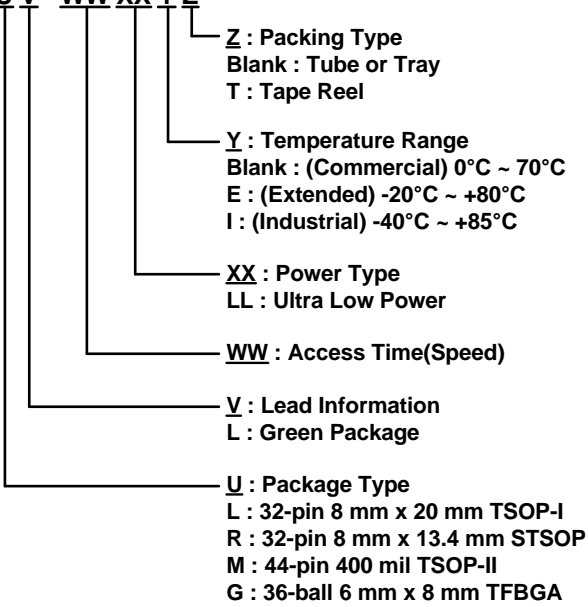
36 ball 6mm x 8mm TFBGA Package Outline Dimension





ORDERING INFORMATION

LY61L5128 U V - WW XX Y Z





®

Lyontek Inc.

LY61L5128

Rev. 2.2

512K X 8 BIT HIGH SPEED CMOS SRAM

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