January 1983

EUROTECHNIQUE

ET2147/ETL2147 Family
4096 × 1 Static Random Access Memories

General Description

The ET2147 is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology X-MOS. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out non-destructively and has the same polarity as the input data.

The separate ship select input automatically switches the part to its low power standby mode.

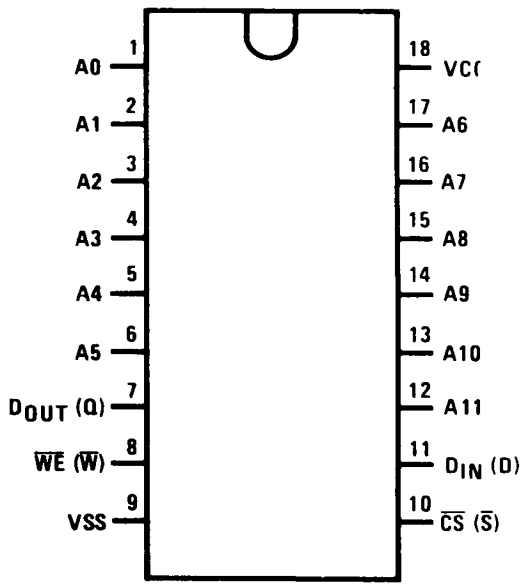
The output is held in a high impedance state during write to simplify common I/O applications

Features

- All inputs and outputs directly TTL compatible
- Static operation -no clocks or refreshing required
- Automatic power down
- High speed - down to 55 ns access time
- Three-state output for bus interface
- Separate Data In and Data Out pins
- Single + 5V supply
- Standard 18-pin dual-in-line package

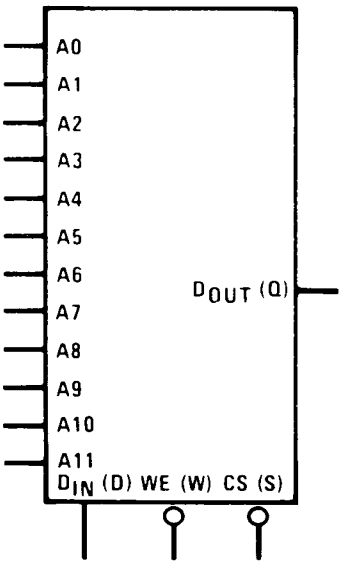
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



Pin Names*

A0–A11	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
DIN (D)	Data In
DOUT (Q)	Data Out
VCC	Power (+5V)
VSS	Ground

Truth Table*

CS (S)	WE (W)	DIN (D)	DOUT (Q)	MODE	POWER
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

*Symbols in parentheses are industry standard.

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Functional Description

Two pins control the operation of the **ET2147** . Chip select enables write and read operations, deselects the device putting it in the low power standby mode, and controls TRI-STATING of the data-output buffer. Write enable chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the controls.

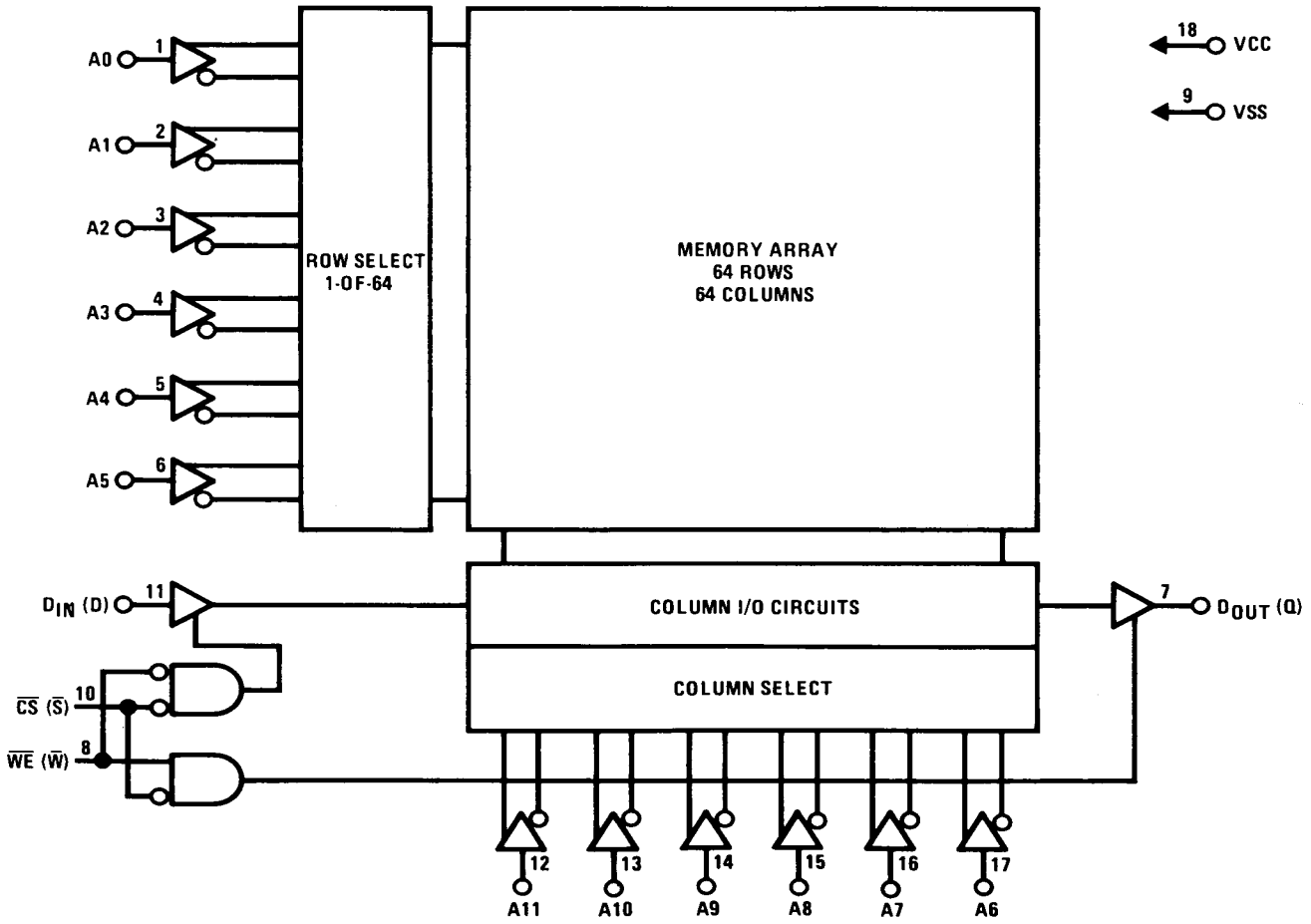
READ-cycle timing is shown in the section on Switching Time Waveforms. Write enable is kept high. Independent of chip select any change in address code causes new data to be fetched and brought to the output buffer. Chip select must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

Address access time is the time required for an address change to produce new data at the output pin, assuming chip select has enabled the output buffer prior to data arrival. Chip-select access time is the time required for chip select to enable the output buffer and transfer previously fetched data to the output pin. Operation with chip select continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both chip select and write enable are low. Minimum write pulse width refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with chip select continuously held low. Write enable then is used to terminate WRITE between address changes. Alternatively, write enable may be held low for successive WRITES and chip select used for write interruption between address change. In any event, either write enable or chip select (or both) must be high during address transitions to prevent erroneous WRITE.

Standby operation allows data to be maintained with approximately 85% less current. The device automatically switches to the low power standby mode whenever it is deselected.

Block Diagram*



*Symbols in parentheses are industry standard.

Absolute Maximum Ratings

Voltage on any Pin Relative to VSS	−1.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−10°C to +85°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+70	°C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

SYMBOL	PARAMETER	CONDITIONS	ET2147-3		ET2147		ETL2147		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
VIH	Logical "1" Input Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VIL	Logical "0" Input Voltage		−1.0	0.8	−1.0	0.8	−1.0	0.8	V
VOH	Logical "1" Output Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
VOL	Logical "0" Output Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
ILI	Input Load Current	VIN = 0 to 5.25V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	VO = 4.5V to Gnd, $\overline{CS}$ = VIH, VCC = Max		50		50		50	μA
ICC1	Power Supply Current	VCC = Max, $\overline{CS}$ = VIL, Outputs Open, TA = 25°C		170		150		135	mA
ICC2	Power Supply Current	VCC = Max, $\overline{CS}$ = VIL, Outputs Open, TA = 0°C		180		160		140	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		30		20		10	mA
IPO	Peak Power ON Current (Note 2)	VCC = Gnd to VCC Min, $\overline{CS}$ = Lower of VCC or VIH (MIN)		70		50		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
CIN	Input Capacitance	All Inputs VIN = 0V		5	pF
COUT	Output Capacitance	VO = 0V		6	pF

AC Test Conditions (Note 4)

Input Pulse Levels	Gnd to 3.5V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See *Figure 1*

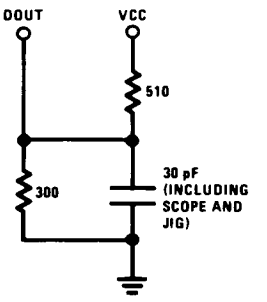


FIGURE 1. Output Load

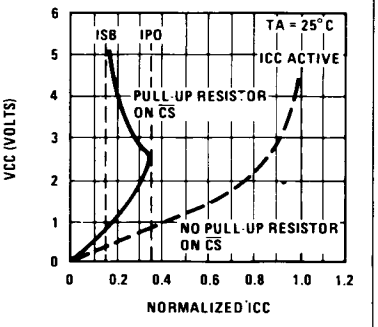


FIGURE 2. Power On Current

Note 1: Guaranteed with transverse air flow greater than 400 linear feet per minute.

Note 2: A pull-up resistor to VCC on the chip select input is required to keep the device deselected or power on current approaches ICC active (see *Figure 2*).

Note 3: This parameter is guaranteed by periodic testing.

Note 4: This device requires a 500 ns time delay after VCC reaches the specified minimum limit to ensure proper operation after power on. This allows the internally generated substrate bias to reach its functional level.

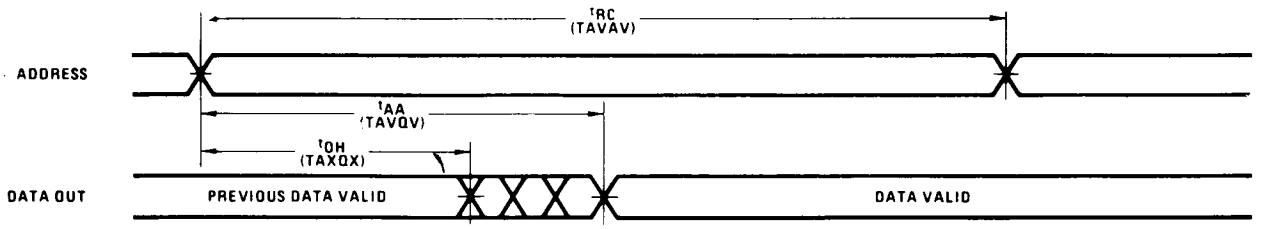
Read Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10%

SYMBOL		PARAMETER	ET2147-3		ET2147, ETL2147		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	
t_{RC}	TAVAV	Read Cycle Time	55		70		ns
t_{AA}	TAVQV	Address Access Time		55		70	ns
t_{ACS1}	TSLQV1	Chip Select Access Time (Note 5)		55		70	ns
t_{ACS2}	TSLQV2	Chip Select Access Time (Note 6)		65		80	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		ns
t_{LZ}	TSLQX	Chip Selection to Output Active	10		10		ns
t_{HZ}	TSHQZ	Chip Deselection to Output TRI-STATE	0	40	0	40	ns
t_{PU}	TSLICCH	Chip Selection to Power Up	0		0		ns
t_{PD}	TSLICCL	Chip Deselection to Power Down		30		30	ns

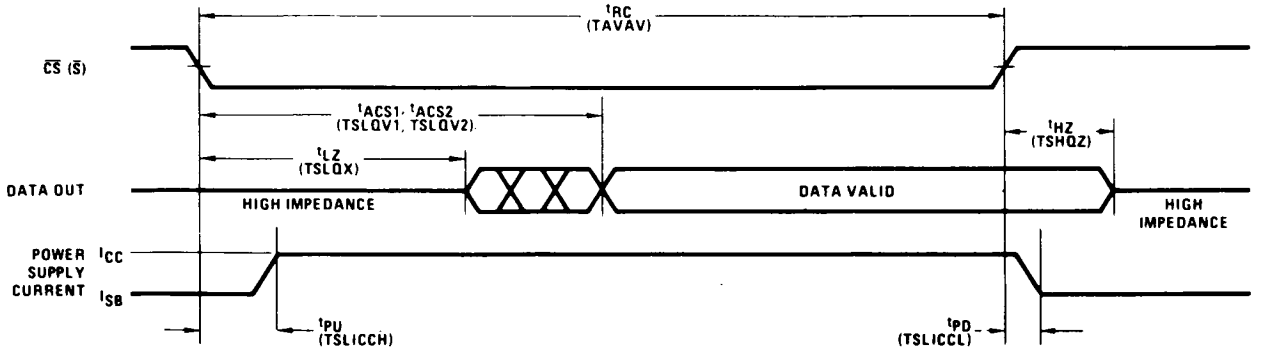
Note 5: Chip deselected for greater than 55 ns prior to selection.
Note 6: Chip deselected for a finite time that is less than 55 ns prior to selection.

Read Cycle Waveforms*

Read Cycle No. 1 (Continuously Selected)



Read Cycle No. 2 (Chip Select Switched)



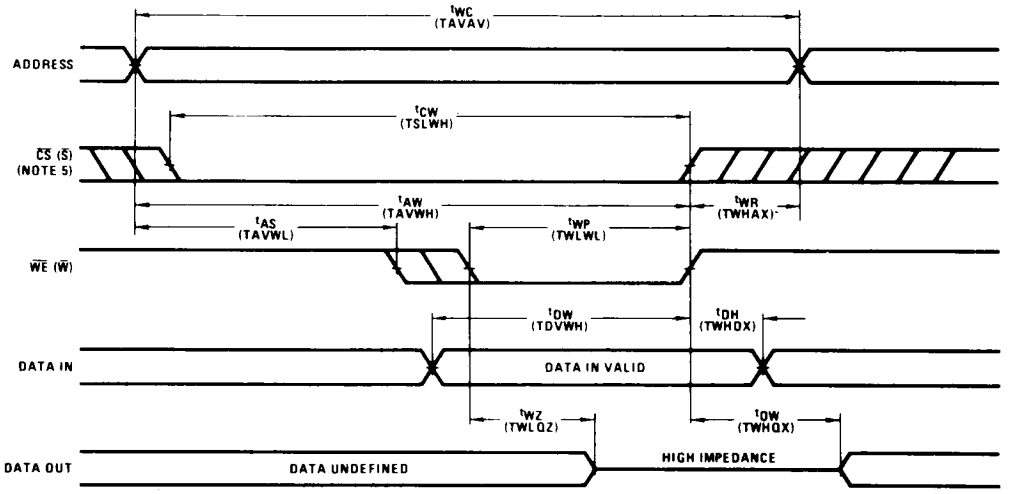
*Symbols in parentheses are industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10%

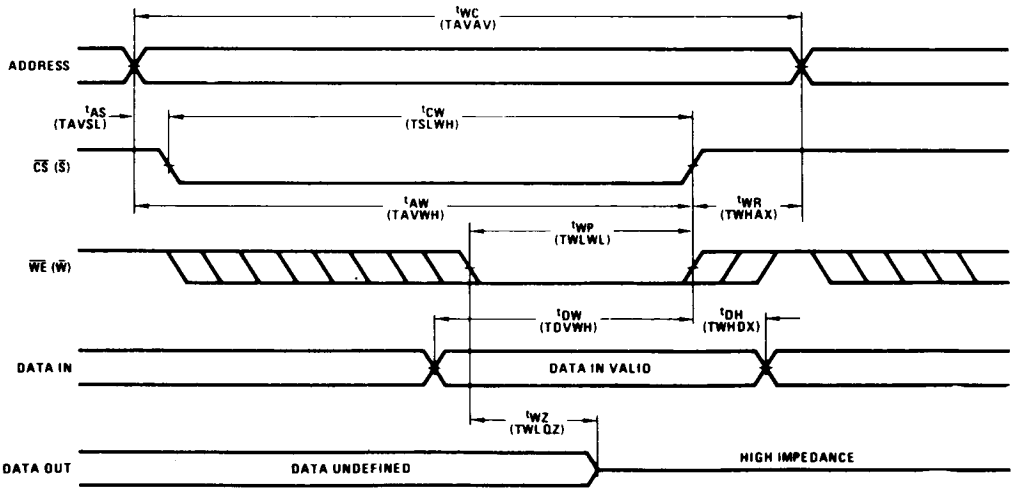
SYMBOL		PARAMETER	ET2147-3		ET2147, ETL2147		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	
t_{WC}	TAVAV	Write Cycle Time	55		70		ns
t_{CW}	TSLWH	Chip Selection to End of Write	45		55		ns
t_{AW}	TAVWH	Address Valid to End of Write	45		55		ns
t_{AS}	TAVWL TAVSL	Address Setup Time	0		0		ns
t_{WP}	TWLWL	Write Pulse Width	35		40		ns
t_{WR}	TWHAX	Write Recovery Time	10		15		ns
t_{DW}	TDVWH	Data Valid to End of Write	25		30		ns
t_{DH}	TWHDX	Data Hold Time	10		10		ns
t_{WZ}	TWLQZ	Write Enabled to Output in Hi-Z	0	30	0	35	ns
t_{OW}	TWHQX	Output Active from End of Write	0		0		ns

Write Cycle Waveforms* (Note 7)

Write Cycle No. 1 ($\overline{WE}$ Controlled)



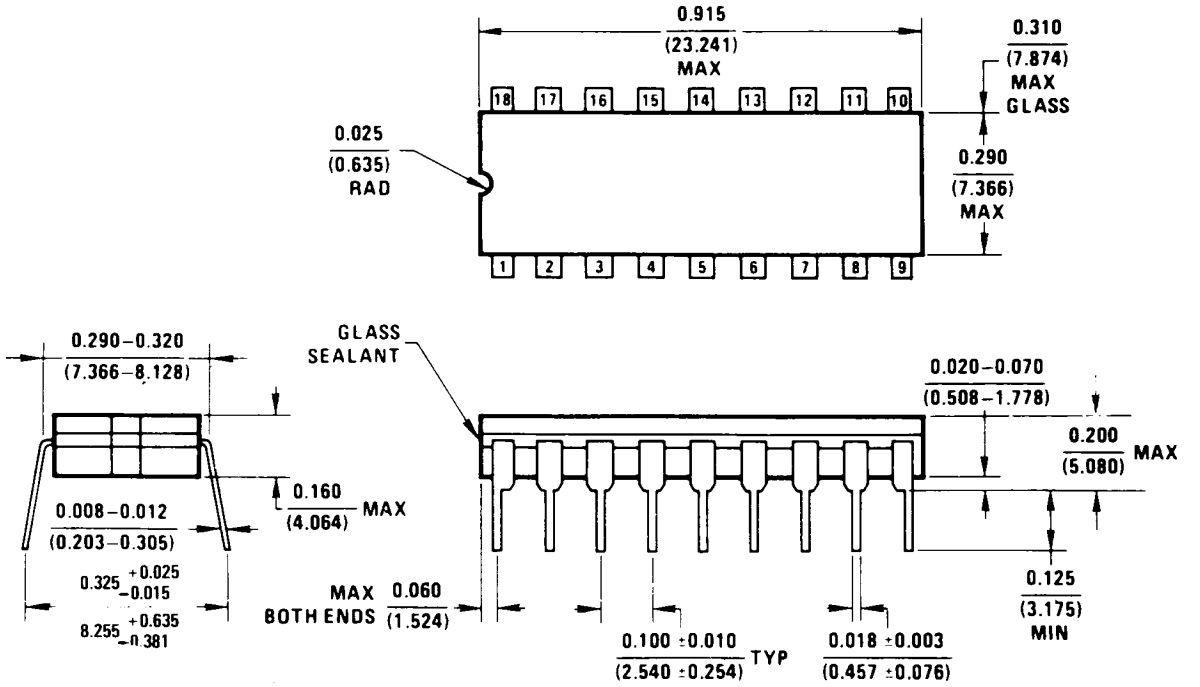
Write Cycle No. 2 ($\overline{CS}$ Controlled)



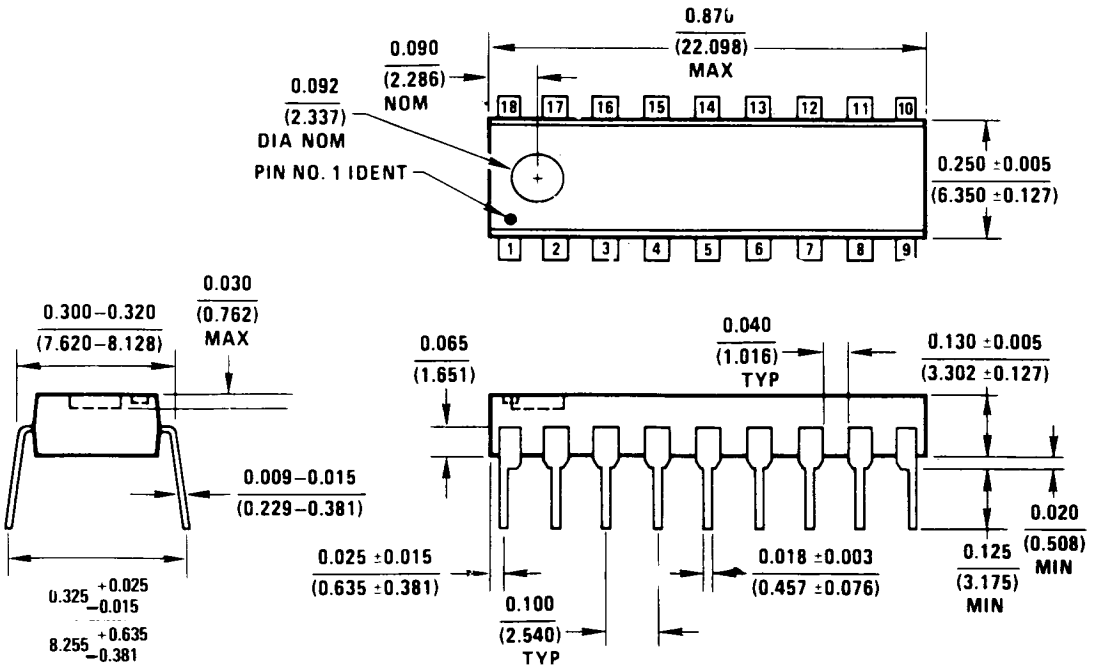
Note 7 : A write occurs during the coincidental low of $\overline{CS}$ and $\overline{WE}$. The output remains TRI-STATE if $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during adress transitions.

*Symbols in parentheses are industry standard.

Physical Dimensions inches (millimeters)



Cavity Dual-In-Line Package (J)
Order Number ET2147J. ETL2147J
or ET2147J-3
Package Number J18A



Moldel Dual-In-Line Package (N)
Order Number ET2147N, ETL2147N
or ET2147N-3
Package Number N18A

EUROTECHNIQUE

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