SEEQ Technology, Incorporated

28C256
Timer E²
256K Electrically Erasable PROM

August 1992

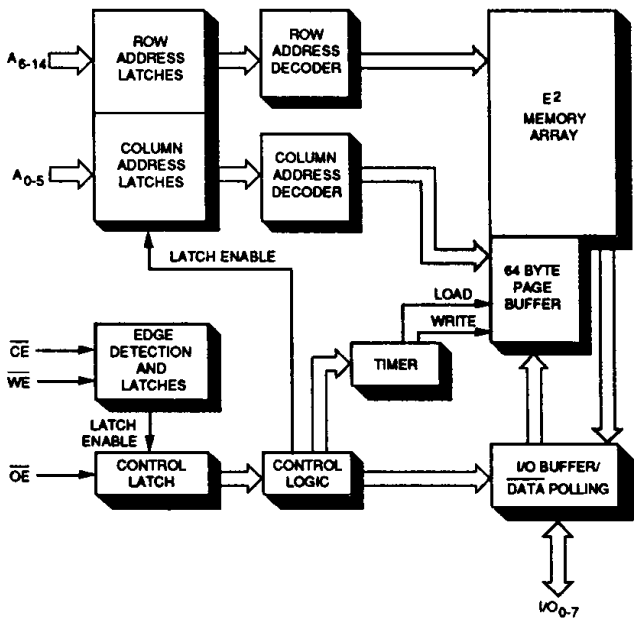
Features

- **Military, Extended and Commercial Temperature Range**
  - –55°C to +125°C Operation (Military)
  - –40°C to +85°C Operation (Extended)
  - 0°C to +70°C Operation (Commercial)
- **CMOS Technology**
- **Low Power**
  - 60 mA Active
  - 250 µA Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160 µs Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - $\overline{\text{DATA}}$ Polling
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- **MIL-STD-883 Class B Compliant**
  5962 SMD Compliant
- **Power Up/Down Protection Circuitry**
- **200 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**

Description

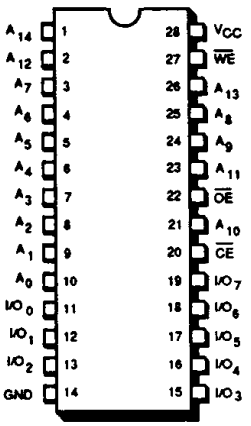
SEEQ's 28C256 is a CMOS 5V only, 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in most popular thru hole and surface mount package options as listed under "Ordering Information". The 28C256 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles

Block Diagram

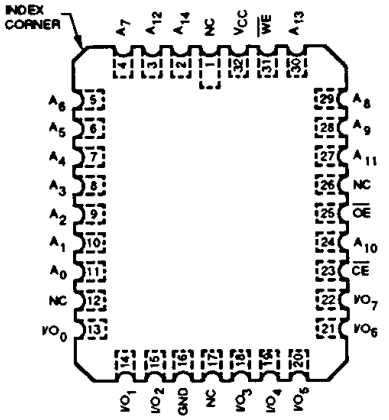


Pin Configuration

DUAL-IN-LINE
TOP VIEW



LEADLESS CHIP CARRIER
TOP VIEW



Note: The PLCC package has the same pin configuration as the LCC except pin 1 and pin 17 are don't connects.

Pin Names

A_0-A_5	ADDRESSES – COLUMN
A_6-A_{14}	ADDRESSES – ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE)/DATA OUTPUT (READ)

per byte and, is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and it's innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

The 28C256 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor for other tasks once the write cycle has been initiated. The 28C256's write cycle time is 10 ms maximum. An automatic byte erase is performed before each byte/page write. The $\overline{DATA}$ polling feature of the 28C256 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 200 ns. Data retention is greater than 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of a forementioned three input lines.

Mode Selection (Table 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write	X	X	V_{IH}	High Z/D_{OUT}
Inhibit	X	V_{IL}	X	High Z/D_{OUT}
Chip Erase	V_{IL}	V_H	V_{IL}	X

X: Any TTL level
V_H: High Voltage

Reads

A read is typically accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{OE}$) to a TTL low. During read, the addresses, $\overline{CE}$, $\overline{OE}$, and input data latches are transparent.

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Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with Output Enable ($\overline{OE}$) being high initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurred first. An automatic erase is performed before data is written.

The 28C256 can write both bytes and a page of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the 28C256 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{OE}$ set up and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data setup and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

Write Mode

One to 64 bytes of data can be randomly loaded into the device. The part latches row addresses, A6-A14, during the first byte write. These addresses are latched on the falling edge of the $\overline{WE}$ signal and are ignored after that until the end of t_{WC}. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write is initiated. These addresses and the $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the 28C256 latches data and starts the internal page load timer. The timer is reset on the falling edge of the $\overline{WE}$ signal if another write is

initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no additional write cycles have been initiated within t_{BLC} after the last $\overline{WE}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can now be read to determine the end of write cycle ($\overline{DATA}$ Polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the 28C256 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{WE}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{DATA}$ Polling

The 28C256 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual end-point of a write cycle. If a read is performed to any address while the 28C256 is **still writing**, the device will present the ones-complement of the last byte written. When the 28C256 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A $\overline{DATA}$ polling read should not be done until a minimum of t_{LP} microseconds after the last byte is written. Timing for a $\overline{DATA}$ polling read is the same as a normal read once the t_{LP} specification has been met.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions.

1. V_{CC} is less than V_{WI} V.
2. A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Range*

Temperature
Storage ..... −65°C to +150°C
Under Bias
Military/Extended ..... −65°C to +135°C
Commercial Temperature ..... −10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground ..... +6.0 V to −0.5 V
Undershoot pulse of less then 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground ..... −1.0 V

Overshoot pulse of less than 10 ns (measred at 50% point)applied to all inputs or outputs with respect to ground ..... + 7.0 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

		28C256-200	28C256-250	28C256-300	28C256-350
Temperature Range	Commercial	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
	Extended	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C	−40°C to +85°C
	Military	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%	5 V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics Read Operation (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		60	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}: All I/O open; Other Inputs = V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O Open; Other Inputs = V_{IL} to V_{IH}
I_{SB2}	Standby V_{CC} Current (CMOS Inputs) Military / Industrial		250	µA	$\overline{CE}$ = V_{CC} –0.3 Other Inputs = V_{IL} to V_{IH} All I/O Open
	Commercial		200	µA	$\overline{CE}$ = V_{CC} –0.3 Other Inputs = V_{IL} to V_{IH} All I/O Open
I_{IL} [2]	Input Leakage Current		1	µA	V_{IN} = V_{CC} Max.
I_{OL} [3]	Output Leakage Current		10	µA	V_{OUT} = V_{CC} Max.
V_{IL}	Input Low Voltage	–0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400 µA
V_{WI} [1]	Write Inhibit Voltage	3.8		V	

NOTES:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.

Capacitance [1] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = OV
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O}$ = OV

A.C. Test Conditions

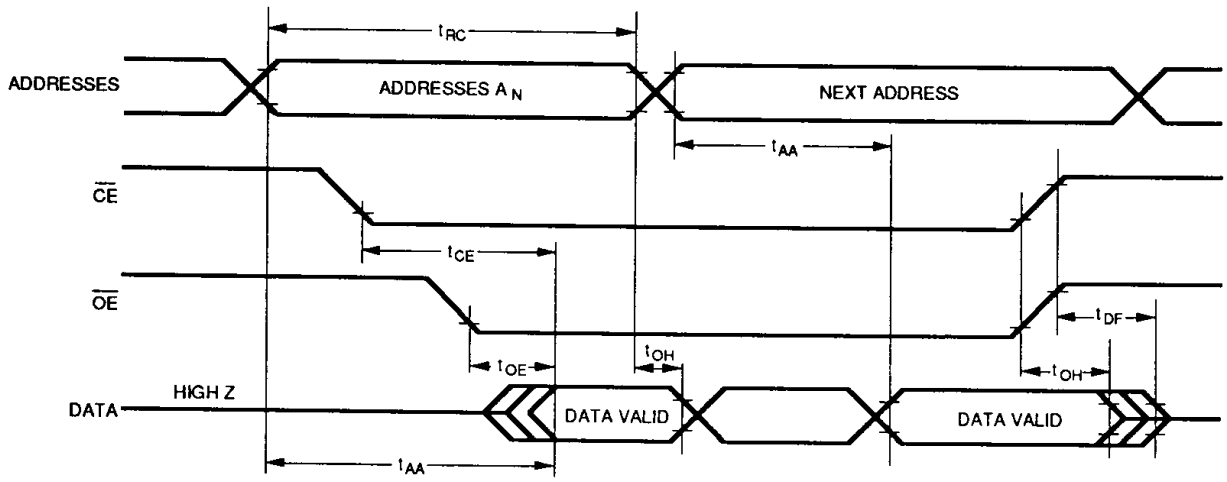
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: < 10 ns
Input Pulse Levels: 0.4 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

AC Characteristics

Read Operation (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits								Units	Test Conditions
		28C256-200		28C256-250		28C256-300		28C256-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE}$ = $\overline{OE}$ =V_{IL}
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE}$ = V_{IL}
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{OE}	Output Enable Access Time		80		90		90		90	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output or Chip Enable High to output in Hi-Z	0	60	0	60	0	80	0	80	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Read /$\overline{DATA}$ Polling Cycle



NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

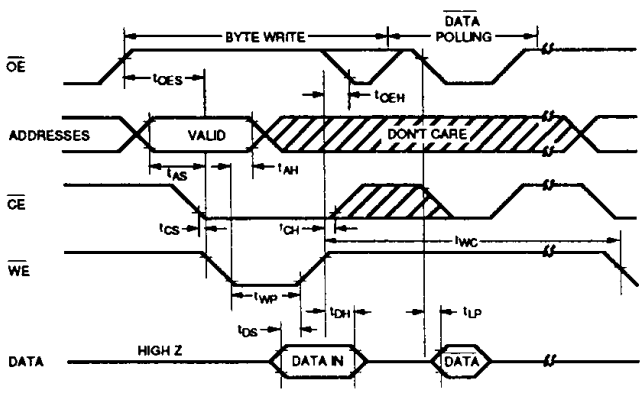
AC Characteristics

Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

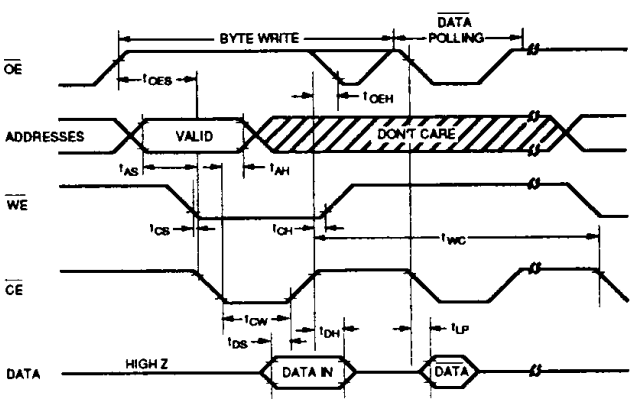
Symbol	Parameter	Limits								Units
		28C256-200		28C256-250		28C256-300		28C256-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	20		20		20		20		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	20		20		20		20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		20		20		20		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	200	0.2	200	0.2	200	0.2	200	µs
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		650		650		650		650	µs

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



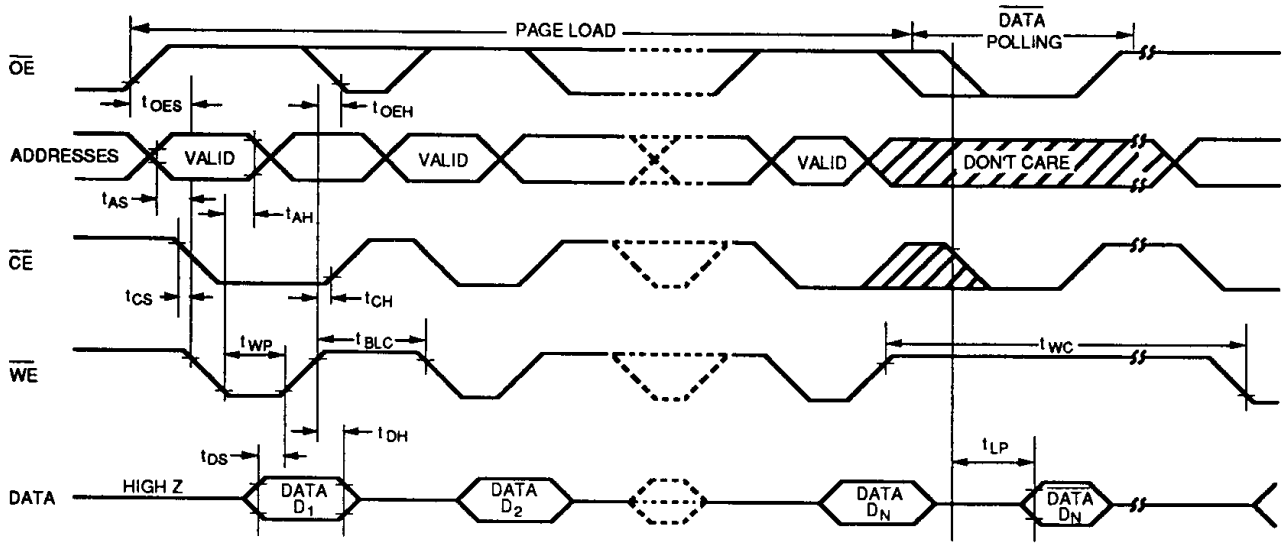
$\overline{CE}$ CONTROLLED WRITE CYCLE



NOTES:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information

D M 28C256 – 250 /B

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D = CERAMIC DIP L = LCC F = FLATPACK N = PLCC P = PLASTIC DIP T = PGA UX = UNENCAPSULATED DIE	M = –55°C to + 125°C (MILITARY) E = –40°C to +85°C (EXTENDED) Q = 0°C to +70°C (COMMERCIAL)	32K x 8 EEPROM	200 = 200 ns 250 = 250 ns 300 = 300 ns 350 = 350 ns	MIL 883 CLASS B SCREENED