Data Sheet
March 1995

AT&T Microelectronics

Optimized Reconfigurable Cell Array (*ORCA*) 1C Series Field-Programmable Gate Arrays (ATT1C03, ATT1C05, ATT1C07, and ATT1C09)

Features

- High density: to 11,400 usable gates
- High I/O: up to 256 usable I/O (for ATT1C09)
- High-performance 0.6 µm CMOS technology
- Fast on-chip user SRAM: 64 bits/PLC
- Innovative programmable logic cell (PLC) architecture for high density and routability
- Four 16-bit look-up tables and four latches/flip-flops per PLC
- Internal carry for fast arithmetic functions
- TTL or CMOS input thresholds programmable per pin
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source
- Nibble-oriented architecture for implementing 4-, 8-, 16-, 32-bit (or wider) bus interfaces
- Built-in boundary scan (*IEEE* 1149.1)
- 100% factory tested
- Low power consumption

Description

The AT&T Optimized Reconfigurable Cell Array (*ORCA*) series is the second generation of SRAM-based field-programmable gate arrays from AT&T. The ATT1C and ATT2C FPGA series provide eleven CMOS FPGAs ranging in complexity from 3,500 to 26,000 gates in a variety of packages, speed grades, and temperature ranges. Table 1 lists the usable gates for the members of the *ORCA* series FPGAs. This data sheet covers the first four members of the *ORCA* series: ATT1C03, ATT1C05, ATT1C07, and ATT1C09.

The *ORCA* series FPGA consists of two basic elements: programmable logic cells (PLCs) and programmable input/output cells (PICs). An array of PLCs is surrounded by PICs, and each PLC contains a programmable function unit (PFU).

The PLCs and PICs also contain routing resources and configuration RAM. All logic is done in the PFU. Each PFU contains four 16-bit look-up tables (LUTs) and four latches/flip-flops (FFs).

The PLC architecture provides a balanced mix of logic and routing which allows a higher utilized gate/PFU than alternative architectures. The routing resources carry logic signals between PFUs and I/O pads. The routing in the PLC is symmetrical about the horizontal and vertical axes. This improves routability by allowing a signal to be routed into the PLC from any direction.

The *ORCA* Foundry Development System is used to process a design from a netlist to a configured FPGA. AT&T provides interfaces and libraries to popular CAE tools for design entry and simulation.

The FPGA functionality is determined by internal configuration RAM. The FPGA's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM, EPROM, or ROM on the circuit board, or any other storage media. The Serial ROMs provide a simple, low pin count method for configuring FPGAs.

Table 1. AT&T *ORCA* 1C Series FPGAs

Device	Usable Gates	Latches/ Flip-Flops	Max User RAM Bits	User I/Os	Array Size
1C03	3,500–4,300	400	6,400	160	10 x 10
1C05	5,000–6,200	576	9,216	192	12 x 12
1C07	7,000–8,800	784	12,544	224	14 x 14
1C09	9,000–11,400	1024	16,384	256	16 x 16

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Description (continued)

ORCA Foundry Development System Overview

The *ORCA* Foundry Development System interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow: at design entry and at the bit stream generation stage.

Following design entry, *ORCA* Foundry's map, place, and route tools translate the netlist into a routed FPGA. The bit stream generator in the development system is then used to generate the configuration data which is loaded into the FPGA's internal configuration RAM. When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, the development system produces configuration data which implements the various logic and routing options discussed in this data sheet.

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	PTA	PTB	PTC	PTD	PTE	PTF	PTG	PTH	PTI	PTJ	PTK	PTL	
PLA	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	PRA
PLB	BA	BB	BC	BD	BE	BF	BG	BH	BI	BJ	BK	BL	PRB
PLC	CA	CB	CC	CD	CE	CF	CG	CH	CI	CJ	CK	CL	PRC
PLD	DA	DB	DC	DD	DE	DF	DG	DH	DI	DJ	DK	DL	PRD
PLE	EA	EB	EC	ED	EE	EF	EG	EH	EI	EJ	EK	EL	PRA
PLF	FA	FB	FC	FD	FE	FF	FG	FH	FI	FJ	FK	FL	PRF
PLG	GA	GB	GC	GD	GE	GF	GG	GH	GI	GJ	GK	GL	PRG
PLH	HA	HB	HC	HD	HE	HF	HG	HH	HI	HJ	HK	HL	PRH
PLI	IA	IB	IC	ID	IE	IF	IG	IH	II	IJ	IK	IL	PRI
PLJ	JA	JB	JC	JD	JE	JF	JG	JH	JI	JJ	JK	JL	PRJ
PLK	KA	KB	KC	KD	KE	KF	KG	KH	KI	KJ	KK	KL	PRK
PLL	LA	LB	LC	LD	LE	LF	LG	LH	LI	LJ	LK	LL	PRL
	PBA	PBB	PBC	PBD	PBE	PBF	PBG	PBH	PBI	PBJ	PBK	PBL	

Figure 1

Figure 1. ATT1C05 Array

Architecture

The *ORCA* Series FPGA is comprised of two basic elements: PLCs and PICs. Figure 1 shows an array of programmable logic cells (PLCs) surrounded by programmable input/output cells (PICs). The ATT1C05 has 144 PLCs arranged in an array of 12 rows and 12 columns. PICs are located on all four sides of the FPGA between the PLCs and the IC edge. The location of a PLC is indicated by its row and column so that a PLC in the second row and third column is BC. PICs are indicated similarly, with PT (top) and PB (bottom) designating rows and PL (left) and PR (right) designating columns, followed by a letter. The routing resources and configuration RAM are not shown. The PICs on the left and right sides are the same height as the PLCs, and the PICs at the top and bottom are the same width as PLCs.

Each PIC contains the necessary I/O buffers to interface to four bond pads. The PICs also contain the routing resources needed to connect signals from the bond pads to/from PLCs. The PICs do not contain any user-accessible logic elements, such as flip-flops.

Combinatorial logic is done in look-up tables (LUTs) located in the PFU. The PFU can be used in different modes to meet different logic requirements. The LUT's configurable medium-/large-grain architecture can be used to implement from one to four combinatorial logic functions. The flexibility of the LUT to handle wide input functions as well as multiple smaller input functions maximizes the gate count/PFU.

Programmable Logic Cells

The programmable logic cell (PLC) consists of a programmable function unit (PFU) and routing resources. All PLCs in the array are identical. The PFU, which contains four LUTs and four latches/FFs for logic implementation, is discussed in the next section.

Programmable Function Unit

The programmable function units (PFUs) are used for logic. The PFU has 19 external inputs and six outputs and can operate in several modes. The functionality of the inputs and outputs depends on the operating mode.

The PFU uses three input data buses (a[4:0], b[4:0], wd[3:0]), four control inputs (c0, ck, ce, lsr), and a carry-input (cin); the last is used for fast arithmetic functions. There is a 5-bit output bus (o[4:0]) and a carry-out (cout).

Figure 2 and Figure 3 show high-level and detailed views of the ports in the PFU, respectively. The ports are referenced with a two- to four-character suffix to a PFU's location. As mentioned, there are two 5-bit input data buses (a[4:0] and b[4:0]) to the LUT, one 4-bit input data bus (wd[3:0]) to the latches/FFs, and an output data bus (o[4:0]).

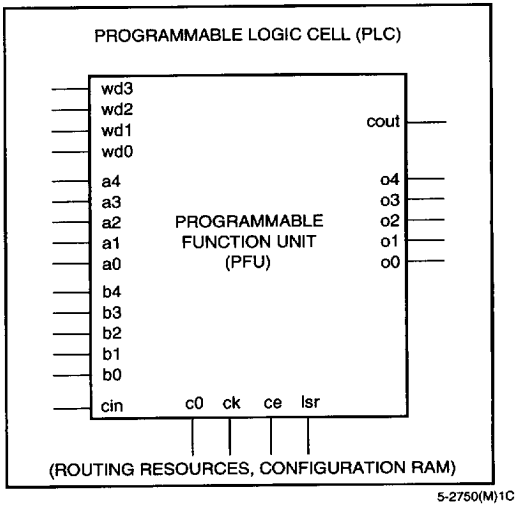


Figure 2. PFU Ports

The PFU is used in a variety of modes, as illustrated in Figures 4 through 11, and it is these modes which are most relevant to PFU functionality.

The PFU does combinatorial logic in the LUT and sequential logic in the latches/FFs. The LUT is static random access memory (SRAM), and can be used for read/write or read-only memory. Table 2 lists the basic operating modes of the LUT. The operating mode affects the functionality of the PFU input and output ports and internal PFU routing.

Programmable Logic Cells (continued)

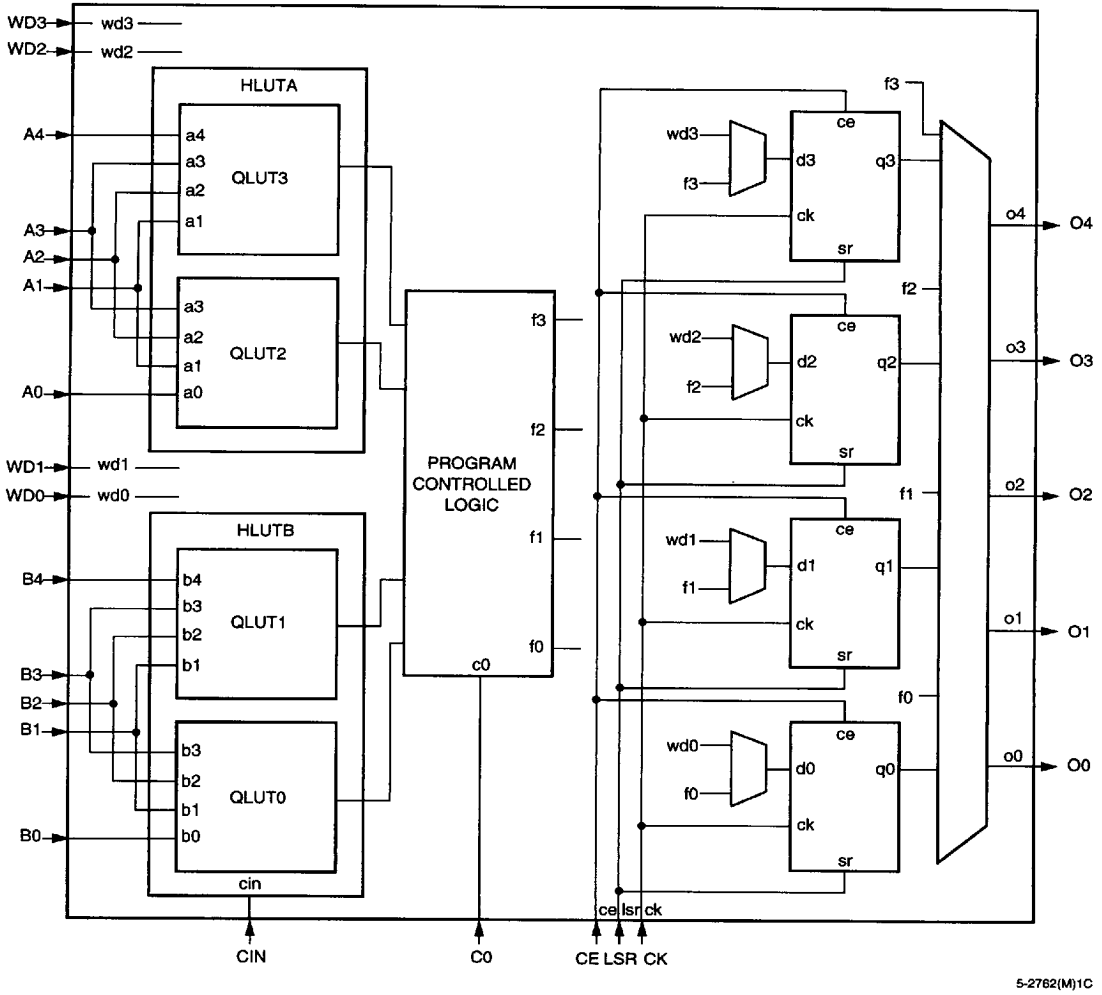


Figure 3. Simplified PFU Diagram

For example, in some operating modes, the wd[3:0] inputs are direct data inputs to the PFU latches/FFs. In the dual 16 x 2 memory mode, the same wd[3:0] inputs are used as a 4-bit data input bus into LUT memory.

Figure 3 shows the four latches/FFs and the 64-bit look-up table (LUT) in the PFU. Each latch/FF can accept data from the LUT. Alternately, the latches/FFs can accept direct data from wd[3:0], eliminating the LUT delay if no combinatorial function is needed. The LUT outputs can bypass the latches/FFs, which reduces the delay out of the PFU. It is possible to use the LUT and latches/FFs more or less independently. For example, the latches/FFs can be used as a 4-bit shift register, and the LUT can be used to detect when a register has a particular pattern in it.

Programmable Logic Cells (continued)

PFU Control Inputs

The four control inputs to the PFU are clock (ck), local set/reset (lsr), clock enable (ce), and c0. The ck, ce, and lsr inputs control the operation of all four latches in the PFU. An active-low global set/reset (gsrn) signal is also available to the latches/FFs in every PFU. Their operation is discussed briefly here, and in more detail in the Latches/Flip-Flops section. The polarity of the control inputs can be inverted.

The ck input is distributed to each PFU from a vertical or horizontal net. The ce input inhibits the latches/FFs from responding to data inputs. The ce input can be disabled, always enabling the clock. Each latch/FF can be independently programmed to be a set or reset by the lsr and the global set/reset (gsrn) signals. Each PFU's lsr input can be configured as synchronous or asynchronous. The gsrn signal is always asynchronous. The lsr signal applies to all four latches/FFs in a PFU. The lsr input can be disabled (the default). The asynchronous set/reset is dominant over clocked inputs.

The c0 input is used as an input in combinatorial logic functions. It is used as an input into special PFU logic gates in wide input functions. The c0 input can be disabled (the default).

Look-Up Table Operating Modes

The LUT can be configured to operate in one of three general modes:

- Combinatorial logic mode
- Ripple mode
- Memory mode

The combinatorial logic mode uses a 64-bit look-up table (LUT) to implement Boolean functions. The two 5-bit logic inputs, a[4:0] and b[4:0], and the c0 input are used as LUT inputs. The use of these ports changes based on the PFU operating mode.

Table 2. Look-Up Table Operating Modes

Mode	Function
F4A	Two functions of four inputs, some inputs shared (QLUT2/QLUT3)
F4B	Two functions of four inputs, some inputs shared (QLUT0/QLUT1)
F5A	One function of five inputs (HLUTA)
F5B	One function of five inputs (HLUTB)
MA	16 x 2 memory (HLUTA)
MB	16 x 2 memory (HLUTB)
R	Ripple—LUT

For combinatorial logic, the LUT can be used to do any single function of six inputs, any two functions of five inputs, or four functions of four inputs (with some inputs shared), and three special functions based on the two five-input functions and c0.

The functionality of the LUT is determined by its operating mode. The entries in Table 2 show the basic modes of operation for combinatorial logic, ripple, and memory functions in the LUT. Depending on the operating mode, the LUT can be divided into sub-LUTs. The LUT is comprised of two 32-bit half look-up tables, HLUTA and HLUTB. Each half look-up table (HLUT) is comprised of two quarter look-up tables (QLUTs). HLUTA consists of QLUT2 and QLUT3, while HLUTB consists of QLUT0 and QLUT1. The outputs of QLUT0, QLUT1, QLUT2, and QLUT3 are f0, f1, f2, and f3, respectively.

If the LUT is configured to operate in the ripple mode, it cannot be used for basic combinatorial logic or memory functions. In modes other than the ripple mode, combinations of operating modes are possible. For example, the LUT can be configured as a 16 x 2 RAM in one HLUT and a five-input combinatorial logic function in the second HLUT. This can be done by configuring HLUTA in the MA mode and HLUTB in the F5B mode (or vice versa).

F4A/F4B Mode—Two Four-Input Functions

Each HLUT can be used to implement two four-input combinatorial functions, but the total number of inputs into each HLUT cannot exceed five. The two QLUTs within each HLUT share three inputs. In HLUTA, the a1, a2, and a3 inputs are shared by QLUT2 and QLUT3. Similarly, in HLUTB, the b1, b2, and b3 inputs are shared by QLUT0 and QLUT1. The four outputs are f0, f1, f2, and f3. The use of the LUT for four functions of up to four inputs each is given in Figure 4.

Programmable Logic Cells (continued)

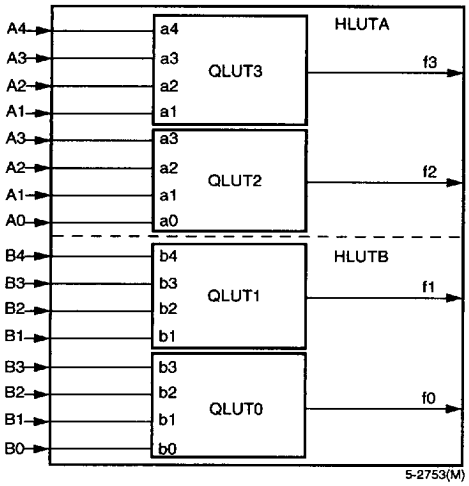


Figure 4. F4 Mode—Four Functions of Four Input Variables

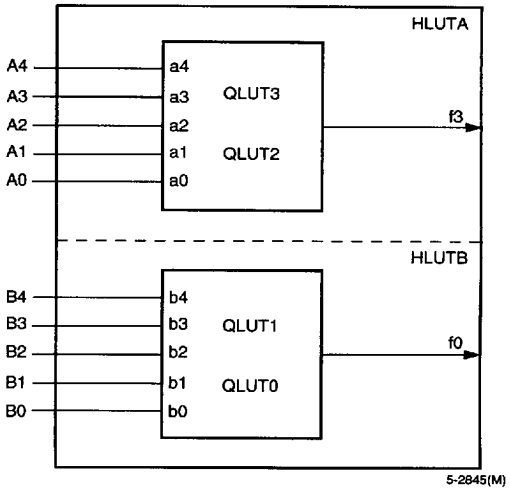


Figure 5. F5 Mode—Two Functions of Five Input Variables

F5A/F5B Mode—One Five-Input Variable Function

Each HLUT can be used to implement any five-input combinatorial function. The input ports are a[4:0] and b[4:0], and the output ports are f0 and f3. One five or less input function is input into a[4:0], and the second five or less input function is input into b[4:0]. The results are routed to the latch/FF d0 and latch/FF d3 inputs, or directly to the outputs o0 and o3. The use of the LUT for two independent functions of up to five inputs is given in Figure 5. In this case, the LUT is configured in the F5A and F5B modes. As a variation, the LUT can do one function of up to five input variables and two four-input functions using F5A and F4B modes or F4A and F5B modes.

F5M and F5X Modes—Special Function Modes

The PFU contains logic to implement two special function modes which are variations on the F5 mode. As with the F5 mode, the LUT implements two independent five-input functions. Figure 6 and Figure 7 show the schematics for F5M and F5X modes. The F5X and F5M functions differ from the basic F5A/F5B functions in that there are three logic gates which have inputs from the LUT. In some cases, this can be used for faster and/or wider logic functions. The HLUTs operate as in the F5 mode, providing outputs on f0 and f3. The resulting output is then input into a NAND and either a multiplexer in F5M mode or an exclusive OR in F5X mode.

As shown, two of the three inputs into the NAND, XOR, and MUX gates, f0 and f3, are from the LUT. The third input is from the c0 input into PFU. The output of the special function (either XOR or MUX) is f1. Since the XOR and multiplexer share the f1 output, the F5X and F5M modes are mutually exclusive. The output of the NAND is f2.

To use either the F5M or F5X functions, the LUT must be in the F5A/F5B mode. In both the F5X and F5M functions, the outputs of the five-input combinatorial functions, f0 and f3, are also usable simultaneously with the logic gate outputs.

The output of the multiplexer is:

$f1 = (HLUTA \times c0) + (HLUTB \times \overline{c0})$

$f1 = (f3 \times c0) + (f0 \times \overline{c0})$

The output of the exclusive OR is:

$f1 = HLUTA \oplus HLUTB \oplus c0$

$f1 = f3 \oplus f0 \oplus c0$

The output of the NAND is:

$f2 = \overline{HLUTA \times HLUTB \times c0}$

$f2 = \overline{f3 \times f0 \times c0}$

Programmable Logic Cells (continued)

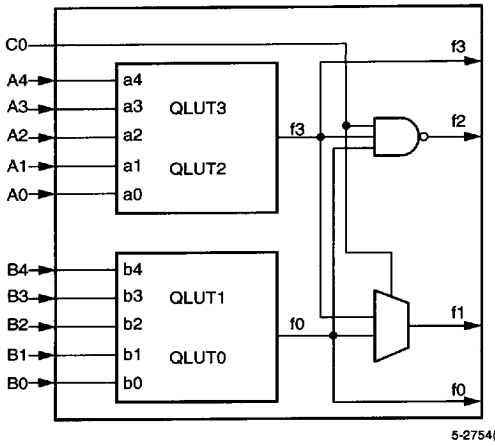


Figure 6. F5M Mode—Multiplexed Function of Two Independent Five-Input Variable Functions

F5M Mode — One Six-Input Variable Function

The LUT can be used to implement any function of six input variables. As shown in Figure 8, five input signals are routed into both the a[4:0] and b[4:0] ports, and the c0 port is used for the sixth input. The output port is f1.

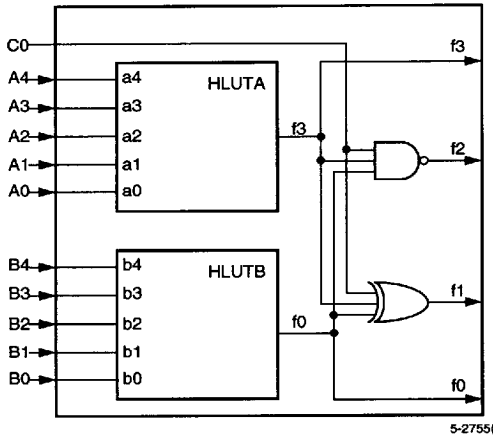


Figure 7. F5X Mode—Exclusive OR Function of Two Independent Five-Input Variable Functions

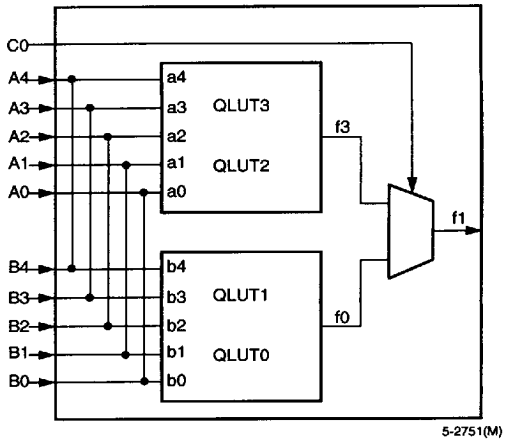


Figure 8. F5M Mode—One Six-Input Variable Function

Ripple Mode

The LUT can do nibble-wide ripple functions with high-speed carry logic. The QLUTs each have a dedicated carry-out net to route the carry to/from the adjacent QLUT. Using the internal carry circuits, fast arithmetic and counter functions can be implemented in one PFU. Similarly, each PFU has carry-in and carry-out ports for fast carry routing between adjacent PFUs.

The ripple mode is generally used in operations on two 4-bit buses. Each QLUT has two operands and a ripple input, and provides a result and ripple (generally carry) output. A single bit is rippled from the previous QLUT and is used as input into the current QLUT. For QLUT0, the ripple input is from the PFU cin port. The cin data can come from either the fast carry routing or the b4 PFU input, or it can be tied to logic 1 or logic 0.

The ripple output is calculated by using generate/propagate circuitry. In ripple mode, the two operands are input into a[3:0] and b[3:0]. The four results bits, one per QLUT, are f[3:0]. The ripple output from QLUT3 can be routed to dedicated carry-out circuitry into any of four adjacent PLCs, or it can be placed on the o4 PFU output, or both. This allows for cascading PLCs in the ripple mode so that nibble-wide ripple functions can be easily expanded to any length. If an up/down counter or adder/subtracter is needed, the control signal is input on a4.

Programmable Logic Cells (continued)

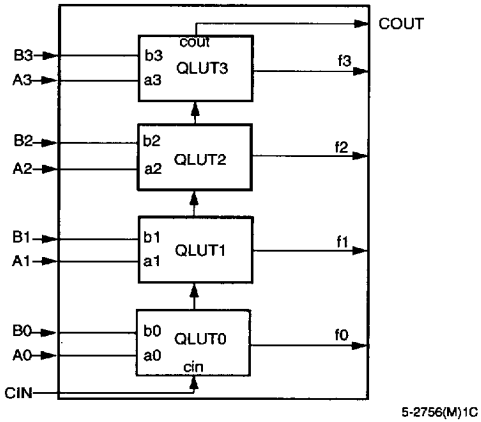


Figure 9. Ripple Mode

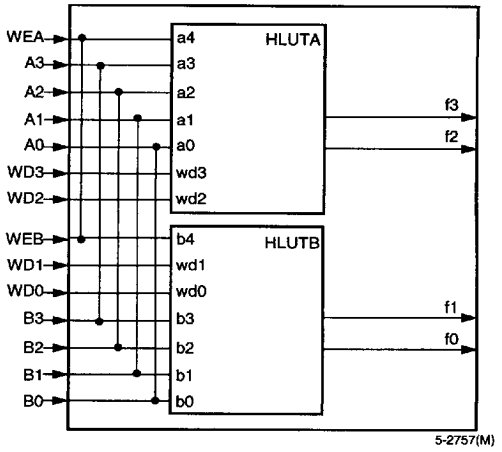


Figure 10. MA/MB Mode—16 x 4 RAM

Each QLUT generates two separate outputs. One of the two outputs selects whether the carry-in is to be propagated to the carry-out of the current QLUT or if the carry-out needs to be generated. The resulting output is placed on the QLUT output. The result bit is created in one half of the QLUT from a single bit from each input bus along with the ripple input bit. These inputs are also used to create the programmable propagate.

Memory Modes—MA and MB Modes

The LUT in the PFU can be configured as either read/write or read-only memory. A read/write address (a[3:0],b[3:0]), write data (wd[1:0], wd[3:2]), and two write enable (wea, web) ports are used for memory. In memory mode, each HLUT can be used as a 16 x 2 memory. Each HLUT is configured independently, allowing functions such as 16 x 4 memory or a 16 x 2 memory in one HLUT and a logic function of five input variables or less in the other HLUT.

Figure 10 illustrates the use of the LUT for a 16 x 4 memory. When the LUTs are used as memory, there are independent address, input data, and output data buses. If the LUT is used as a 16 x 4 read/write memory, the a[3:0] and b[3:0] ports are address inputs. The a4 and b4 ports are write-enable (we) signals. The wd[3:0] inputs are the data inputs. The f[3:0] data outputs can be routed out on the o[4:0] PFU outputs or to the latch/FFs d[3:0] inputs.

To increase memory address locations (e.g., 32 x 4), two or more PLCs can be used. The address and write data inputs for the two PLCs are tied together (bit by bit) and the data outputs are routed through a 3-statable BIDI and then tied together (bit by bit).

The write enable and read enable for each PLC is created from an extended address. The read enable is connected to the 3-state enable input to the BIDIs for a given PLC and then used to enable the 4 bits of data from a PLC onto the read data bus.

To increase the memory's word size (e.g., 16 x 8), two or more PLCs are used again. The address and write enable of the PLCs are tied together, and the data is different for each PLC. Increasing both the address locations and word size is done by using a combination of these two techniques.

The LUT can also be used for both memory and a combinatorial logic function simultaneously. Figure 11 shows the use of a LUT implementing a 16 x 2 RAM (HLUTA) and any function of up to five input variables (HLUTB).

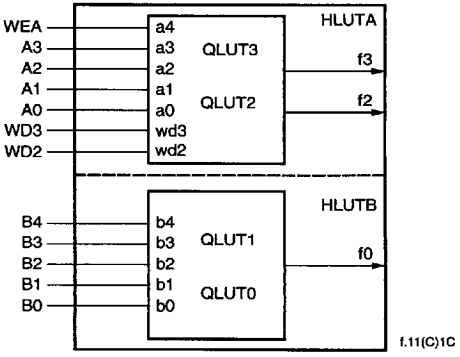


Figure 11. MA/F5 Mode—16 x 2 Memory and One Function of Five Input Variables

Programmable Logic Cells (continued)

Latches/Flip-Flops

The four latches/FFs in the PFU can be used in a variety of configurations. In some cases, the configuration options apply to all four latches/FFs in the PFU. For other options, each latch/FF is independently programmable. Table 3 summarizes these latch/FF options. The latches/FFs can be configured as either positive or negative level sensitive latches, or positive or negative edge-triggered flip-flops. All latches/FFs in a given PFU share the same clock, and the clock to these latches/FFs can be inverted. The input into each latch/FF is from either the corresponding QLUT output, i.e., f[3:0], or the direct data input, wd[3:0]. The four latch/FF outputs q[3:0] can be arbitrarily placed on the five PFU outputs, o[4:0].

Table 3. Configuration RAM Controlled Latch/Flip-Flop Operation

Function	Options
Functionality Common to All Latch/FFs in PFU	
LSR Operation	Asynchronous or Synchronous
Clock Polarity	Noninverted or Inverted
Front-End Select	Direct (wd[3:0]) or from LUT (f[3:0])
Functionality Set Individually in Each Latch/FF in PFU	
Latch/FF Mode	Latch or Flip-Flop
Set/Reset Mode	Set or Reset

The four latches/FFs in a PFU share the clock (ck), clock enable (ce), and local set/reset (lsr) inputs. When ce is disabled, each latch/FF retains its previous value when clocked, unless there is an asynchronous set/reset. Both the clock enable and lsr inputs can be inverted to be active-low.

The set/reset operation of the latch/FF is controlled by two parameters: reset mode and set/reset value. When neither the global (gsrn) or local set/reset (lsr) are active, the storage element operates normally as a latch or FF. The reset mode is used to select either synchronous or asynchronous lsr operation. If synchronous, lsr is enabled only if clock enable (ce) is active.

The clock enable is supported on FFs, not latches, and is implemented using a two-input multiplexer on the FF input, where one input is the previous state of the FF and the other input is the data applied to the FF. The select of this two-input multiplexer is clock enable (ce). When ce is inactive, the FF output does not change when the clock edge arrives.

The global reset, gsrn, is only asynchronous, and it sets/resets all latches/FFs in the FPGA, based upon the set/reset configuration bit for each latch/FF. The set/reset value determines whether gsrn and lsr is a set or reset input. The set/reset value is independent for each latch/FF.

If the local set/reset is not needed, the latch/FF can be configured to have a data front-end select. Two data inputs are possible in the front-end select mode, with the lsr signal used to select which data input is used. As mentioned, the data input into each latch/FF is from the output of its associated QLUT or direct from wd[3:0], bypassing the LUT. In the front-end data select mode, both signals are available to the latches/FFs.

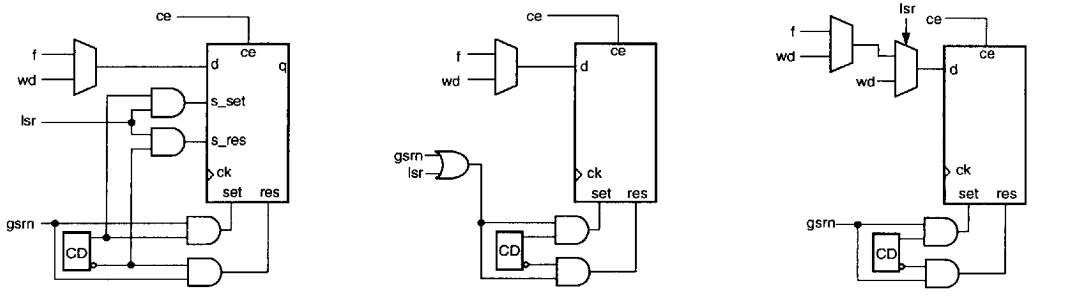
The latches/FFs can be configured in three modes:

1. Local synchronous set/reset: the input into the PFU's lsr port is used to synchronously set or reset each latch/FF.
2. Local asynchronous set/reset: the input into lsr asynchronously sets or resets each latch/FF.
3. Latch/FF with front-end select: the data select signal (actually lsr) selects the input into the latches/FFs between the LUT output and direct data in.

For all three modes, each latch/FF can be independently programmed as either set or reset. Each latch/FF in the PFU is independently configured to operate as either a latch or flip-flop.

Figure 12 provides the logic functionality of the front-end select, global set/reset, and local set/reset operations. To speed up the interface between signals external to the FPGA and the latches/FFs, there are direct paths from latch/FF outputs to the I/O pads. This is done for each PLC that is adjacent to a PIC.

Programmable Logic Cells (continued)



Note: CD = configuration data.

Figure 12. Latch/FF Set/Reset Configurations

PLC Routing Resources

Routing Resources

Generally, the *ORCA* Foundry Development System is used to automatically route interconnections. Interactive routing with the *ORCA* Foundry design editor (*EPIC*) is also available for design optimization. To use *EPIC* for interactive layout, an understanding of the routing resources is needed and is provided in this section.

The routing resources consist of switching circuitry and metal interconnect segments. Generally, the metal lines which carry the signals are designated as routing nodes (R-nodes). The switching circuitry connects the routing nodes, providing one or more of three basic functions: signal switching, amplification, and isolation. A net running from a PFU or PIC output (source) to a PLC or PIC input (destination) consists of one or more R-nodes, connected by switching circuitry designated as configurable interconnect points (CIPs).

The following sections discuss the switching circuitry, intra-PLC routing, inter-PLC routing, and clock distribution.

Configurable Interconnect Points

The process of connecting R-nodes uses three basic types of switching circuits: two types of configurable interconnect points (CIPs) and bidirectional buffers (BIDIs). The basic element in CIPs is one or more pass transistors, each controlled by a configuration RAM bit.

The two types of CIPs are mutually exclusive (or multiplexed) and independent. A mutually exclusive set of CIPs contains two or more CIPs, only one of which can be on at a time. An independent CIP has no such restrictions and can be on independent of the state of other CIPs. Figure 13 shows an example of both types of CIPs.

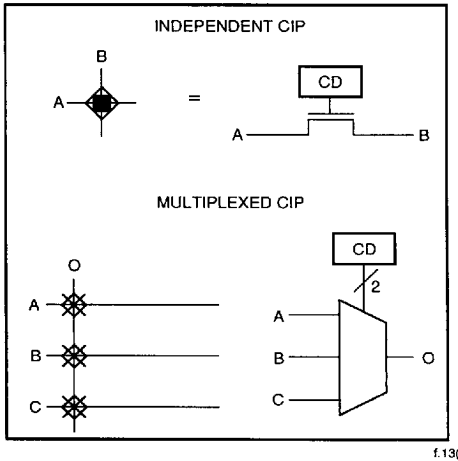


Figure 13. Configurable Interconnect Points

PLC Routing Resources (continued)

3-Statable Bidirectional Buffers

Bidirectional buffers provide isolation as well as amplification for signals routed a long distance. Bidirectional buffers are also used to drive signals directly onto either vertical or horizontal xL R-nodes (to be described later in the inter-PLC routing section). BIDIs are also used to indirectly route signals through the switching R-nodes. Any number from zero to four BIDIs can be used in a given PLC.

2

An application net can be connected to the TRI input of the BIDI controller to 3-state/enable the BIDIs under user control. If one of the BIDIs in the PLC is 3-statable, all are 3-statable by the TRI signal. The TRI input signal can also be inverted to be active-low. Figure 14 shows the four 3-statable bidirectional buffers in each PLC.

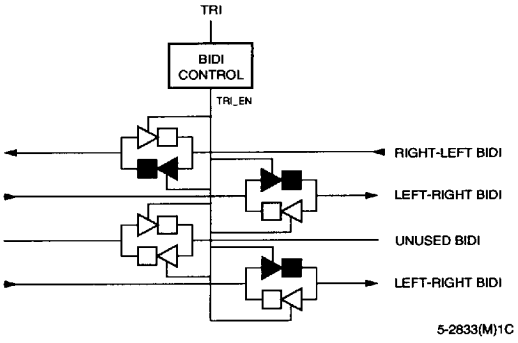


Figure 14. 3-Statable Bidirectional Buffers

Intra-PLC Routing Resources

The function of the intra-PLC routing resources is to connect the PFU's input and output ports to the routing resources used for entry to and exit from the PLC. These are nets for providing PFU feedback, turning corners, or switching from one type of routing resource to another.

PFU Input and Output Ports. There are nineteen input ports to each PFU. The PFU input ports are labeled a[4:0], b[4:0], wd[3:0], c0, ck, lsr, cin, and ce. The six output ports are o[4:0] and cout. These ports correspond to those described in the PFU section.

Switching R-Nodes. There are four sets of switching R-nodes in each PLC, one in each corner. Each set consists of five switching elements, labeled sul[4:0], sur[4:0], sll[4:0], and slr[4:0], for the upper-left, upper-right, lower-left, and lower-right sections of the PFUs, respectively. The switching R-nodes connect to the PFU inputs and outputs as well as the BIDI R-nodes, to be described later. They also connect to both the horizontal and vertical x1 and x4 R-nodes (inter-PLC routing resources, described below) in their specific corner.

One of the four sets of switching R-nodes can be connected to a set of switching R-nodes in each of the four adjacent PLCs or PICs. This allows direct routing of up to five signals without using inter-PLC routing.

BIDI R-Nodes. Each side of the four BIDIs in the PLC is connected to a BIDI R-node: BL[3:0] on the left and BR[3:0] on the right. These R-nodes can also be connected to the xL R-nodes through CIPs, with BL[3:0] connected to the vertical xL R-nodes, and BR[3:0] connected to the horizontal xL R-nodes. Both BL[3:0] and BR[3:0] also have CIPs which connect to the switching R-nodes.

PLC Routing Resources (continued)

Inter-PLC Routing Resources

The inter-PLC routing is used to route signals between PLCs. The R-nodes occur in groups of four, and differ in the numbers of PLCs spanned. The x1 R-nodes span one PLC, the x4 R-nodes span four PLCs, and the xL R-nodes span the width (height) of the PLC array. All three types of R-nodes run in both the horizontal and vertical directions. Table 4 shows the groups of inter-PLC R-nodes in each PLC for three array sizes (1C03, 1C05, 1C07).

Table 4. Inter-PLC Routing Resources

Horizontal R-Nodes	Vertical R-Nodes	Distance Spanned
hx1[3:0]	vx1[3:0]	One PLC
hx1[7:4]	vx1[7:4]	One PLC
hx4[3:0]	vx4[3:0]	Four PLCs
hx4[7:4]	vx4[7:4]	Four PLCs
hxL[3:0]	vxL[3:0]	PLC Array

In the table, there are two rows/columns each for x1 and x4 lines. In the design editor, the horizontal x1 and x4 R-nodes are located above and below the PFU. Similarly, the vertical segments are located on each side. The xL R-nodes only run below and to the left of the PFU. The indexes specify individual R-nodes within a group. For example, the vx4[2] R-node runs vertically to the left of the PFU, spans four PLCs, and is the third line in the 4-bit wide bus.

Figure 15 shows the inter-PLC routing within one PLC. Figure 16 provides a more global view of inter-PLC routing resources across multiple PLCs.

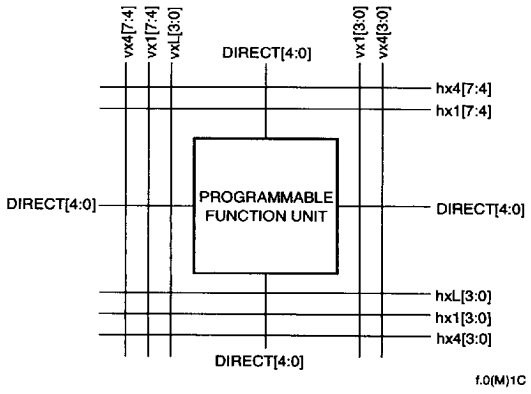


Figure 15. Single PLC View of Inter-PLC R-Nodes

x1 R-Nodes. There are a total of sixteen x1 R-nodes per PLC: eight vertical and eight horizontal. Each of these is subdivided into nibble-wide buses: hx1[3:0], hx1[7:4], vx1[3:0], and vx1[7:4]. An x1 line is one PLC long. If a net is longer than one PLC, an x1 R-node can be lengthened to n times its length by turning on n – 1 CIPs. A signal is routed onto an x1 R-node via the switching R-nodes.

x4 R-Nodes. There are four sets of four x4 R-nodes for a total of 16 x4 R-nodes per PLC. They are hx4[3:0], hx4[7:4], vx4[3:0], and vx4[7:4]. Each set of x4 R-nodes is twisted each time it passes through a PLC, and one of the four is broken with a CIP. This allows a signal to be routed for a length of four cells in any direction on a single line without additional CIPs. The x4 R-nodes can be used to route any nets that require minimum delay. A longer net is routed by connecting two x4 R-nodes together by a CIP. The x4 R-nodes are accessed via the switching R-nodes.

xL R-Nodes. The xL R-nodes run vertically and horizontally the height and width of the array, respectively. There are a total of eight xL R-nodes per PLC: four horizontal, hxL[3:0], and four vertical, vxL[3:0]. Each PLC column has four xL lines, and each PLC row has four xL R-nodes. The ATT1C03, which consists of a 10 x 10 array of PLCs, contains 40 vxL and 40 hxL R-nodes. They are intended primarily for global signals which must travel long distances and require minimum delay and/or skew, such as clocks.

There are three methods to route signals onto the xL R-nodes. In each PLC, there are two long line drivers, one for a horizontal xL and one for a vertical xL R-node. Using the long line drivers produces the least delay. The xL R-nodes can also be driven directly by PFU outputs using the BIDI R-nodes. In the third method, the xL R-nodes are accessed by the bidirectional buffers, again using the BIDI R-nodes.

PLC Routing Resources (continued)

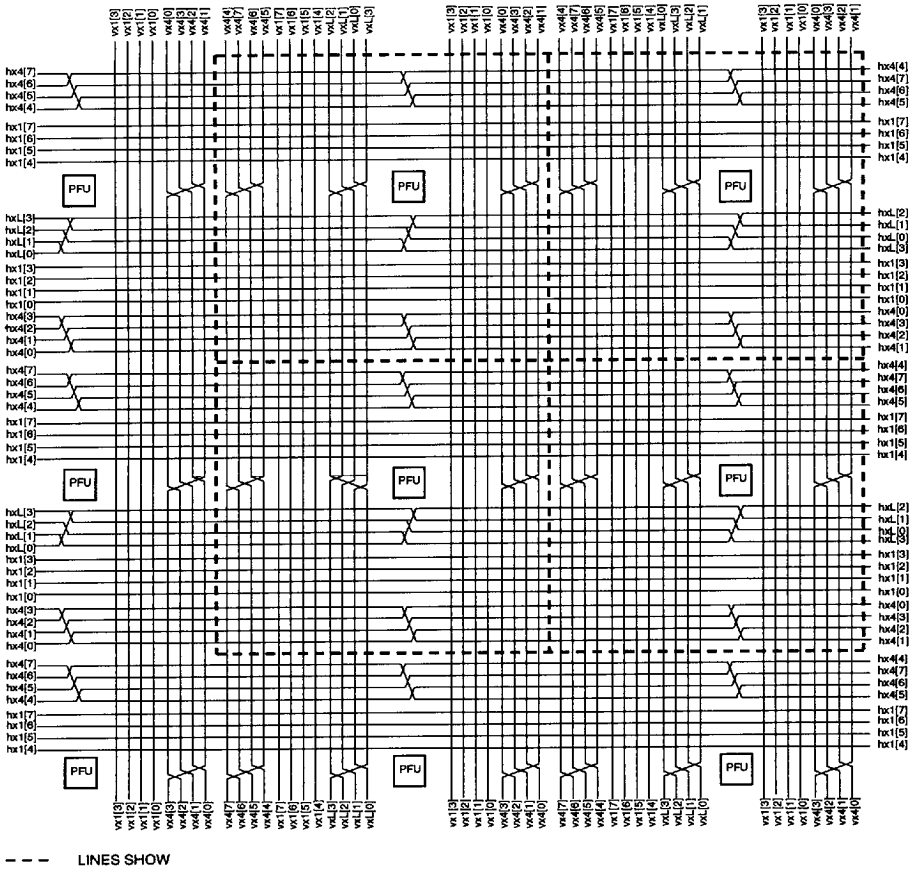


Figure 16. Multiple PLC View of Inter-PLC Routing

Minimizing Routing Delay

The CIP is an active element used to connect two R-nodes. As an active element, it adds significantly to the resistance and capacitance of a net, thus increasing the net's delay. The advantage of the x1 R-node over an x4 R-node is routing flexibility. A net from PLC db to PLC cb is easily routed by using x1 R-nodes. As more CIPs are added to a net, the delay increases. To increase speed, routes that are greater than two PLCs away are routed on the x4 R-nodes because a CIP is located only in every fourth PLC. A net which spans eight PLCs requires seven x1 R-nodes and six CIPs. Using x4 R-nodes, the same net uses two R-nodes and one CIP.

All routing resources in the PLC can carry 4-bit buses. In order for data to be used at a destination PLC that is in data path mode, the data must arrive unscrambled. For example, in data path operation, the least significant bit 0 must arrive at either a[0] or b[0]. If the bus is to be routed by using either x4 or xL R-nodes, both of which twist as they propagate, the bus must be placed on the appropriate lines at the source PLC so that the data arrives at the destination unscrambled.

The switching R-nodes provide the most efficient means of connecting adjacent PLCs. Signals routed using the switching R-nodes have minimum propagation delay.

PLC Routing Resources (continued)

Clock Distribution Network

The *ORCA* Series clock distribution scheme does not require the use of dedicated clock input pins. This provides the system designer with flexibility in assigning clock input pins. One advantage is that board-level clock traces routed to the FPGA are shorter. On a PC board, the added length of high-speed clock traces routed to dedicated-clock input pins can significantly increase the parasitic impedances. The primary advantage of the *ORCA* clock distribution is the availability of a large number of clocks, since all I/O pins are configurable as clocks.

If the clock signal originates from either side of the FPGA, it can be routed through the bidirectional buffers in the PIC onto one of the adjacent PLC's horizontal xL R-nodes. If the clock signal originates from either the top or bottom of the FPGA, the vertical xL R-nodes are used for this purpose. In either case, an xL R-node is used as the clock spine.

Figure 17 illustrates the distribution of a low-skew clock to a large number of loads using a main spine and branches. From the main spine of the clock, network branches are tapped into individual PLCs. Detail A shows the routing of the clock spine from the input pads to the vxL R-nodes using the BIDIHs. Detail B shows the routing from a branch into the PFU.

In each PLC, a low-skew connection through a long line driver can be used to connect a horizontal xL R-node to a vertical xL R-node or vice versa. This is used to route the branches from the clock spine. If the clock spine is a vertical xL R-node, then the branches are horizontal xL R-nodes and vice versa. The clock is then routed into each PLC from the xL R-node clock branches.

To minimize skew, the PLC clock input for all PLCs must be connected to the branch xL R-nodes, not the spine xL R-node. Even in PLCs where the clock is routed from the spine to the branches, the clock should be routed back into the PLC from the clock branch. If the clock is to drive only a limited number of loads, the PFUs can be connected directly to the clock spine. In this case, all flip-flops driven by the clock must be located in the same row or column.

Alternatively, the clock can be routed from the spine to the branches by using the BIDIs instead of the long line drivers. This results in added delay in the clock net, but the clock skew is approximately equal to the clock routed using the long line drivers. Clock signals such as the output of a counter can also be generated in PLCs and routed onto an xL R-node, which then acts as a clock spine. Although the clock can be generated in any PLC, it is recommended that the clock be located as close to the center of the FPGA as possible to minimize clock skew.

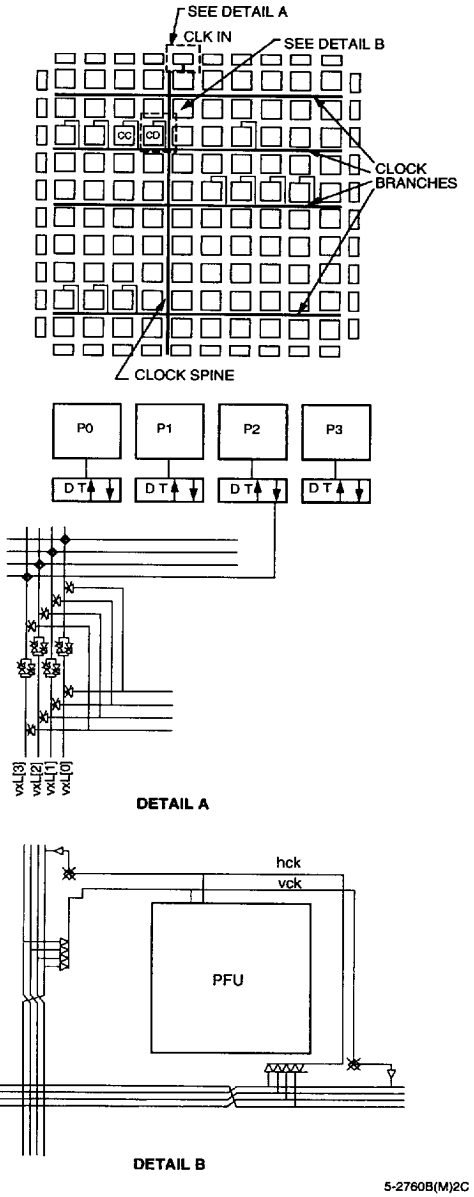


Figure 17. Clock Distribution Network

PLC Architectural Description

Figure 18 is an architectural drawing of the PLC. The drawing shows the PFU, the R-nodes, and the CIPs. A discussion of each of the letters in the drawing follows.

A. There are switching R-nodes which give the router flexibility. In general switching theory, the more levels of indirection in the routing, the more routable the network. The switching R-nodes can also connect to adjacent PLCs.

The switching R-nodes can provide direct connections to PLCs directly to the top, bottom, left, and right, without using other routing resources. The ability to disable this connection between PLCs is provided so each side of these connections can be used exclusively as switching R-nodes in their respective PLC.

B. These CIPs connect the x1 routing. These are located in the middle of the PLC to allow the block to connect to either the left end of the horizontal x1 R-node from the right or the right end of the horizontal x1 R-node from the left, or both. By symmetry, the same principle is used in the vertical direction. The x1 lines are not twisted, making them suitable for data paths.

C. This pattern of CIPs is used to connect the x1 and x4 nets to the switching R-nodes, or to other x1 and x4 nets.

The CIPs on the major diagonal allow data to be transmitted from x1 nets to the switching R-nodes without being scrambled. The CIPs on the major diagonal also allow unscrambled data to be passed between the x1 and x4 nets.

In addition to the major diagonal CIPs for the x1 lines, other CIPs provide an alternative entry path into the PLC in case the first one is already used. The other CIPs are arrayed in two patterns, as shown. Both of these patterns start with the main diagonal, but the extra CIPs are arrayed on either a parallel diagonal shifted by one or shifted by two (modulo the size of the vertical bus (5)). This allows any four application nets incident to the PLC corner to be transferred to the five switching R-nodes in that corner. Many patterns of five nets can also be transferred.

D. The x4 R-nodes are twisted each time they pass through a PLC. One of the four x4 lines is broken with a CIP. This allows a signal to be routed a distance of four PLCs in any direction on a single R-node, without an intermediate CIP. The x4 R-nodes are less populated with CIPs than the x1 lines to increase their speed. A CIP can be enabled to extend the x4 R-node four more PLCs, and so on.

For example, if an application signal is routed onto hx4[4] in a PLC, it appears on hx4[5] in the PLC to the right. This signal step-up continues until it reaches hx4[7] two PLCs later. At that point, the user can break the connection or continue the signal for another four PLCs.

E. These symbols are bidirectional buffers (BIDIs). There are four BIDIs per PLC, and they provide signal amplification as needed to decrease signal delay. The BIDIs are also used to transmit signals on xL lines.

F. The 3-state control signal can be disabled. It can be configured as active-high or active-low.

G. This set of CIPs allows a BIDI to get or put a signal from two sets of switching R-nodes on each side. The BIDIs can be accessed by the switching R-nodes. These CIPs allow a nibble of data to be routed though the BIDIs and continue to a subsequent block. They also provide an alternative routing resource to improve routability.

H. These CIPs are used to take data from/to the BIDIs to/from the xL R-nodes. These CIPs have been optimized to allow the BIDI buffers to drive the large load usually seen when using xL R-nodes.

I. Each latch/FF can accept data from a LUT output or a direct data input signal from general routing. In addition, the LUT outputs can bypass the latches/FFs completely and output data on the general routing resources. The four inputs shown are used as the direct input to the latches/FFs. If the LUT is in memory mode, the four inputs wd[3:0] are the data input to the memory.

PLC Architectural Description (continued)

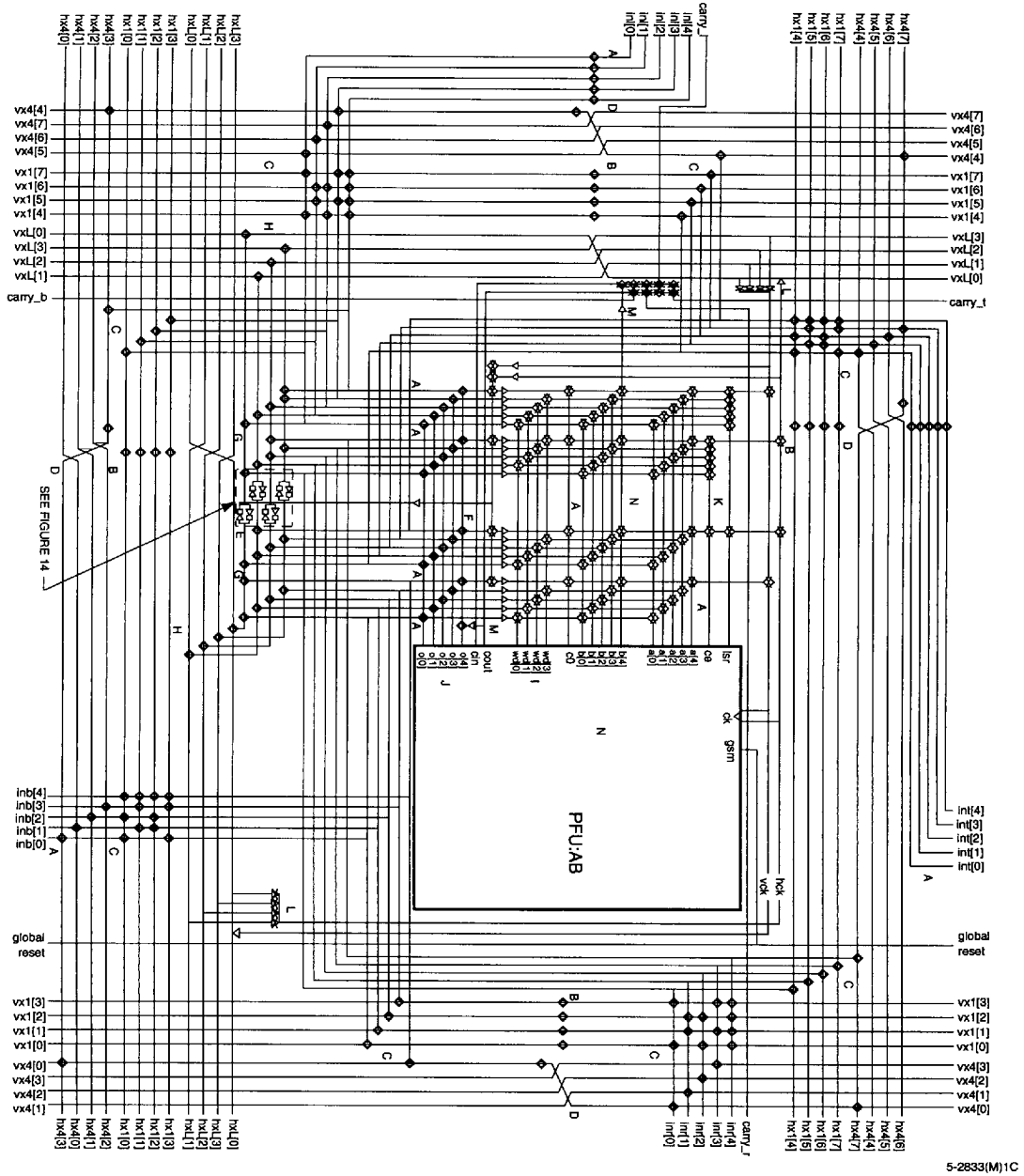


Figure 18. PLC Architecture

PLC Architectural Description
(continued)

J. Any five of the eight output signals can be routed out of the PLC. The eight signals are the four LUT outputs (f0, f1, f2, f3) and the four latch/FF outputs (q0, q1, q2, q3). This allows the user to access all four latch/FF outputs, read the present state and next state of a latch/FF, build a 4-bit shift register, etc. Each of the outputs can drive any number of the five PFU outputs. The speed of a signal can be increased by dividing its load among multiple PFU output drivers.

K. These lines deliver the auxiliary signals clock enable and set/reset to the latches/FFs. All four of the latches/FFs share these signals.

L. This is the clock input to the latches/FFs. Any of the horizontal and vertical long lines can drive the clock of the PLC latches/FFs. Long line drivers are provided so that a PLC can drive one long line in the horizontal direction and one long line in the vertical direction. The four long lines in each direction exhibit the same properties as x4 lines except there are no CIPs.

   The long lines run the length or width of the PLC array. They rotate to allow four PLCs in one row or column to generate four independent global signals. These lines do not have to be used for clock routing. Any highly used application net can use this resource, especially one requiring low skew.

M. These R-nodes are used to route the fast carry signal to/from the neighboring four PLCs. The carry-out (cout) of the PFU can also be routed out of the PFU onto the fifth output (o4). The carry-in (cin) signal can also be supplied by the B4 input to the PFU.

N. These are the 11 logic inputs to the LUT. The a[4:0] inputs are provided into HLUTA, and the b[4:0] inputs are provided into HLUTB. The c0 input bypasses the main LUT and is used in the pfumux, pfuxor, and pfunAND functions (F5M, F5X modes). Since this input bypasses the LUT, it can be used as a fast path around the LUT, allowing the implementation of fast, wide combinatorial functions. The c0 input can be disabled or inverted.

Programmable Input/Output Cells

The programmable input/output cells (PICs) are located along the perimeter of the device. Each PIC interfaces to four bond pads and contains the necessary routing resources to provide an interface between I/O pads and the PLCs. Each PIC is composed of input buffers, output buffers, and routing resources as described below. Table 5 provides an overview of the programmable functions in an I/O cell. Figure 19 is a simplified diagram of the functionality of the *ORCA* series I/O cells.

Table 5. Input/Output Cell Options

Input	Option
Input Levels	TTL/CMOS
Input Speed	Fast/Delayed
Float Value	Pull-up/Pull-down/None
Output	**Option**
Output Drive	12 mA/6 mA or 6 mA/3 mA
Output Speed	Fast/Slewlim/Sinklim
Output Source	FF Direct Out/General Routing
Output Sense	Active-high/low
3-State Sense	Active-high/low (3-state)

Inputs

Each I/O can be configured to be either an input, an output, or bidirectional I/O. Inputs can be configured as either TTL or CMOS compatible. To allow zero hold time on PLC latches/FFs, the input signal can be delayed. Pull-up or pull-down resistors are available on inputs to minimize power consumption. Inputs should have transition times of less than 100 ns and should not be left floating. If an input can float, a pull-up or pull-down should be enabled.

Floating inputs increase power consumption, produce oscillations, and increase system noise. The inputs have a typical hysteresis of approximately 280 mV to reduce sensitivity to input noise. The PIC contains input circuitry which provides protection against latch-up and electrostatic discharge.

Programmable Input/Output Cells
(continued)

Outputs

The PIC's output drivers have programmable drive capability and slew rates. Three propagation delays (fast, slewlim, sinklim) are available on output drivers. The sinklim mode has the longest propagation delay and is used to minimize system noise and minimize power consumption. The fast and slewlim modes allow critical timing to be met.

The drive current is 12 mA sink/6 mA source for the slewlim and fast output speed selections and 6 mA sink/3 mA source for the sinklim output. Two adjacent outputs can be interconnected to increase the output sink current to 24 mA.

All outputs that are not speed critical should be configured as sinklim to minimize power and noise. The number of outputs that switch simultaneously in the same direction should be limited to minimize ground bounce. It may be beneficial to locate heavily loaded output buffers near the ground pads. Ground bounce is generally a function of the driving circuits, traces on the PCB, and loads, and is best determined with a circuit simulation. Outputs can be inverted and 3-state control signals can be active-high or active-low. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only by a low.

At powerup, the output drivers are in slewlim mode and the input buffers are configured as TTL-level compatible with a pull-up. If an output is not to be driven in the selected configuration mode, the output is 3-stated.

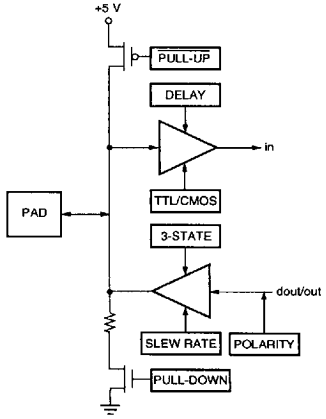


Fig.19(C)1C

Figure 19. Simplified Diagram of Programmable I/O Cell

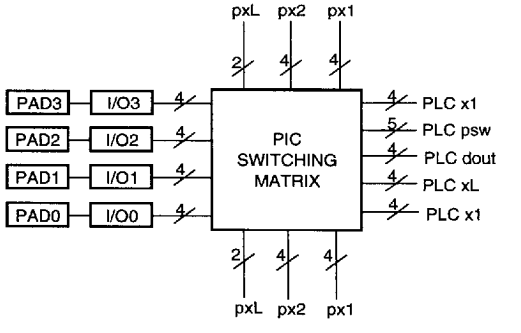
PIC Routing Resources

The PIC routing is designed to route 4-bit wide buses efficiently. For example, any four consecutive I/O pads can have both their input and output signals routed into one PLC. Using only PIC routing, either the input or output data can be routed to/from a single PLC from/to any eight pads in a row.

The connections between PLCs and the I/O pad are provided by two basic types of routing resources. These are routing resources internal to the PIC and routing resources used for PIC-PLC connection. Figures 20 and 21 show a high-level and detailed view of these routing resources.

The PIC's name is represented by a three-letter designation to indicate its location. The first letter, P, designates that the cell is a PIC and not a PLC. The second letter indicates the side of the array where the PIC is located. The four sides are left (L), right (R), top (T), and bottom (B). The third letter indicates either the row (for the left or right sides) or the column (for the top or bottom side). As an example, PIC PLD is located on the left side in the fourth row.

Each PIC has four pads and each pad can be configured as an input, an output (3-statable), a direct output, or a bidirectional I/O. When the pads are used as inputs, the external signals are provided to the internal circuitry at in[3:0]. When the pads are used as outputs, the internal signals connect to the pads through out[3:0]. When the pads are used as direct outputs, the output from the latches/flip-flops in the PLCs to the PIC is designated dout[3:0]. When the outputs are 3-statable, the 3-state enable signals are ts[3:0].



f.20(M)1C

Figure 20. Simplified PIC Routing Diagram

Programmable Input/Output Cells

(continued)

Routing Resources Internal to the PIC

For inter-PIC routing, the PIC contains ten R-nodes used to route signals around the perimeter of the FPGA. Figure 20 shows these lines running vertically for a PIC located on the left side. Figure 21 shows the R-nodes running horizontally for a PIC located at the top of the FPGA.

2

pxL R-Nodes. Each PIC has two pxL R-nodes, labeled pxL[1:0]. Like the xL R-nodes of the PLC, the pxL R-nodes span the entire edge of the FPGA.

px2 R-Nodes. There are four px2 R-nodes in each PIC, labeled px2[3:0]. The px2 R-nodes pass through two adjacent PICs before being broken. These are used to route nets around the perimeter a distance of two or more PICs.

px1 R-Nodes. Each PIC has four px1 R-nodes, labeled px1[3:0]. The px1 R-nodes are one PIC long and are extended to adjacent PICs by enabling CIPs.

PLC-PIC Routing Resources

There is no direct connection between the inter-PIC R-nodes and the PLC R-nodes. All connections to/from the PLC must be done through the connecting R-nodes which are perpendicular to the ten R-nodes in the PIC. The use of perpendicular and parallel R-nodes will be clearer if the PLC and PIC architectures (Figure 18 and Figure 21) are placed side by side. Seventeen R-nodes in the PLC can be connected to the ten R-nodes in the PIC. The key to Figure 21 appears below.

A. As in the PLCs, the PIC contains a set of R-nodes which run the length (width) of the array. The pxL R-nodes connect in the corners of the array to other pxL R-nodes. The pxL R-nodes also connect to the PIC BIDI and LLDRV R-nodes. As in the PLC xL R-nodes, the pxH R-nodes twist as they propagate through the PICs.

B. The px2[3:0] R-nodes span a length of two PICs before intersecting with a CIP. The CIP allows the length of a path using px2 R-nodes to be extended two PICs.

C. The px1[3:0] R-nodes span a single PIC before intersecting with a CIP. The CIP allows the length of a path using px1 R-nodes to be extended by one PIC.

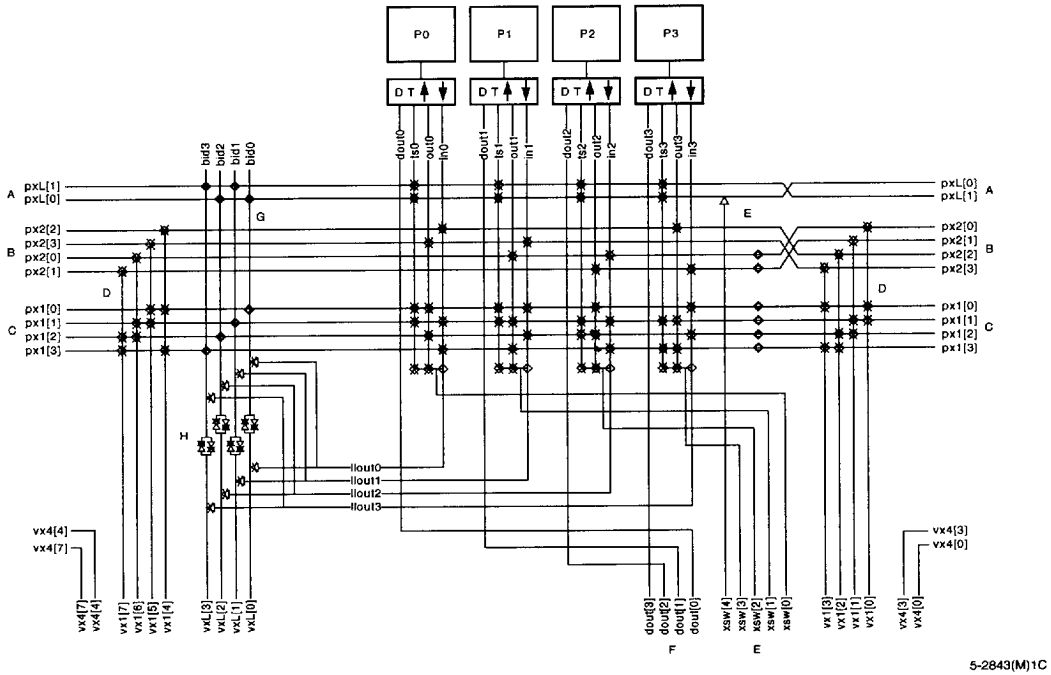


Figure 21. PIC Architecture

Programmable Input/Output Cells
(continued)

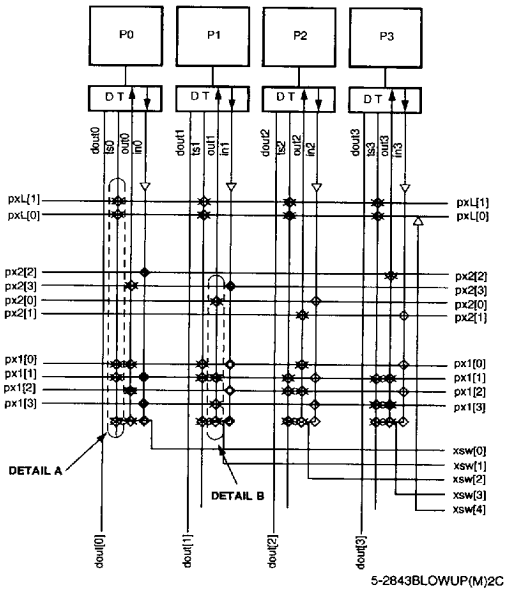


Figure 22. PIC Detail

D. The eight x1 R-nodes of the PLC perpendicular to the PIC (four on each side) can be connected to either the px1 or px2 R-nodes in the PIC. Multiple connections between the PIC px1 R-nodes and the PLC x1 R-nodes are available. These allow buses placed in any arbitrary order on the I/O pads to be unscrambled when placed on the PLC x1 R-nodes. Connections are also available between the PIC px2 R-nodes and the PLC x1 R-nodes.

E. The PLC switching R-nodes can be connected on the side adjacent to the PIC. The out[3:0], ts[3:0], and in[3:0] signals for each I/O pad can be routed directly to the PLC switching R-nodes. The switching R-nodes can also be used to drive a signal onto one of the pxL R-nodes through a long line driver.

F. The PIC also has four dedicated direct output R-nodes connected to the I/O buffers. The direct R-nodes allow signals to go directly from a PLC latch/FF to an output buffer, minimizing the latch/FF to pad propagation delay.

G. The four xL R-nodes of the PLC perpendicular to the PIC can be connected to either the px1 or pxL R-nodes in the PIC. These connections are made through programmable TRIDIs. There is also the fast connection from the I/O pads to the xL R-nodes.

H. The four tridirectional (TRIDI) buffers in each PIC can do the following:

- Drive a signal from an I/O pad onto one of the adjacent PLC's xL R-nodes
- Drive a signal from an I/O pad onto one of the two pxL R-nodes in the PIC
- Drive a signal from the PLC xL R-nodes onto one of the two pxL R-nodes in the PIC
- Drive a signal from the PIC pxL R-nodes onto one of the PLC xL R-nodes

Figure 22 shows paths to and from pads and the use of MUX CIPs to connect R-nodes. Detail A shows five MUX CIPs for the pad P0 used to construct the net for the 3-state signal. In the MUX CIP, one of five R-nodes is connected to an R-node to form the net. In this case, the ts0 signal can be driven by either of the two pxLs, px1[0], px1[1], or the xsw[0] R-nodes. Detail B shows the four MUX CIPs used to drive the P1 output. The source R-node for out1 is either xsw[1], px1[1], px1[3], or px2[2].

Programmable Corner Cells

The programmable corner cell (PCC) contains the circuitry to connect the routing of the two PICs in each corner of the device. The PIC px1 and px2 R-nodes are directly connected together from one PIC to another. The PIC pxL R-nodes are connected from one block to another through tridirectional buffers.

In addition to routing functions, special-purpose functions are located in each FPGA corner. The upper-left PCC contains connections to the boundary-scan logic. The upper-right PCC contains connections to the readback logic. The lower-left PCC contains connections to the internal oscillator.

The lower-right PCC contains connections to the start-up and global reset logic. The global set/reset signal (gsrn) can either be disabled (the default), directly connected to the $\overline{\text{RESET}}$ input pad, or sourced by a lower-right corner signal. If the $\overline{\text{RESET}}$ input pad is not used as a global reset after configuration, this pad can be used as a normal input pad.

During start-up, the release of the global set/reset, the release of the I/Os, and the release of the external DONE signal can each be timed individually based upon the start-up clock. The start-up clock can come from CCLK or it can be routed into the start-up block using the lower-right corner routing resources.

FPGA States of Operation

Prior to becoming operational, the FPGA goes through a sequence of states, including initialization, configuration, and start-up. This section discusses these three states. Figure 23 outlines the FPGA states.

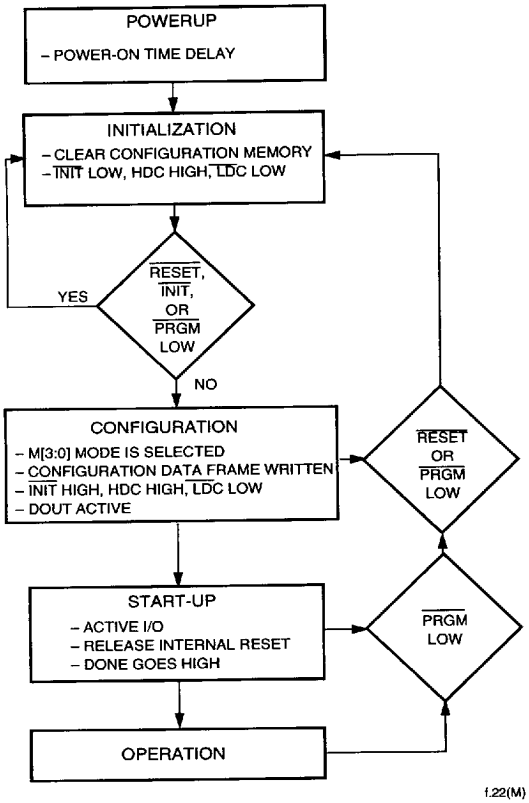


Figure 23. FPGA States of Operation

Initialization

Upon powerup, the device goes through an initialization process. First, an internal power-on-reset circuit is triggered when power is applied. When VDD reaches the voltage at which portions of the FPGA begin to operate (2.5 V to 3.0 V), the I/Os are configured based on the configuration mode, as determined by the mode select inputs M[2:0]. A time-out delay is initiated when VDD reaches between 3.0 V and 4.0 V to allow the power supply voltage to stabilize. The $\overline{\text{INIT}}$ and DONE outputs are low. At powerup, if VDD does not rise from 2.0 V to VDD in less than 25 ms, the user should delay configuration by inputting a low into $\overline{\text{INIT}}$, $\overline{\text{PRGM}}$, or $\overline{\text{RESET}}$ until VDD is greater than the recommended minimum operating voltage (4.75 V for commercial devices).

At the end of initialization, the default configuration option is that the configuration RAM is written to a low state. This prevents shorts prior to configuration. As a configuration option, after the first configuration, the user can reconfigure without clearing the internal configuration RAM first.

The active-low, open-drain initialization signal $\overline{\text{INIT}}$ is released and must be pulled high by an external resistor when initialization is complete. To synchronize the configuration of multiple FPGAs, one or more $\overline{\text{INIT}}$ pins should be wire-ANDed. If $\overline{\text{INIT}}$ is held low by one or more FPGAs or an external device, the FPGA remains in the initialization state. $\overline{\text{INIT}}$ can be used to signal that the FPGAs are not yet initialized. After $\overline{\text{INIT}}$ goes high for two internal clock cycles, the mode lines are sampled and the FPGA enters the configuration state.

The high during configuration (HDC), low during configuration ($\overline{\text{LDC}}$), and DONE signals are active outputs in the FPGA's initialization and configuration states. HDC, $\overline{\text{LDC}}$, and DONE can be used to provide control of external logic signals such as reset, bus enable, or PROM enable during configuration. For parallel master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

FPGA States of Operation (continued)

If configuration has begun, an assertion of $\overline{\text{RESET}}$ or $\overline{\text{PRGM}}$ initiates an abort, returning the FPGA to the initialization state. The $\overline{\text{PRGM}}$ and $\overline{\text{RESET}}$ pins must be pulled back high before the FPGA will enter the configuration state. During the start-up and operating states, only the assertion of $\overline{\text{PRGM}}$ will cause a reconfiguration.

In the master configuration modes, the FPGA is the source of configuration clock (CCLK). In this mode, the initialization state is extended. This is to ensure that in daisy-chain operation, all daisy-chained slave devices are ready. Independent of differences in clock rates, master mode devices remain in the initialization state an additional six internal clock cycles after $\overline{\text{INIT}}$ goes high.

When configuration is initiated, a counter in the FPGA is set to 0 and begins to count configuration clock cycles applied to the FPGA. As each configuration data frame is supplied to the FPGA, it is internally assembled into data words. Each data word is loaded into the internal configuration memory. The configuration loading process is complete when the internal length count equals the loaded length count in the length count field, and the required end of configuration frame is written.

All I/Os operate as TTL inputs during configuration. All I/Os that are not used during the configuration process are 3-stated with internal pull-ups. During configuration, the PLC latch/FFs are held set/reset and the internal BIDI buffers are 3-stated. The TRIDIs in the PIC are not 3-stated. The combinatorial logic begins to function as the FPGA is configured. Figure 24 shows the general waveform of the initialization, configuration, and start-up states.

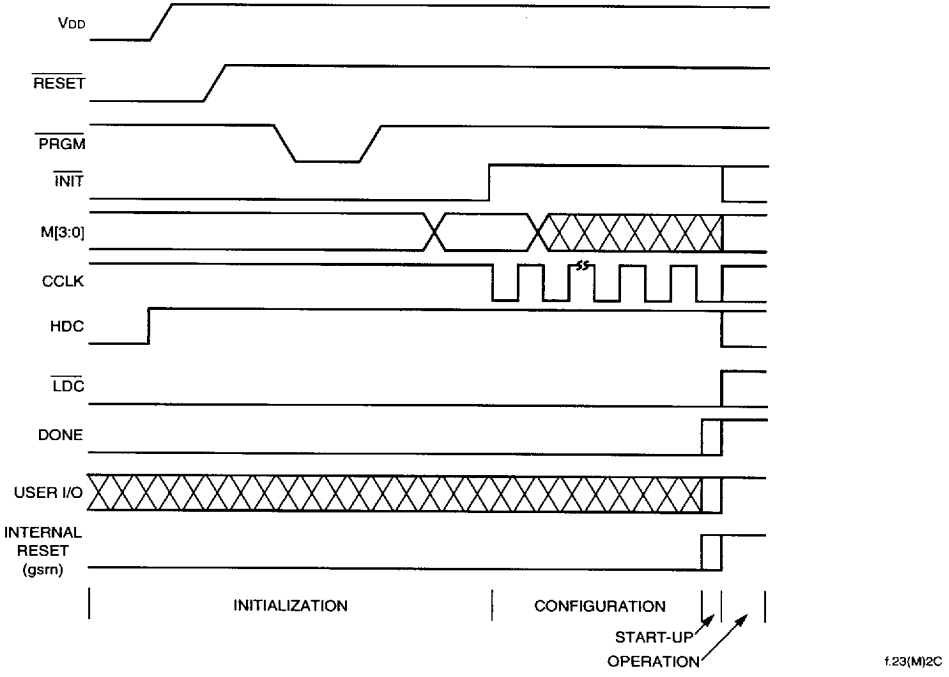


Figure 24. Initialization/Configuration/Start-Up Waveform

FPGA States of Operation (continued)

Configuration

The *ORCA* Series FPGA functionality is determined by the state of internal configuration RAM. This configuration RAM can be loaded in a number of different modes. In these configuration modes, the FPGA can act as a master or a slave of other devices in the system. The decision as to which configuration mode to use is a system design issue. The next section discusses configuration in detail, including the configuration data format and the configuration modes used to load the configuration data in the FPGA.

2

Start-Up

After configuration, the FPGA enters the start-up phase. This phase is the transition between the configuration and operational states.

This begins when the number of CCLKs received after $\overline{\text{INIT}}$ goes high is equal to the value of the length count field in the configuration frame and when the end of configuration frame has been written. The system design issue in the start-up phase is to ensure the user I/Os become active without inadvertently activating devices in the system or causing bus contention. A second system design concern is the timing of the release of global set/reset of the PLC latches/FFs.

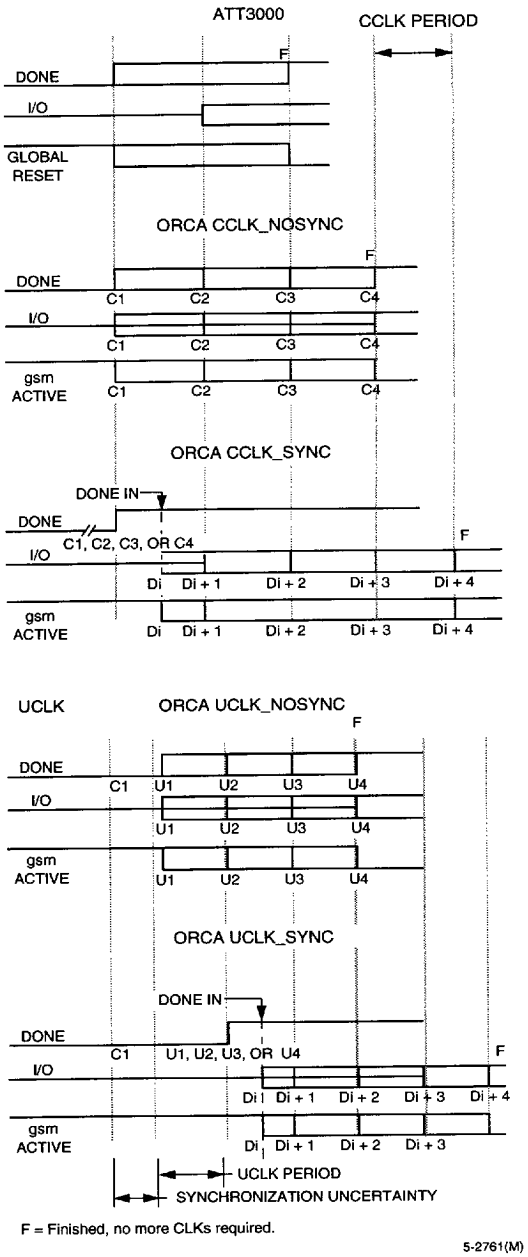


Figure 25. Start-Up Waveform

FPGA States of Operation (continued)

There are configuration options which control the relative timing of three events: DONE going high, release of the set/reset of internal FFs, and user I/Os becoming active. Figure 25 shows the start-up timing for both the *ORCA* and ATT3000 Series FPGAs.

The system designer determines the relative timing of the I/Os becoming active, DONE going high, and the release of the set/reset of internal FFs. In the *ORCA* Series FPGA, the three events can occur in any arbitrary sequence. This means that they can occur before or after each other, or they can occur simultaneously.

The default is for DONE to go high first. This allows configuration sources to be disconnected so that there is no bus contention when the I/Os become active in later cycles. The FFs are set/reset one cycle after DONE goes high so that operation begins in a known state.

The DONE output is an open drain and may include an optional internal pull-up resistor to accommodate wired ANDing. The open-drain DONE outputs from multiple FPGAs can be ANDed and used as an active-high ready signal, an active-low PROM enable, or a reset to other portions of the system.

There is also a synchronous start-up mode where start-up does not begin until DONE goes high. The enabling of the FPGA outputs and the set/reset of the internal flip-flops can be triggered or delayed from the rising edge of DONE. Start-up can be delayed by holding the DONE signal low in the synchronous start-up mode. If the DONE signals of multiple FPGAs are tied together, with all in the synchronous start-up mode, start-up does not begin until all of the FPGAs are configured.

Normally, the three events are triggered by CCLK. As a configuration option, the three events can be triggered by a user clock, UCLK. This allows start-up to be synchronized by a known system clock. When the user clock option is enabled, the user can still hold DONE low to delay start-up. This allows the synchronization of the start-up of multiple FPGAs.

In addition to controlling the FPGA during start-up, additional start-up techniques to avoid contention include using isolation devices between the FPGA and other circuits in the system, reassigning I/O locations, and maintaining I/Os as 3-stated outputs until contentions are resolved.

Reconfiguration

To reconfigure the FPGA when the device is operating in the system, a low pulse is input into $\overline{\text{PRGM}}$. The configuration data in the FPGA is cleared and the I/Os not used for configuration are 3-stated. The FPGA then samples the mode select inputs and begins reconfiguration. When reconfiguration is complete, DONE is released, allowing it to be pulled high.

Configuration Data Format

This section discusses using *ORCA* Foundry to generate configuration RAM data and then provides the details of the configuration frame format.

Using *ORCA* Foundry to Generate Configuration RAM Data

The configuration data defines the I/O functionality, logic, and interconnections. The bit stream is generated by the *ORCA* Foundry Development System. The bit stream created by the bit stream generation tool is a series of 1s and 0s used to write the FPGA configuration RAM. The bit stream can be loaded into the FPGA using one of the configuration modes discussed later. In the bit stream generator, the designer selects options which affect the FPGA's functionality. Using the output of the bit stream generator, circuit.bit, the development system's download tool can load the configuration data into the *ORCA* series FPGA evaluation board from a PC or workstation. Alternately, a user can program a PROM (such as the ATT1700 Series Serial ROMs or standard EPROMs) and load the FPGA from the PROM. *ORCA* Foundry's PROM programming tool produces a file in .mks or .exo format.

Configuration Data Frame

A detailed description of frame format and contents is shown in Figure 26. The header frame begins with a series of 1s and a preamble of 0010, followed by a 24-bit length count field representing the total number of configuration clocks needed to complete loading of the FPGA(s). The configuration data follows, in frames, with each frame starting with 0 and ending with one or more high stop bits. The data frames can be transmitted in a compressed or uncompressed format. This is determined in the data frame by the compression bit, which follows the program bit. Multiple FPGAs can be loaded using a single bit stream. The FPGAs do not have to be the same size.

The length and number of data frames and information about the PROM size for ATT1C03, ATT1C05, ATT1C07, and ATT1C09 FPGAs are given in Table 6.

Table 6. Configuration Frame Size

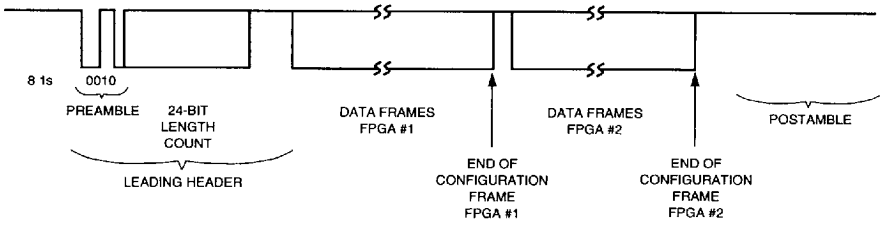
Device	1C03	1C05	1C07	1C09
# of Frames	446	530	614	698
Data Bits/Frame	96	114	132	150
Configuration Data (# of frames x # of data bits/frame)	42,816	60,420	81,048	104,700
Max Total # Bits/ Frame (align bits, 1 write bit, 8 stop bits)	128	144	160	176
Max Configuration Data (# bits x # of frames)	57,088	76,320	98,240	122,848
Max PROM Size (bits) (add 40-bit header and 16-bit end of configuration frame)	57,144	76,376	98,296	122,904

The data frames for ATT1C03, ATT1C05, ATT1C07, and ATT1C09 are given in Table 7. An alignment field is required in the slave parallel mode. The alignment field is a series of 0s: seven for ATT1C03, five for ATT1C05, three for ATT1C07, and one for ATT1C09. The alignment field is not required in any other mode.

Table 7. Compressed and Uncompressed Frames

Configuration Data Frame	
ATT1C03	
Uncompressed	010[addr12:0] [A]1[Data95:0]111
Compressed	011[addr12:0]111
ATT1C05	
Uncompressed	010[addr12:0] [A]1[Data113:0]111
Compressed	011[addr12:0]111
ATT1C07	
Uncompressed	010[addr12:0] [A]1[Data131:0]111
Compressed	011[addr12:0]111
ATT1C09	
Uncompressed	010[addr12:0] [A]1[Data149:0]111
Compressed	011[addr12:0]111

Configuration Data Format (continued)



f.24(M)1C

Figure 26. Serial Configuration Data Format

Header	11111111	Leading header — 4 bits minimum dummy bits
	0010	Preamble
	24-Bit Length Count	Configuration frame length
	1111	Trailing header — 4 bits minimum dummy bits
Configuration Data Frame (repeated for each data frame)	0	Frame start
	P - 1 or 0	1 indicates data frame; 0 indicates all frames are written
	C - 1 or 0	Uncompressed — 0 indicates data and address are supplied
		Compressed — 1 indicates only address is supplied
	Addr[12:0]	Column address in FPGA to be written
	A	Alignment bit (different number of 0s needed for each part)
	1	Write bit — used in uncompressed data frame
	Data Bits	Needed only in an uncompressed data frame
	.	.
	.	.
	1	One or more stop bits (high) to separate frames
End of Configuration	0011111111111111	16 bits minimum — 00 indicates all frames are written
Postamble	111111 . . .	Additional 1s

Note: For slave parallel mode, the byte containing the preamble must be 11110010. The number of leading header dummy bits must be (n * 8) + 4, where n is any nonnegative integer and the number of trailing dummy bits must be (n * 8), where n is any positive integer. The number of stop bits/frame for slave parallel mode must be (x * 8), where x is a positive integer. Note also that the bit stream generator tool supplies a bit stream which is compatible to all configuration modes, including slave parallel mode.

Figure 27. Configuration Frame Format and Contents

FPGA Configuration Modes

There are eight methods of configuring the FPGA. Seven of the configuration modes are selected on the M0, M1, and M2 inputs. The eighth configuration mode is accessed through the boundary-scan interface. A fourth input, M3, is used to select the frequency of the internal oscillator, which is the source for CCLK in some configuration modes. The nominal frequencies of the internal oscillator are 1.25 MHz and 10 MHz. The 1.25 MHz frequency is selected when the M3 input is unconnected or driven to a high state.

2

There are three basic FPGA configuration modes: master, slave, and peripheral. The configuration data can be transmitted to the FPGA serially or in parallel bytes. As a master, the FPGA provides the control signals out to strobe data in. As a slave device, a clock is generated externally and provided into CCLK. In the peripheral mode, the FPGA acts as a microprocessor peripheral. Table 8 lists the functions of the configuration mode pins.

Table 8. Configuration Modes

M2	M1	M0	CCLK	Configuration Mode	Data
0	0	0	Output	Master	Serial
0	0	1	Input	Slave Parallel	Parallel
0	1	0	Reserved		
0	1	1	Input	Sync Peripheral	Parallel
1	0	0	Output	Master (up)	Parallel
1	0	1	Output	Async Peripheral	Parallel
1	1	0	Output	Master (down)	Parallel
1	1	1	Input	Slave	Serial

Master Parallel Mode

The master parallel configuration mode is generally used to interface to industry-standard byte-wide memory such as the 2764 and larger EPROMs. Figure 28 provides the connections for master parallel mode. The FPGA outputs an 18-bit address on A[17:0] to memory and reads one byte of configuration data on the rising edge of RCLK. The parallel bytes are internally serialized starting with the least significant bit, D0.

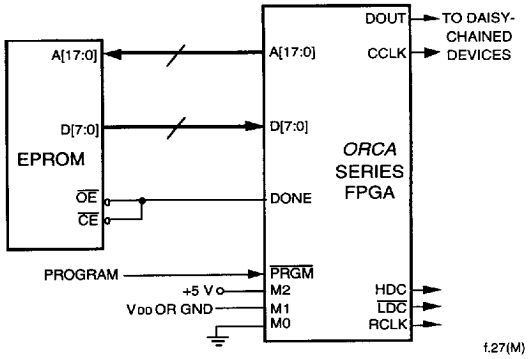


Figure 28. Master Parallel Configuration Schematic

There are two parallel master modes: master up and master down. In master up, the starting memory address is 00000 Hex and the FPGA increments the address for each byte loaded. In master down, the starting memory address is 3FFFF Hex and the FPGA decrements the address for each byte loaded.

One master mode FPGA can interface to the memory and provide configuration data on DOUT to additional FPGAs in a daisy chain. The configuration data on DOUT is provided synchronously with the falling edge of CCLK. The frequency of the CCLK output is eight times that of RCLK.

FPGA Configuration Modes (continued)

Master Serial Mode

In the master serial mode, the FPGA loads the configuration data from an external serial ROM. The configuration data is either loaded automatically at start-up or on a $\overline{\text{PRGM}}$ command to reconfigure. The ATT1700 Series can be used to configure the FPGA in the master serial mode. This provides a simple four-pin interface in an eight-pin package. The ATT1736, ATT1765, and ATT17128 serial ROMs store 32K, 64K, and 128K bits, respectively.

Configuration in the master serial mode can be done at powerup and/or upon a configure command. The system or the FPGA must activate the serial ROM's RESET/OE and $\overline{\text{CE}}$ inputs. At powerup, the FPGA and serial ROM each contain internal power-on reset circuitry which allows the FPGA to be configured without the system providing an external signal. The power-on reset circuitry causes the serial ROM's internal address pointer to be reset. After powerup, the FPGA automatically enters its initialization phase.

The serial ROM/FPGA interface used depends on such factors as the availability of a system reset pulse, availability of an intelligent host to generate a configure command, whether a single serial ROM is used or multiple serial ROMs are cascaded, whether the serial ROM contains a single or multiple configuration programs, etc. Because of differing system requirements and capabilities, a single FPGA/serial ROM interface is generally not appropriate for all applications.

Data is read in the FPGA sequentially from the serial ROM. The DATA output from the serial ROM is connected directly into the DIN input of the FPGA. The CCLK output from the FPGA is connected to the CLOCK input of the serial ROM. During the configuration process, CCLK clocks one data bit on each rising edge.

Since the data and clock are direct connects, the FPGA/serial ROM design task is to use the system or FPGA to enable the RESET/OE and $\overline{\text{CE}}$ of the serial ROM(s). There are several methods for enabling the serial ROM's RESET/OE and $\overline{\text{CE}}$ inputs. The serial ROM's RESET/OE is programmable to function with RESET active-high and OE active-low or RESET active-low and OE active-high.

In Figure 29, serial ROMs are cascaded to configure multiple daisy-chained FPGAs. The host generates a 500 ns low pulse into the FPGA's $\overline{\text{PRGM}}$ input and into the serial ROMs' $\overline{\text{RESET}}$/OE input, which has been programmed to function with RESET active-low and OE active-high. The FPGA DONE is routed to the $\overline{\text{CE}}$ pin. The low on DONE enables the serial ROMs. At the completion of configuration, the high on the FPGA's DONE disables and resets the ROM's address pointers.

Serial ROMs can also be cascaded to support the configuration of multiple FPGAs or to load a single FPGA when configuration data requirements exceed the capacity of a single serial ROM. After the last bit from the first serial ROM is read, the serial ROM outputs $\overline{\text{CEO}}$ low and 3-states the DATA output. The next serial ROM recognizes the low on $\overline{\text{CE}}$ input and outputs configuration data on the DATA output. After configuration is complete, the FPGA's DONE output into $\overline{\text{CE}}$ disables the serial ROMs.

This FPGA/serial ROM interface is not used in applications in which a serial ROM stores multiple configuration programs. In these applications, the next configuration program to be loaded is stored at the ROM location that follows the last address for the previous configuration program. The reason the interface in Figure 28 will not work in this application is that the $\overline{\text{PRGM}}$ signal would reset the serial ROM address pointer, causing the first configuration to be reloaded.

In some applications, there can be contention on the FPGA's DIN pin. During configuration, DIN receives configuration data, and after configuration, it is a user I/O at start-up. If there is contention, an early DONE (selected in *ORCA* Foundry) may correct the problem. An alternative is to use $\overline{\text{LDC}}$ to drive the serial ROM's $\overline{\text{CE}}$ pin.

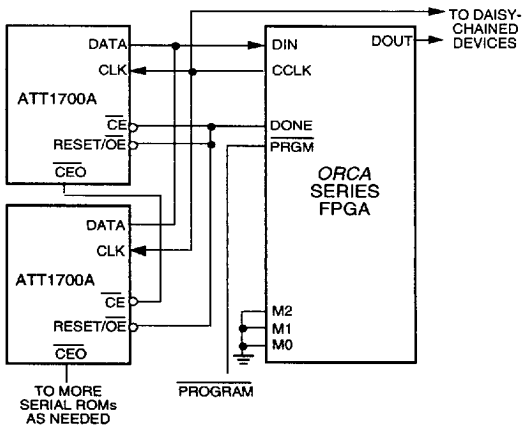


Figure 29. Master Serial Configuration Schematic

FPGA Configuration Modes (continued)

Asynchronous Peripheral Mode

Figure 30 shows the connections needed for the asynchronous peripheral mode. In this mode, the FPGA system interface is similar to that of a microprocessor-peripheral interface. The microprocessor generates the control signals to write an 8-bit byte into the FPGA. The FPGA control inputs include active-low $\overline{CS0}$ and active-high CS1 chip selects and a write $\overline{WR}$ input. The chip selects can be cycled or maintained at a static level during the configuration cycle. Each byte of data is written into the FPGA's D[7:0] input pins.

The FPGA provides a RDY/$\overline{BUSY}$ status output to indicate that another byte can be loaded. A low on RDY/$\overline{BUSY}$ indicates that the double-buffered hold/shift registers are not ready to receive data. The shortest time RDY/$\overline{BUSY}$ is low occurs when a byte is loaded into the hold register and the shift register is empty, in which case the byte is immediately transferred to the shift register. The longest time for RDY/$\overline{BUSY}$ to remain low occurs when a byte is loaded into the holding register and the shift register has just started shifting configuration data into configuration RAM. The RDY/$\overline{BUSY}$ status is also available on the D7 pin by enabling the chip selects, setting $\overline{WR}$ high, and setting $\overline{RD}$ low.

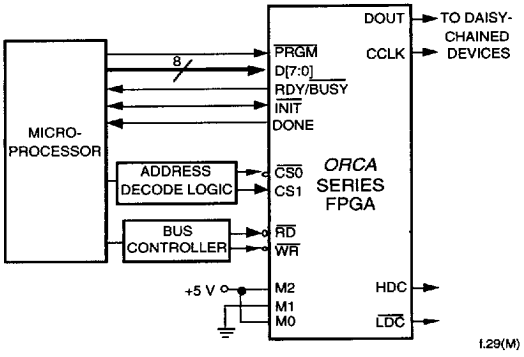


Figure 30. Asynchronous Peripheral Configuration Schematic

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after $\overline{INIT}$ goes high. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The RDY/$\overline{BUSY}$ signal is an output which acts as an acknowledge. RDY/$\overline{BUSY}$ goes high one CCLK after data is clocked and after one CCLK cycle, it returns low. The process repeats until all of the data is loaded into the FPGA. The data begins shifting on DOUT 1.5 cycles after it is loaded in parallel. It requires additional CCLKs after the last byte is loaded to complete the shifting. Figure 31 shows the connections for synchronous peripheral mode.

As with master modes, the peripheral modes can be used as the lead FPGA for a daisy chain of slave FPGAs.

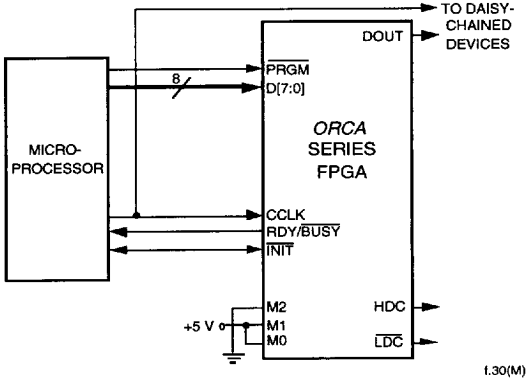


Figure 31. Synchronous Peripheral Configuration Schematic

FPGA Configuration Modes (continued)

Slave Serial Mode

The slave serial mode is primarily used when multiple FPGAs are configured in a daisy chain. The serial slave serial mode is also used on the FPGA evaluation board which interfaces to the download cable. A device in the slave serial mode can be used as the lead device in a daisy chain. Figure 32 shows the connections for the slave serial configuration mode.

The configuration data is provided into the FPGA's DIN input synchronous with the configuration clock CCLK input. After the FPGA has loaded its configuration data, it retransmits the incoming configuration data on DOUT. CCLK is routed into all slave serial mode devices in parallel.

Multiple slave FPGAs can be loaded with identical configurations simultaneously. This is done by loading the configuration data into the DIN inputs in parallel.

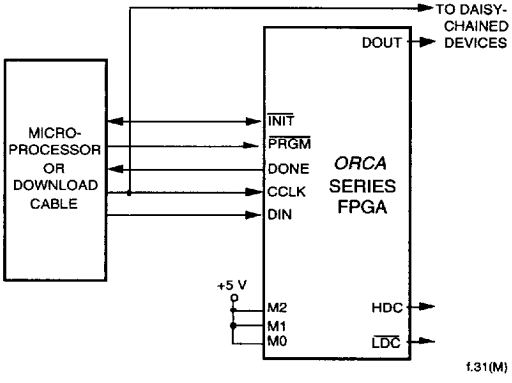


Figure 32. Slave Serial Configuration Schematic

Slave Parallel Mode

The slave parallel mode is essentially the same as the slave serial mode except that 8 bits of data are input on pins D[7:0] for each CCLK cycle. Due to 8 bits of data being input per CCLK cycle, the DOUT pin does not contain a valid bit stream for slave parallel mode. As a result, the lead device cannot be used in the slave parallel mode in a daisy-chain configuration.

Multiple slave FPGAs can be loaded with identical configurations simultaneously. This is done by loading the configuration data into the D[7:0] inputs in parallel. Figure 33 is a schematic of the connections for the slave parallel configuration mode. $\overline{WR}$ and $\overline{CS0}$ are active-low chip select signals, and CS1 is an active-high chip select signal.

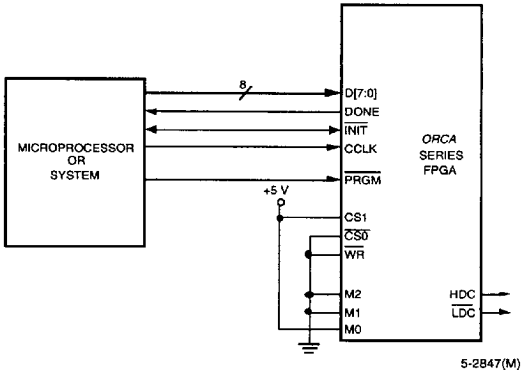


Figure 33. Slave Parallel Configuration Schematic

FPGA Configuration Modes (continued)

Daisy Chain

Multiple FPGAs can be configured by using a daisy chain of the FPGAs. Daisy chaining uses a lead FPGA and one or more FPGAs configured in slave serial mode. The lead FPGA can be configured in any mode except slave parallel mode. (Daisy chaining is not available with the boundary-scan ram_w instruction, as discussed later.)

2

All daisy-chained FPGAs are connected in series. Each FPGA reads and shifts the preamble and length count in on positive CCLK and out on negative CCLK edges.

An upstream FPGA which has received the preamble and length count outputs a high on DOUT until it has received the appropriate number of data frames so that downstream FPGAs do not receive frame start bits (0s). After loading and retransmitting the preamble and length count to a daisy chain of slave devices, the lead device loads its configuration data frames. The loading of configuration data continues after the lead device has received its configuration data if its internal frame bit counter has not reached the length count. When the configuration RAM is full and the number of bits received is less than the length count field, the FPGA shifts any additional data out on DOUT.

The configuration data is read into DIN of slave devices on the positive edge of CCLK, and shifted out DOUT on the negative edge of CCLK. Figure 34 shows the connections for loading multiple FPGAs in a daisy-chain configuration.

The generation of CCLK for the daisy-chained devices which are in slave serial mode differs depending on the configuration mode of the lead device. A master parallel mode device uses its internal timing generator to produce an internal CCLK at 8 times its memory address rate (RCLK). The asynchronous peripheral mode device outputs eight CCLKs for each write cycle. If the lead device is configured in either synchronous peripheral or a slave mode, CCLK is routed to the lead device and to all of the daisy-chained devices.

The *ORCA* Foundry Development System can create a composite configuration bit stream for configuring daisy-chained FPGAs. The frame format is a preamble, a length count for the total bit stream, multiple concatenated data frames, an end-of-configuration frame per device, a postamble, and an additional fill bit per device in the serial chain.

As seen in Figure 34, the $\overline{\text{INIT}}$ pins for all of the FPGAs are connected together. This is required to guarantee that powerup and initialization will work correctly. In general, the DONE pins for all of the FPGAs are also connected together as shown to guarantee that all of the FPGAs enter the start-up state simultaneously. This may not be required, depending upon the start-up sequence desired.

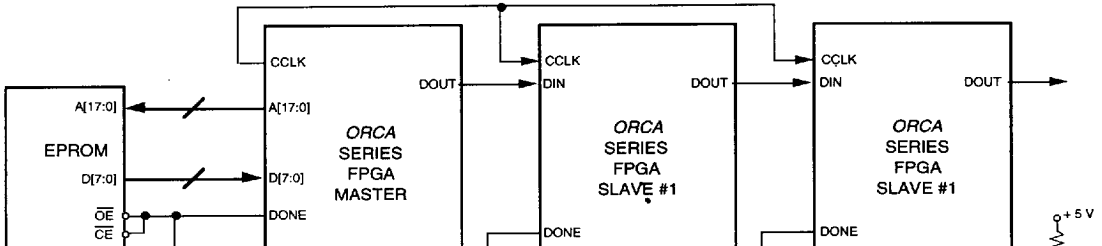


Figure 34. Daisy-Chain Configuration Schematic

Readback

Readback is used to read back the configuration data and, optionally, the state of the PFU outputs. A readback operation can be done while the FPGA is in normal system operation. The readback operation cannot be daisy chained. To use readback, the user selects options in the bit stream generator in the development system.

Table 9 provides readback options selected in the bit stream generator tool. The table provides the number of times that the configuration data can be read back. This is intended primarily to give the user control over the security of the FPGA's configuration program. The user can prohibit readback (0), allow a single readback (1), or allow unrestricted readback (U).

The pins used for readback are readback data (RD_DATA), read configuration ($\overline{\text{RD\_CFGN}}$), and configuration clock (CCLK). A readback operation is initiated by a high-to-low transition on $\overline{\text{RD\_CFGN}}$. The $\overline{\text{RD\_CFGN}}$ input must remain low during the readback operation. The readback operation can be restarted at frame 0 by setting the $\overline{\text{RD\_CFGN}}$ pin high, applying at least two rising edges of CCLK, and then applying $\overline{\text{RD\_CFGN}}$ low again. One bit of data is shifted out on RD_DATA on the rising edge of CCLK. The first start bit of the readback frame is transmitted out on the first rising edge of CCLK after $\overline{\text{RD\_CFGN}}$ is input low.

The readback frame contains the configuration data and the state of the internal logic. During readback, the value of all five PFU outputs can be captured. The following options are allowed when doing a capture of the PFU outputs:

1. Do not capture data (the data written to the RAMs, usually 0, will be read back).
2. Capture data upon entering readback.
3. Capture data based upon a configurable signal internal to the FPGA. If this signal is tied to logic 0, capture RAMs are written continuously, which is equivalent to ATT3000 series capture.
4. Capture data on either options 2 or 3 above.

The readback frame has a similar, but not identical, format to the configuration frame. This eases a bitwise comparison between the configuration and readback data. The readback data is not inverted. Every data frame has one low start bit and one high stop bit. The preamble, including the length count field, is not part of the readback frame. The readback frame contains states in locations not used in the configuration. These locations need to be masked out when comparing the configuration and readback frames. The development system optionally provides a readback bit steam to compare to readback data from the FPGA.

Table 9. Readback Options

Option	Function
0	Inhibit Readback
1	Allow One Readback Only
U	Allow Unrestricted Number of Readbacks

Boundary Scan

The increasing complexity of integrated circuits (ICs) and IC packages has increased the difficulty of testing printed-circuit boards (PCBs). To address this testing problem, the *IEEE* standard 1149.1-1990 (*IEEE* Standard Test Access Port and Boundary-Scan Architecture) is implemented in the *ORCA* series of FPGAs. It allows users to efficiently test the interconnection between integrated circuits on a PCB, as well as test the integrated circuit itself. The *IEEE* 1149.1 standard is a well-defined protocol that ensures interoperability among boundary-scan (BSCAN) equipped devices from different vendors.

The *IEEE* 1149.1 standard defines a test access port (TAP) that consists of a 4-pin interface with an optional reset pin for boundary-scan testing of integrated circuits in a system. The *ORCA* Series FPGA provides four interface pins: test data in (TDI), test mode select (TMS), test clock (TCK), and test data out (TDO). The $\overline{\text{PRGM}}$ pin used to reconfigure the device also resets the boundary-scan logic. The user test host serially loads test commands and test data into the FPGA through these pins to drive outputs and examine inputs. In the configuration shown in Figure 35, where boundary scan is used to test ICs, test data is transmitted serially into TDI of the first BSCAN device (U1), through TDO/TDI connections between BSCAN devices (U2 and U3), and out TDO of the last BSCAN device (U4). In this configuration, the TMS and TCK signals are routed to all boundary-scan ICs in parallel so that all boundary-scan components operate in the same state. In other configurations, multiple scan paths are used instead of a single ring. When multiple scan paths are used, each ring is independently controlled by its own TMS and TCK signals.

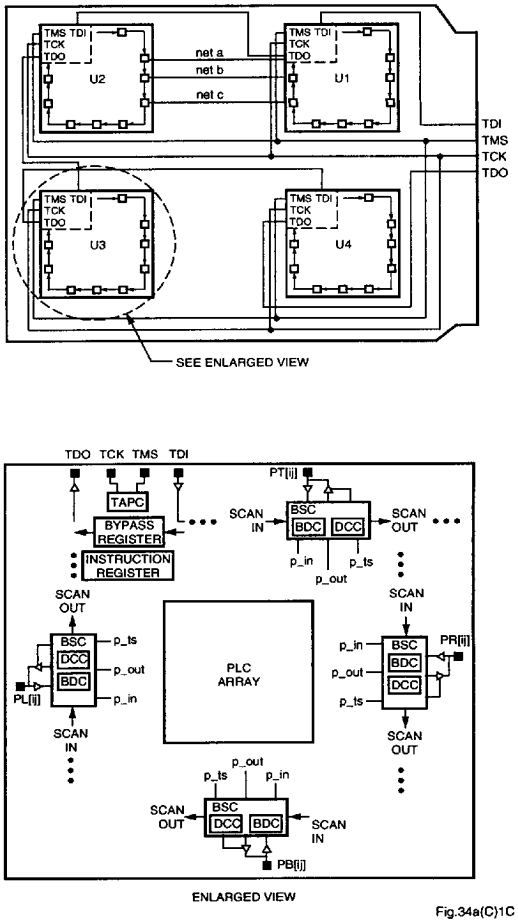


Fig.34a(C)1C

Key: BSC = boundary-scan cell, BDC = bidirectional data cell, and DCC = data control cell.

Figure 35. Printed-Circuit Board with Boundary-Scan Circuitry

Boundary Scan (continued)

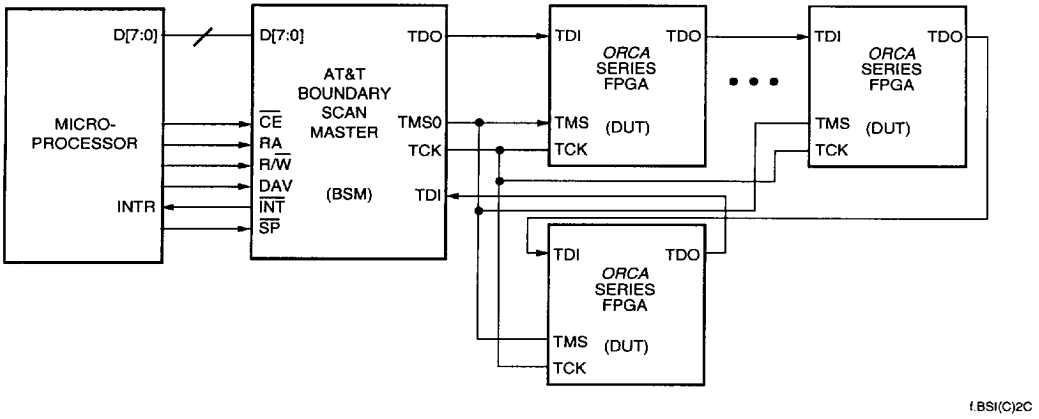


Figure 36. Boundary-Scan Interface

Figure 36 provides a system interface for components used in the boundary-scan testing of PCBs. The three major components shown are the test host, boundary-scan support circuit, and the devices under test (DUTs). The DUTs shown here are *ORCA* series FPGAs with dedicated boundary-scan circuitry. The test host is normally one of the following: automatic test equipment (ATE), a workstation, a PC, or a microprocessor.

The boundary-scan support circuit shown is the AT&T 497AA Boundary-Scan Master (BSM). The BSM offloads tasks from the test host to increase test throughput. To interface between the test host and the DUTs, the BSM has a general microprocessor interface and provides parallel-to-serial/serial-to-parallel conversion, as well as three 8K data buffers. The BSM also increases test throughput with a dedicated automatic test pattern generator and with compression of the test response with a signature analysis register. The PC-based AT&T Boundary-Scan Test card/software allows a user to quickly prototype a boundary-scan test setup.

Boundary-Scan Instructions

The *ORCA* series boundary-scan circuitry is used for three mandatory *IEEE* 1149.1 tests (EXTEST, SAMPLE/PRELOAD, BYPASS) and four AT&T-defined instructions. The 3-bit wide instruction register supports the seven instructions listed in Table 10.

Table 10. *ORCA* Boundary-Scan Instructions

Code	Instruction
000	EXTEST
001	PLC Scan Ring 1
010	RAM Write (RAM_W)
011	Reserved
100	SAMPLE/PRELOAD
101	PLC Scan Ring 2
110	RAM Read (RAM_R)
111	BYPASS

Boundary Scan (continued)

The external test (EXTEST) instruction allows the interconnections between ICs in a system to be tested for opens and stuck-at faults. If an EXTEST instruction is performed for the system shown in Figure 35, the connections between U1 and U2 (shown by nets a, b, and c) can be tested by driving a value onto the given nets from one device and then determining whether the same value is seen at the other device. This is determined by shifting 2 bits of data for each pin (one for the output value and one for the 3-state value) through the BSR until each one aligns to the appropriate pin. Then, based upon the value of the 3-state signal, either the I/O pad is driven to the value given in the BSR, or the BSR is updated with the input value from the I/O pad, which allows it to be shifted out TDO.

The SAMPLE instruction is useful for system debugging and fault diagnosis by allowing the data at the FPGA's I/Os to be observed during normal operation. The data for all of the I/Os is captured simultaneously into the BSR, allowing them to be shifted-out TDO to the test host. Since each I/O buffer in the PICs is bidirectional, two pieces of data are captured for each I/O pad: the value at the I/O pad and the value of the 3-state control signal.

There are four AT&T-defined instructions. The PLC scan rings 1 and 2 (PSR1, PSR2) allow user-defined internal scan paths using the PLC latches/FFs. The RAM_Write Enable (RAM_W) instruction allows the user to serially configure the FPGA through TDI. The RAM_Read Enable (RAM_R) allows the user to read back RAM contents on TDO after configuration.

ORCA Boundary-Scan Circuitry

The *ORCA* Series boundary-scan circuitry includes a test access port controller (TAPC), instruction register (IR), boundary-scan register (BSR), and bypass register. It also includes circuitry to support the four AT&T-defined instructions.

Figure 37 shows a functional diagram of the boundary-scan circuitry that is implemented in the *ORCA* series. The input pins' (TMS, TCK, and TDI) locations vary depending on the part, and the output pin is the dedicated TDO/RD_DATA output pad. Test data in (TDI) is the serial input data. Test mode select (TMS) controls the boundary-scan test access port controller (TAPC). Test clock (TCK) is the test clock on the board.

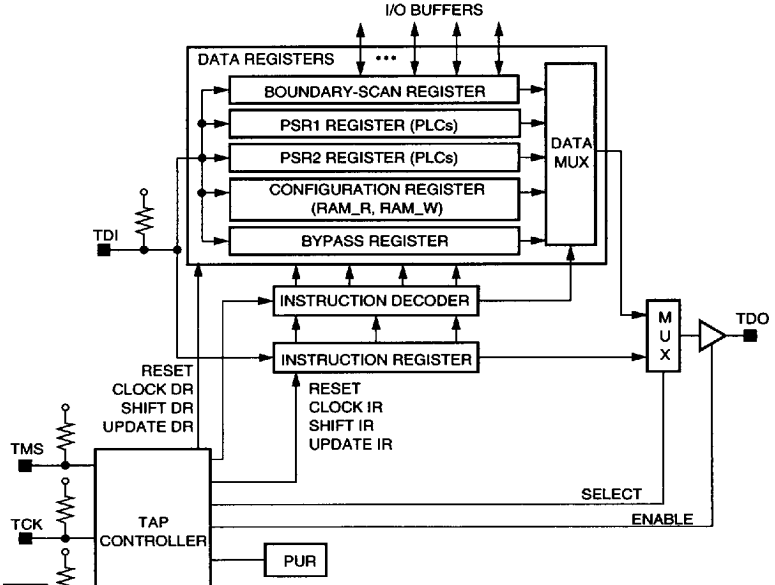


Figure 37. *ORCA* Series Boundary-Scan Circuitry Functional Diagram

Boundary Scan (continued)

The BSR is a series connection of boundary-scan cells (BSCs) around the periphery of the IC. Each I/O pad on the FPGA, except for CCLK, DONE, and the boundary-scan pins (TCK, TDI, TMS, and TDO), is included in the BSR. The first BSC in the BSR (connected to TDI) is located in the first PIC I/O pad on the left of the top side of the FPGA (PTA PIC). The BSR proceeds clockwise around the top, right, bottom, and left sides of the array. The last BSC in the BSR (connected to TDO) is located on the top of the left side of the array (PLA3).

The bypass instruction uses a single FF which resynchronizes test data which is not part of the current scan operation. In a bypass instruction, test data received on TDI is shifted out of the bypass register to TDO. Since the BSR (which requires a two FF delay for each pad) is bypassed, test throughput is increased when devices that are not part of a test operation are bypassed.

The boundary-scan logic is enabled before and during configuration. After configuration, a configuration option determines whether or not boundary-scan logic is used.

The 32-bit boundary-scan identification register contains the manufacturer's ID number, unique part number, and version, but is not implemented in the *ORCA* series of FPGAs. If boundary scan is not used, TMS, TDI, and TCK become user I/Os, and TDO is 3-stated or used in the readback operation.

ORCA Series TAP Controller (TAPC)

The *ORCA* Series TAP controller (TAPC) is a 1149.1 compatible test access port controller. The 16 JTAG state assignments from the *IEEE* 1149.1 specification are used. The TAPC is controlled by TCK and TMS. The TAPC states are used for loading the IR to allow three basic functions in testing: providing test stimuli (Update DR), test execution (Run Test/Idle), and obtaining test responses (Capture DR). The TAPC allows the test host to shift in and out both instructions and test data/results. The inputs and outputs of the TAPC are provided in the table below. The outputs are primarily the control signals to the instruction register and the data register.

Table 11. TAP Controller Input/Outputs

Symbol	I/O	Function
TMS	I	Test Mode Select
TCK	I	Test Clock
PUR	I	Powerup Reset
$\overline{\text{PRGM}}$	I	BSCAN Reset
TRESET	O	Test Logic Reset
Select	O	Select IR (High); Select DR (Low)
Enable	O	Test Data Out Enable
Capture DR	O	Capture/Parallel Load DR
Capture IR	O	Capture/Parallel Load IR
Shift DR	O	Shift Data Register
Shift IR	O	Shift Instruction Register
Update DR	O	Update/Parallel Load DR
Update IR	O	Update/Parallel Load IR

Boundary Scan (continued)

The TAPC generates control signals which allow capture, shift, and update operations on the instruction and data registers. In the capture operation, data is loaded into the register. In the shift operation, the captured data is shifted out while new data is shifted in. In the update operation, either the instruction register is loaded for instruction decode, or the boundary-scan register is updated for control of outputs.

2

The test host generates a test by providing input into the *ORCA* Series TMS input synchronous with TCK. This sequences the TAPC through states in order to perform the desired function on the instruction register or a data register. Figure 38 provides a state diagram of the state transition for the TAPC where the next state is determined by the TMS input value.

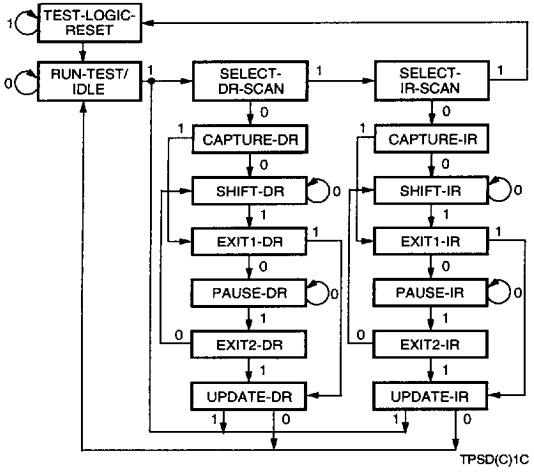


Figure 38. TAP Controller State Transition Diagram

Boundary-Scan Cells

Figure 39 is a diagram of the boundary-scan cell (BSC) in the *ORCA* series PICs. There are four BSCs in each PIC: one for each pad, except as noted above. The BSCs are connected serially to form the BSR. The BSC controls the functionality of the in, out, and 3-state signals for each pad.

The BSC allows the I/O to function in either the normal or test mode. Normal mode is defined as when an output buffer receives input from the PLC array and provides output at the pad or when an input buffer provides input from the pad to the PLC array. In the test mode, the BSC executes a boundary-scan operation, such as shifting in scan data from an upstream BSC in the BSR, providing test stimuli to the pad, capturing test data at the pad, etc.

The primary functions of the BSC are shifting scan data serially in the BSR and observing input (p_in), output (p_out), and 3-state (p_ts) signals at the pads. The BSC consists of two circuits: the bidirectional data cell is used to access the input and output data, and the direction control cell is used to access the 3-state value. Both cells consist of a flip-flop used to shift scan data which feeds a flip-flop to control the I/O buffer. The bidirectional data cell is connected serially to the direction control cell to form a boundary-scan shift register.

Boundary Scan (continued)

The TAPC signals (capture, update, shiftn, treset, and TCK) and the MODE signal control the operation of the BSC. The bidirectional data cell is also controlled by the high out/low in (HOLI) signal generated by the direction control cell. When HOLI is low, the bidirectional data cell receives input buffer data into the BSC. When HOLI is high, the BSC is loaded with functional data from the PLC.

The MODE signal is generated from the decode of the instruction register. When the MODE signal is high (EXTEST), the scan data is propagated to the output buffer. When the MODE signal is low (BYPASS or SAMPLE), functional data from the FPGA's internal logic is propagated to the output buffer.

The boundary-scan description language (BSDL) is provided for each device in the ORCA series of FPGAs. The BSDL is generated from a device profile, pinout, and other boundary-scan information.

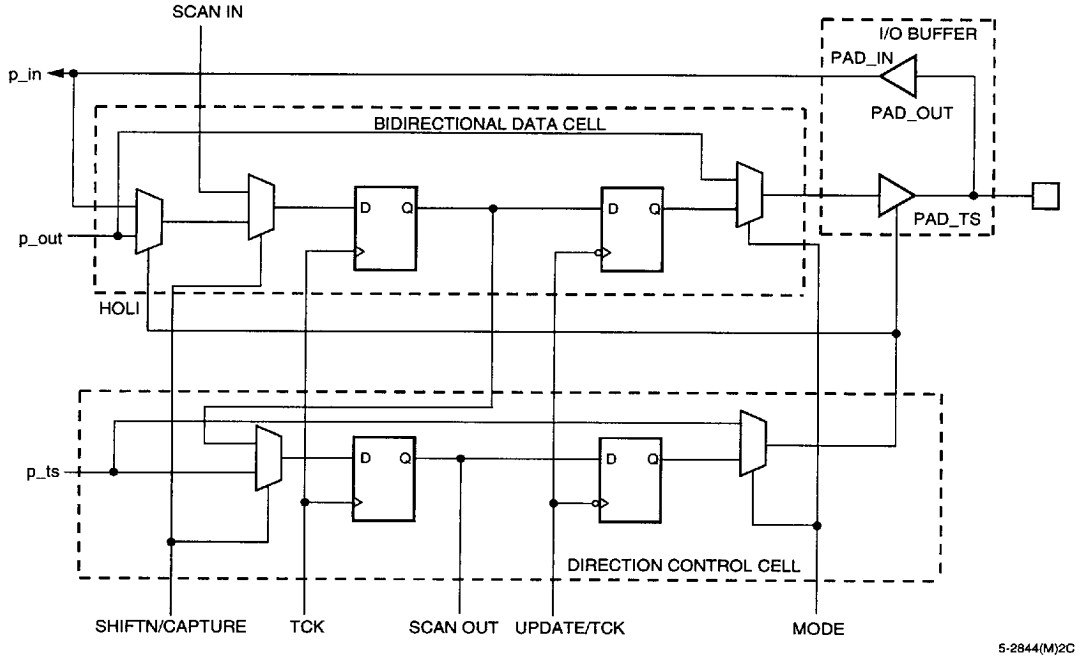


Figure 39. Boundary-Scan Cell

Boundary Scan (continued)

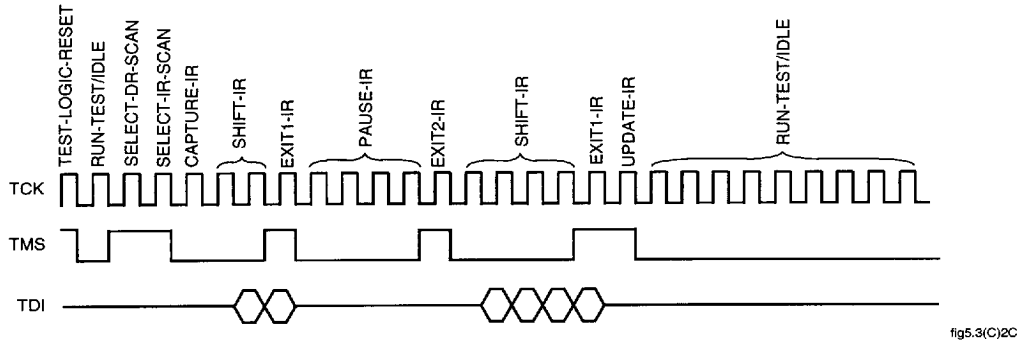


Figure 40. Instruction Register Scan Timing Diagram

Boundary-Scan Timing

To ensure race-free operation, data changes on specific clock edges. The TMS and TDI inputs are clocked in on the rising edge of TCK, while changes on TDO occur on the falling edge of TCK. In the execution of an EXTEST instruction, parallel data is output from the BSR to the FPGA pads on the falling edge of TCK. The maximum frequency allowed for TCK is 10 MHz.

Figure 40 shows timing waveforms for an instruction scan operation. The diagram shows the use of TMS to sequence the TAPC through states. The test host (or BSM) changes data on the falling edge of TCK, and it is clocked into the DUT on the rising edge.

ORCA Timing Characteristics

To define speed grades, the *ORCA* Series part number designation (see Table 42) uses a single-digit number to designate a speed grade. This number is not related to any single ac parameter. Higher numbers indicate a faster set of timing parameters. The actual speed sorting is based on testing the delay in a path consisting of an input buffer, all PLCs in a column, and an output buffer.

The most accurate timing characteristics are reported by the timing analyzer. A timing report provided by the development system after layout divides path delays into logic and routing delays. Some third-party CAE software provides logic delays prior to layout. While this allows routing budget estimates, there is wide variance in routing delays associated with different layouts.

The logic timing parameters noted in the Electrical Characteristics section of this data sheet are the same as those in the design tools. In the PFU timing given in Table 27, symbol names are generally a concatenation of the PFU operating mode (as defined in Table 2) and the parameter type. The wildcard character (*) is used in symbol names to indicate that the parameter applies to any sub-LUT. The setup, hold, and propagation delay parameters, defined below, are designated in the symbol name by SET, HLD, and DEL characters, respectively.

The values given for the parameters are worst-case in that the production tests of the AT&T FPGAs use supply voltage and operating temperature extremes for the speed grade/temperature being tested. Actual delays at nominal temperature and voltage for best-case processes can be much better than the values given in Table 26. The best-case AT&T 0.6 µm process is typically 50% faster than a worst-case process. Table 12 provides approximate power supply and temperature derating. Taken cumulatively, the range of parameter values for best-case vs. worst-case processing, supply voltage, and temperature can approach 3 to 1.

In addition to supply voltage, process variation, and operating temperature, circuit and process improvements of the *ORCA* series FPGAs over time will result in significant improvement of the actual performance over those listed for a speed grade. Even though lower speed grades may still be available, the distribution of yield to timing parameters may be several speed bins higher than that designated on a product brand. Design practices need to consider best-case timing parameters (e.g., delays = 0), as well as worst-case timing.

Table 12. Power Supply and Temperature Derating

Temp (°C)	Power Supply Voltage				
	4.5 V	4.75 V	5.0 V	5.25 V	5.5 V
–40	0.86	0.82	0.79	0.76	0.74
0	1.03	0.98	0.94	0.91	0.88
25	1.09	1.04	1.00	0.97	0.94
85	1.31	1.25	1.20	1.17	1.13
125	1.44	1.38	1.32	1.28	1.24

The routing delays are a function of fan-out and the capacitance associated with the CIPs and metal interconnect in the path. The number of logic elements which can be driven (or fan-out) by PFUs is unlimited, although the delay to reach a valid logic level can exceed timing requirements. It is difficult to make accurate routing delay estimates prior to design compilation based on fan-out. This is because the CAE software may delete redundant logic inserted by the designer to reduce fan-out, and/or it may also automatically reduce fan-out by net splitting.

The waveform test points are given in the Measurement Conditions section of this data sheet. The timing parameters given in the electrical characteristics tables in this data sheet follow industry practices, and the values they reflect are described below.

Propagation Delay—the time between the specified reference points. The delays provided are the worst case of the tphh and tpll delays for noninverting functions, tplh and tphl for inverting functions, and tphz and tplz for 3-state enable.

Setup Time—the interval immediately preceding the transition of a clock or latch enable signal, during which the data must be stable to ensure it is recognized as the intended value.

Hold Time—the interval immediately following the transition of a clock or latch enable signal, during which the data must be held stable to ensure it is recognized as the intended value.

3-state Enable—the time from when a ts[3:0] signal becomes active and the output pad reaches the high-impedance state.

Estimating Power Dissipation

The total operating power dissipated is estimated by summing the standby (I_{DDSB}), internal, and external power dissipated. The internal and external power is the power consumed in the PLCs and PICs, respectively. In general, the standby power is small and may be neglected. The total operating power is as follows:

The internal operating power is made of two parts: clock generation and PFU output power. PFU output power can be estimated based on the number of PFU outputs switching when driving an average fan-out of 2:

$$P_{PFU} = 0.34 \text{ mW/MHz}$$

For each PFU output that switches, 0.34 mW/MHz needs to be multiplied by the frequency (in MHz) that the output switches. Generally, this can be estimated by using one-half the clock rate, multiplied by some activity factor; for example, 20%.

The power dissipated by the clock generation circuitry is based upon three parts: the fixed clock power, the power/clock branch row or column, and the clock power dissipated in each PFU that uses this particular clock. Therefore, the clock power can be calculated for the three parts using the following equations:

1C03 Clock Power

P = [0.89 mW/MHz
+ (0.32 mW/MHz – Branch) (# Branches)
+ (0.026 mW/MHz – PFU) (# PFUs)] f_{CLK}

For a quick estimate, the worst-case (typical circuit) 1C03 clock power ≈ 5.4 mW/MHz.

1C05 Clock Power

P = [0.99 mW/MHz
+ (0.36 mW/MHz – Branch) (# Branches)
+ (0.026 mW/MHz – PFU) (# PFUs)] f_{CLK}

For a quick estimate, the worst-case (typical circuit) 1C05 Clock Power ≈ 7.2 mW/MHz.

1C07 Clock Power

P = [1.11 mW/MHz
+ (0.40 mW/MHz – Branch) (# Branches)
+ (0.026 mW/MHz – PFU) (# PFUs)] f_{CLK}

For a quick estimate, the worst-case (typical circuit) 1C07 Clock Power ≈ 9.3 mW/MHz.

1C09 Clock Power

P = [1.22 mW/MHz
+ (0.43 mW/MHz – Branch) (# Branches)
+ (0.026 mW/MHz – PFU) (# PFUs)] f_{CLK}

For a quick estimate, the worst-case (typical circuit) 1C09 Clock Power ≈ 11.5 mW/MHz.

The power dissipated in a PIC is the sum of the power dissipated in the four I/Os in the PIC. This consists of power dissipated by inputs and ac power dissipated by outputs. The power dissipated in each I/O depends on whether it is configured as an input, output, or input/output. If an I/O is operating as an output, then there is a power dissipation component for P_{IN}, as well as P_{OUT}. This is because the output feeds back to the input.

The power dissipated by a TTL input buffer is estimated as:

$$P_{TTL} = 1.8 \text{ mW} + 0.35 \text{ mW/MHz}$$

The power dissipated by a CMOS input buffer is estimated as:

$$P_{CMOS} = 0.35 \text{ mW/MHz}$$

The ac power dissipation from an output or bidirectional is estimated by the following:

$P_{OUT} = (C_L + 7.4 \text{ pF}) \times V_{DD}^2 \times F$ W; the unit for C_L is farads, and the unit for F is Hz.

As an example of estimating power dissipation, suppose a fully utilized 1C07 has an average of 3 outputs for each of the 196 PFUs, that all 14 clock branches are used, 75 of the 196 PFUs have FFs clocked at 30 MHz, and the PFUs have an average activity factor of 20%. Twenty TTL-configured inputs, 20 CMOS-configured inputs, 32 outputs driving 30 pF loads, and 16 bidirectional I/Os driving 50 pF loads are also generated from the 40 MHz clock with an average activity factor of 20%. The worst-case power dissipation is estimated as follows:

P_{PFU} = 196 x 3 (0.34 mW/MHz x 15 MHz x 20%)
= 600 mW

P_{CLK} = [1.11 mW/MHz + (0.40 mW/MHz – Branch) (14 Branches)
+ (0.026 mW/MHz – PFU) (75 PFUs) [30 MHz]]
= 260 mW

P_{TTL} = 20 x [1.8 mW + (0.35 mW/MHz x 15 MHz x 20%)]
= 57 mW

P_{CMOS} = 20 x [0.35 mW x 15 MHz x 20%]
= 21 mW

P_{OUT} = 30 x [(30 pF + 7.4 pF) x 5.25^2 x 15 MHz x 20%]
= 93 mW

P_{BID} = 16 x [(50 pF + 7.4 pF) x 5.25^2 x 15 MHz x 20%]
= 76 mW

TOTAL = 1.11 W

Pin Information

Table 13. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD	—	Positive power supply.
GND	—	Ground supply.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration. During operation, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input which causes all PLC latches/FFs to be asynchronously globally set/reset.
CCLK	I	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in. In the slave or synchronous peripheral mode, CCLK is input synchronous with the data on DIN or D[7:0].
DONE	I/O	DONE is a bidirectional pin with an optional pull-up resistor. As an output, it indicates that configuration is complete. As an input, a low level on DONE delays FPGA start-up after configuration.
$\overline{\text{PRGM}}$	I	$\overline{\text{PRGM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry.
$\overline{\text{RD\_CFGN}}$	I	After configuration, a high-to-low transition on $\overline{\text{RD\_CFGN}}$ initiates a readback of configuration data, including PFU output states, starting with frame address 0. During configuration, this pin should be a logic "1" to ensure compatibility with future upgrades.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary scan, TDO is test data out.
Special-Purpose Pins		
RDY/$\overline{\text{BUSY}}$	O	During configuration in peripheral mode, RDY/$\overline{\text{BUSY}}$ indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. After configuration, the pin is a user-programmable I/O. This pin is shared with RCLK.
RCLK	O	During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used. After configuration, this pin is a user-programmable I/O pin. This pin is shared with RDY/$\overline{\text{BUSY}}$.
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. After configuration, this pin is a user-programmable I/O pin.
M0, M1, M2	I	M[2:0] are used to select the configuration mode. See Table 8 for the configuration modes. After configuration, the pins are user-programmable I/O.
M3	I	M3 is used to select the frequency of the internal oscillator during configuration. When M3 is low, the oscillator frequency is 10 MHz. When M3 is high, the oscillator is 1.25 MHz. After configuration, this pin is a user I/O pin.
TDI, TCK, TMS	I	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs. If boundary scan is not selected, all boundary-scan functions are inhibited once configuration is complete, and these pins are user-programmable I/O pins. Also, either TCK or TMS must be held at logic 1 during configuration.
HDC	O	High During Configuration is output high until configuration is complete. It is used as a control output indicating that configuration is not complete. After configuration, this pin is a user-programmable I/O pin.

Pin Information (continued)

Table 13. Pin Descriptions (continued)

Symbol	I/O	Description
$\overline{\text{LDC}}$	O	$\overline{\text{Low During Configuration}}$ is output low until configuration is complete. It is used as a control output indicating that configuration is not complete. After configuration, this pin is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. An external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, the pin is a user-programmable I/O pin.
$\overline{\text{CS0}}$, CS1, $\overline{\text{WR}}$, $\overline{\text{RD}}$	I	$\overline{\text{CS0}}$, CS1, $\overline{\text{WR}}$, $\overline{\text{RD}}$ are used in the asynchronous peripheral configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. When selected, a low on the write strobe, $\overline{\text{WR}}$, loads the data on D[7:0] inputs into an internal data buffer. $\overline{\text{WR}}$, $\overline{\text{CS0}}$, and CS1 are also used as chip selects in the slave parallel mode. A low on $\overline{\text{RD}}$ changes D7 into a status output. As a status indication, a high indicates ready and a low indicates busy. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. After configuration, the pins are programmable I/O pins.
A[17:0]	O	During master parallel configuration mode, A[17:0] address the configuration EPROM. After configuration, the pins are user-programmable I/O pins.
D[7:0]	I	During master parallel, peripheral, and slave parallel configuration modes, D[7:0] receive configuration data. After configuration, the pins are user-programmable I/O pins.
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave LCA devices. Data out on DOUT changes on the falling edge of CCLK. After configuration, DOUT is a user-programmable I/O pin.

Pin Information (continued)

Package Compatibility

The package pinouts are consistent across *ORCA* Series FPGAs. This allows a designer to select a package based on I/O requirements and change the FPGA without revising the layout of the printed-circuit board. The change can be to a larger FPGA, if added functionality is needed, or to a smaller FPGA to decrease unit cost.

The ATT1C03 and ATT1C05 have identical pinouts in the 84-pin PLCC, 100-pin TQFP, and 132-pin BQFP.

The ATT1C05, ATT1C07, and ATT1C09 have identical pinouts in the 208-pin SQFP. The ATT1C03 has the same power and dedicated pins as the other *ORCA* Series devices, but there are 11 package pins which are not connected.

The ATT1C03 and ATT1C05 have identical VDD/VSS pins, and the ATT1C03 I/O locations match the I/O locations in the ATT1C05.

In the 225-pin CPGA/PPGA package, the ATT1C03 has 32 package pins which are not connected.

In the 240-pin SQFP, the ATT1C07, and ATT1C09 are identical except for pins 113 and 188.

In the 304-pin SQFP, the ATT1C07 has the same VDD and VSS pins as the ATT1C09, with fewer I/Os.

Package dimensions are provided on pages 97—107.

Table 14 provides the number of user I/Os available for AT&T *ORCA* Series FPGAs for each available package. Each package has six dedicated configuration pins.

Tables 15—23 provide the package pins and pin functions for the *ORCA* Series FPGAs and packages. The bond pad name is identified in the PIC nomenclature used in the *ORCA* Foundry Design Editor.

Table 14. *ORCA* 1C Series FPGA I/Os Summary

Device	84-Pin PLCC	100-Pin TQFP	132-Pin BQFP	144-Pin TQFP	208-Pin SQFP	225-Pin CPGA/ PPGA	240-Pin SQFP	280-Pin CPGA	304-Pin SQFP
ATT1C03									
User I/Os	64	77	106	114	160	160	—	—	—
VDD/VSS	14	17	20	24	31	27	—	—	—
ATT1C05									
User I/Os	64	77	106	114	171	192	192	—	—
VDD/VSS	14	17	20	24	31	27	42	—	—
ATT1C07									
User I/Os	—	—	—	—	171	—	192	224	224
VDD/VSS	—	—	—	—	31	—	40	34	46
ATT1C09									
User I/Os	—	—	—	—	171	—	192	—	252
VDD/VSS	—	—	—	—	31	—	40	—	46

Pin Information (continued)

Table 15. ATT1C03 and ATT1C05 84-Pin PLCC Pinout

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
1	VSS	VSS	VSS	43	VSS	VSS	VSS
2	PTE0	PTF0	I/O-D2	44	PBF0	PBG0	I/O
3	VSS	VSS	VSS	45	VSS	VSS	VSS
4	PTD3	PTE3	I/O-D1	46	PBG0	PBH0	I/O
5	PTD0	PTE0	I/O-D0/DIN	47	PBG3	PBH3	I/O
6	PTC0	PTD0	I/O-DOUT	48	PBH0	PBI0	I/O-HDC
7	PTB3	PTC3	I/O	49	PBI0	PBJ0	I/O-$\overline{\text{LDC}}$
8	PTB0	PTC0	I/O-TDI	50	PBI3	PBJ3	I/O
9	PTA3	PTB0	I/O-TMS	51	PBJ0	PBK0	I/O-$\overline{\text{INIT}}$
10	PTA0	PTA0	I/O-TCK	52	PBJ3	PBL0	I/O
11	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO	53	DONE	DONE	DONE
12	VDD	VDD	VDD	54	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
13	VSS	VSS	VSS	55	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
14	PLA2	PLA0	I/O-A0	56	PRJ0	PRL0	I/O-M0
15	PLA0	PLB0	I/O-A1	57	PRJ3	PRK0	I/O
16	PLB3	PLC3	I/O-A2	58	PRI0	PRJ0	I/O-M1
17	PLB0	PLC0	I/O-A3	59	PRI3	PRJ3	I/O
18	PLC0	PLD0	I/O-A4	60	PRH0	PRI0	I/O-M2
19	PLD3	PLE3	I/O-A5	61	PRG0	PRH0	I/O-M3
20	PLD0	PLE0	I/O-A6	62	PRG3	PRH3	I/O
21	PLE0	PLF0	I/O-A7	63	PRF0	PRG0	I/O
22	VDD	VDD	VDD	64	VDD	VDD	VDD
23	PLF0	PLG0	I/O-A8	65	PRE0	PRF0	I/O
24	VSS	VSS	VSS	66	VSS	VSS	VSS
25	PLG3	PLH3	I/O-A9	67	PRD0	PRE0	I/O
26	PLG0	PLH0	I/O-A10	68	PRD3	PRE3	I/O
27	PLH0	PLI0	I/O-A11	69	PRC0	PRD0	I/O-CS1
28	PLI3	PLJ3	I/O-A12	70	PRB0	PRC0	I/O-$\overline{\text{CS0}}$
29	PLI0	PLJ0	I/O-A13	71	PRB3	PRC3	I/O
30	PLJ3	PLK0	I/O-A14	72	PRA0	PRB0	I/O-$\overline{\text{RD}}$
31	PLJ0	PLL0	I/O-A15	73	PRA3	PRA0	I/O-$\overline{\text{WR}}$
32	CCLK	CCLK	CCLK	74	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$
33	VDD	VDD	VDD	75	VDD	VDD	VDD
34	VSS	VSS	VSS	76	VSS	VSS	VSS
35	PBA0	PBA0	I/O-A16	77	PTJ2	PTL0	I/O-RDY/RCLK
36	PBA3	PBB0	I/O-A17	78	PTI3	PTK0	I/O-D7
37	PBB0	PBC0	I/O	79	PTI2	PTJ3	I/O
38	PBB3	PBC3	I/O	80	PTI0	PTJ0	I/O-D6
39	PBC0	PBD0	I/O	81	PTH0	PTI0	I/O-D5
40	PBD0	PBE0	I/O	82	PTG3	PTH3	I/O
41	PBD3	PBE3	I/O	83	PTG0	PTH0	I/O-D4
42	PBE0	PBF0	I/O	84	PTF0	PTG0	I/O-D3

Pin Information (continued)

Table 16. ATT1C03 and ATT1C05 100-Pin TQFP Pinout

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
1	VDD	VDD	VDD	43	PBH2	PBI2	I/O
2	VSS	VSS	VSS	44	PBH3	PBI3	I/O
3	PLA2	PLA0	I/O-A0	45	PBI0	PBJ0	I/O-$\overline{LDC}$
4	PLA0	PLB0	I/O-A1	46	PBI3	PBJ3	I/O
5	PLB3	PLC3	I/O-A2	47	PBJ0	PBK0	I/O-$\overline{INIT}$
6	PLB0	PLC0	I/O-A3	48	PBJ3	PBL0	I/O
7	PLC3	PLD3	I/O	49	DONE	DONE	DONE
8	PLC0	PLD0	I/O-A4	50	VDD	VDD	VDD
9	PLD3	PLE3	I/O-A5	51	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$
10	PLD0	PLE0	I/O-A6	52	$\overline{PRGM}$	$\overline{PRGM}$	$\overline{PRGM}$
11	PLE3	PLF3	I/O	53	PRJ0	PRL0	I/O-M0
12	PLE0	PLF0	I/O-A7	54	PRJ3	PRK0	I/O
13	VDD	VDD	VDD	55	PRI0	PRJ0	I/O-M1
14	PLF0	PLG0	I/O-A8	56	PRI3	PRJ3	I/O
15	VSS	VSS	VSS	57	PRH0	PRI0	I/O-M2
16	PLG3	PLH3	I/O-A9	58	PRH3	PRI3	I/O
17	PLG0	PLH0	I/O-A10	59	PRG0	PRH0	I/O-M3
18	PLH0	PLI0	I/O-A11	60	PRG3	PRH3	I/O
19	PLI3	PLJ3	I/O-A12	61	VSS	VSS	VSS
20	PLI2	PLJ2	I/O	62	PRF0	PRG0	I/O
21	PLI0	PLJ0	I/O-A13	63	VDD	VDD	VDD
22	PLJ3	PLK0	I/O-A14	64	PRE0	PRF0	I/O
23	PLJ0	PLL0	I/O-A15	65	VSS	VSS	VSS
24	VSS	VSS	VSS	66	PRD0	PRE0	I/O
25	CCLK	CCLK	CCLK	67	PRD3	PRE3	I/O
26	VDD	VDD	VDD	68	PRC0	PRD0	I/O-CS1
27	VSS	VSS	VSS	69	PRC3	PRD3	I/O
28	PBA0	PBA0	I/O-A16	70	PRB0	PRC0	I/O-$\overline{CS0}$
29	PBA2	PBA3	I/O	71	PRB3	PRC3	I/O
30	PBA3	PBB0	I/O-A17	72	PRA0	PRB0	I/O-$\overline{RD}$
31	PBB0	PBC0	I/O	73	PRA2	PRB3	I/O
32	PBB3	PBC3	I/O	74	PRA3	PRA0	I/O-$\overline{WR}$
33	PBC0	PBD0	I/O	75	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
34	PBD0	PBE0	I/O	76	VDD	VDD	VDD
35	PBD3	PBE3	I/O	77	VSS	VSS	VSS
36	PBE0	PBF0	I/O	78	PTJ2	PTL0	I/O-RDY/RCLK
37	VSS	VSS	VSS	79	PTI3	PTK0	I/O-D7
38	PBF0	PBG0	I/O	80	PTI2	PTJ3	I/O
39	VSS	VSS	VSS	81	PTI0	PTJ0	I/O-D6
40	PBG0	PBH0	I/O	82	PTH3	PTI3	I/O
41	PBG3	PBH3	I/O	83	PTH0	PTI0	I/O-D5
42	PBH0	PBI0	I/O-HDC	84	PTG3	PTH3	I/O

Pin Information (continued)

Table 16. ATT1C03 and ATT1C05 100-Pin TQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
85	PTG0	PTH0	I/O-D4	93	PTC3	PTD3	I/O
86	PTF3	PTG3	I/O	94	PTC0	PTD0	I/O-DOUT
87	PTF0	PTG0	I/O-D3	95	PTB3	PTC3	I/O
88	Vss	Vss	Vss	96	PTB0	PTC0	I/O-TDI
89	PTE0	PTF0	I/O-D2	97	PTA3	PTB0	I/O-TMS
90	Vss	Vss	Vss	98	PTA2	PTA3	I/O
91	PTD3	PTE3	I/O-D1	99	PTA0	PTA0	I/O-TCK
92	PTD0	PTE0	I/O-D0/DIN	100	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO

Pin Information (continued)

Table 17. ATT1C03 and ATT1C05 132-Pin BQFP Pinout

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
1	VSS	VSS	VSS	43	PLH0	PLI0	I/O-A11
2	PTE3	PTF3	I/O	44	PLI3	PLJ3	I/O-A12
3	PTE2	PTF2	I/O	45	PLI0	PLJ0	I/O-A13
4	PTE0	PTF0	I/O-D2	46	PLJ3	PLK0	I/O-A14
5	PTD3	PTE3	I/O-D1	47	PLJ2	PLL3	I/O
6	PTD0	PTE0	I/O-D0/DIN	48	PLJ0	PLL0	I/O-A15
7	PTC3	PTD3	I/O	49	VSS	VSS	VSS
8	PTC0	PTD0	I/O-DOUT	50	CCLK	CCLK	CCLK
9	VDD	VDD	VDD	51	VSS	VSS	VSS
10	PTB3	PTC3	I/O	52	PBA0	PBA0	I/O-A16
11	PTB2	PTC2	I/O	53	PBA2	PBA3	I/O
12	PTB0	PTC0	I/O-TDI	54	PBA3	PBB0	I/O-A17
13	PTA3	PTB0	I/O-TMS	55	PBB0	PBB3	I/O
14	PTA2	PTA3	I/O	56	PBB2	PBC0	I/O
15	PTA0	PTA0	I/O-TCK	57	PBB3	PBC3	I/O
16	VSS	VSS	VSS	58	VDD	VDD	VDD
17	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO	59	PBC0	PBD0	I/O
18	VSS	VSS	VSS	60	PBC3	PBD3	I/O
19	PLA3	PLA3	I/O	61	PBD0	PBE0	I/O
20	PLA2	PLA0	I/O-A0	62	PBD2	PBE2	I/O
21	PLA1	PLB3	I/O	63	PBD3	PBE3	I/O
22	PLA0	PLB0	I/O-A1	64	PBE0	PBF0	I/O
23	PLB3	PLC3	I/O-A2	65	PBE2	PBF2	I/O
24	PLB0	PLC0	I/O-A3	66	PBE3	PBF3	I/O
25	PLC3	PLD3	I/O	67	VSS	VSS	VSS
26	PLC2	PLD2	I/O	68	PBF0	PBG0	I/O
27	PLC0	PLD0	I/O-A4	69	PBF2	PBG2	I/O
28	PLD3	PLE3	I/O-A5	70	PBF3	PBG3	I/O
29	PLD0	PLE0	I/O-A6	71	PBG0	PBH0	I/O
30	VSS	VSS	VSS	72	PBG3	PBH3	I/O
31	PLE3	PLF3	I/O	73	PBH0	PBI0	I/O-HDC
32	PLE2	PLF2	I/O	74	PBH3	PBI3	I/O
33	PLE0	PLF0	I/O-A7	75	VDD	VDD	VDD
34	VDD	VDD	VDD	76	PBI0	PBJ0	I/O-$\overline{LDC}$
35	PLF3	PLG3	I/O	77	PBI2	PBJ2	I/O
36	PLF2	PLG2	I/O	78	PBI3	PBJ3	I/O
37	PLF0	PLG0	I/O-A8	79	PBJ0	PBK0	I/O-$\overline{INIT}$
38	VSS	VSS	VSS	80	PBJ2	PBK3	I/O
39	PLG3	PLH3	I/O-A9	81	PBJ3	PBL0	I/O
40	PLG0	PLH0	I/O-A10	82	VSS	VSS	VSS
41	PLH3	PLI3	I/O	83	DONE	DONE	DONE
42	PLH2	PLI2	I/O	84	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$

Pin Information (continued)

Table 17. ATT1C03 and ATT1C05 132-Pin BQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
85	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	109	PRB0	PRC0	I/O-$\overline{\text{CS0}}$
86	PRJ0	PRL0	I/O-M0	110	PRB3	PRC3	I/O
87	PRJ1	PRL3	I/O	111	PRA0	PRB0	I/O-$\overline{\text{RD}}$
88	PRJ3	PRK0	I/O	112	PRA1	PRB2	I/O
89	PRI0	PRJ0	I/O-M1	113	PRA2	PRB3	I/O
90	PRI2	PRJ2	I/O	114	PRA3	PRA0	I/O-$\overline{\text{WR}}$
91	PRI3	PRJ3	I/O	115	VSS	VSS	VSS
92	PRH0	PRI0	I/O-M2	116	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$
93	PRH1	PRI1	I/O	117	VSS	VSS	VSS
94	PRH3	PRI3	I/O	118	PTJ3	PTL3	I/O
95	PRG0	PRH0	I/O-M3	119	PTJ2	PTL0	I/O-RDY/RCLK
96	PRG3	PRH3	I/O	120	PTJ1	PTK3	I/O
97	VSS	VSS	VSS	121	PTI3	PTK0	I/O-D7
98	PRF0	PRG0	I/O	122	PTI2	PTJ3	I/O
99	PRF3	PRG3	I/O	123	PTI0	PTJ0	I/O-D6
100	VDD	VDD	VDD	124	VDD	VDD	VDD
101	PRE0	PRF0	I/O	125	PTH3	PTI3	I/O
102	PRE3	PRF3	I/O	126	PTH0	PTI0	I/O-D5
103	VSS	VSS	VSS	127	PTG3	PTH3	I/O
104	PRD0	PRE0	I/O	128	PTG1	PTH1	I/O
105	PRD3	PRE3	I/O	129	PTG0	PTH0	I/O-D4
106	PRC0	PRD0	I/O-CS1	130	PTF3	PTG3	I/O
107	PRC3	PRD3	I/O	131	PTF2	PTG2	I/O
108	VDD	VDD	VDD	132	PTF0	PTG0	I/O-D3

Pin Information (continued)

Table 18. ATT1C03 and ATT1C05 144-Pin TQFP Pinout

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
1	VDD	VDD	VDD	43	PBB1	PBC1	I/O
2	VSS	VSS	VSS	44	PBB3	PBC3	I/O
3	PLA2	PLA0	I/O-A0	45	VDD	VDD	VDD
4	PLA1	PLB3	I/O	46	PBC0	PBD0	I/O
5	PLA0	PLB0	I/O-A1	47	PBC3	PBD3	I/O
6	PLB3	PLC3	I/O-A2	48	PBD0	PBE0	I/O
7	PLB0	PLC0	I/O-A3	49	PBD2	PBE2	I/O
8	PLC3	PLD3	I/O	50	PBD3	PBE3	I/O
9	PLC2	PLD2	I/O	51	PBE0	PBF0	I/O
10	PLC0	PLD0	I/O-A4	52	PBE2	PBF2	I/O
11	PLD3	PLE3	I/O-A5	53	PBE3	PBF3	I/O
12	PBD2	PBE2	I/O	54	VSS	VSS	VSS
13	PLD0	PLE0	I/O-A6	55	PBF0	PBG0	I/O
14	VSS	VSS	VSS	56	PBF2	PBG2	I/O
15	PLE3	PLF3	I/O	57	PBF3	PBG3	I/O
16	PLE2	PLF2	I/O	58	PBG0	PBH0	I/O
17	PLE0	PLF0	I/O-A7	59	PBG3	PBH3	I/O
18	VDD	VDD	VDD	60	PBH0	PBI0	I/O-HDC
19	PLF3	PLG3	I/O	61	PBH2	PBI2	I/O
20	PLF2	PLG2	I/O	62	PBH3	PBI3	I/O
21	PLF0	PLG0	I/O-A8	63	VDD	VDD	VDD
22	VSS	VSS	VSS	64	PBI0	PBJ0	I/O-$\overline{\text{LDC}}$
23	PLG3	PLH3	I/O-A9	65	PBI2	PBJ2	I/O
24	PLG0	PLH0	I/O-A10	66	PBI3	PBJ3	I/O
25	PLH3	PLI3	I/O	67	PBJ0	PBK0	I/O-$\overline{\text{INIT}}$
26	PLH2	PLI2	I/O	68	PBJ2	PBK3	I/O
27	PLH0	PLI0	I/O-A11	69	PBJ3	PBL0	I/O
28	PLI3	PLJ3	I/O-A12	70	VSS	VSS	VSS
29	PLI2	PLJ2	I/O	71	DONE	DONE	DONE
30	PLI0	PLJ0	I/O-A13	72	VDD	VDD	VDD
31	PLJ3	PLK0	I/O-A14	73	VSS	VSS	VSS
32	PLJ2	PLL3	I/O	74	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
33	PLJ1	PLL1	I/O	75	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
34	PLJ0	PLL0	I/O-A15	76	PRJ0	PRL0	I/O-M0
35	VSS	VSS	VSS	77	PRJ1	PRL3	I/O
36	CCLK	CCLK	CCLK	78	PRJ3	PRK0	I/O
37	VDD	VDD	VDD	79	PRI0	PRJ0	I/O-M1
38	VSS	VSS	VSS	80	PRI2	PRJ2	I/O
39	PBA0	PBA0	I/O-A16	81	PRI3	PRJ3	I/O
40	PBA2	PBA3	I/O	82	PRH0	PRI0	I/O-M2
41	PBA3	PBB0	I/O-A17	83	PRH1	PRI1	I/O
42	PBB0	PBC0	I/O	84	PRH3	PRI3	I/O

Pin Information (continued)

Table 18. ATT1C03 and ATT1C05 144-Pin TQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
85	PRG0	PRH0	I/O-M3	115	PTI2	PTJ3	I/O
86	PRG3	PRH3	I/O	116	PTI1	PTJ2	I/O
87	VSS	VSS	VSS	117	PTI0	PTJ0	I/O-D6
88	PRF0	PRG0	I/O	118	VDD	VDD	VDD
89	PRF2	PRG2	I/O	119	PTH3	PTI3	I/O
90	PRF3	PRG3	I/O	120	PTH0	PTI0	I/O-D5
91	VDD	VDD	VDD	121	PTG3	PTH3	I/O
92	PRE0	PRF0	I/O	122	PTG1	PTH1	I/O
93	PRE2	PRF2	I/O	123	PTG0	PTH0	I/O-D4
94	PRE3	PRF3	I/O	124	PTF3	PTG3	I/O
95	VSS	VSS	VSS	125	PTF2	PTG2	I/O
96	PRD0	PRE0	I/O	126	PTF0	PTG0	I/O-D3
97	PRD2	PRE2	I/O	127	VSS	VSS	VSS
98	PRD3	PRE3	I/O	128	PTE3	PTF3	I/O
99	PRC0	PRD0	I/O-CS1	129	PTE2	PTF2	I/O
100	PRC3	PRD3	I/O	130	PTE0	PTF0	I/O-D2
101	PRB0	PRC0	I/O-$\overline{CS0}$	131	PTD3	PTE3	I/O-D1
102	PRB3	PRC3	I/O	132	PTD2	PTE2	I/O
103	PRA0	PRB0	I/O-$\overline{RS}$	133	PTD0	PTE0	I/O-D0/DIN
104	PRA1	PRB1	I/O	134	PTC3	PTD3	I/O
105	PRA2	PRB3	I/O	135	PTC0	PTD0	I/O-DOUT
106	PRA3	PRA0	I/O-$\overline{WS}$	136	VDD	VDD	VDD
107	VSS	VSS	VSS	137	PTB3	PTC3	I/O
108	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	138	PTB2	PTC2	I/O
109	VDD	VDD	VDD	139	PTB0	PTC0	I/O-TDI
110	VSS	VSS	VSS	140	PTA3	PTB0	I/O-TMS
111	PTJ3	PTL3	I/O	141	PTA2	PTA3	I/O
112	PTJ2	PTL0	I/O-RDY/RCLK	142	PTA0	PTA0	I/O-TCK
113	PTJ1	PTK3	I/O	143	VSS	VSS	VSS
114	PTI3	PTK0	I/O-D7	144	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/TDO

Pin Information (continued)

Table 19. ATT1C03, ATT1C05, ATT1C07, and ATT1C09 208-Pin SQFP Pinout

Pin	1C03 Pad	1C05 Pad	1C07 Pad	1C09 Pad	Function
1	VSS	VSS	VSS	VSS	VSS
2	VSS	VSS	VSS	VSS	VSS
3	PLA3	PLA3	PLA3	PLA3	I/O
4	PLA2	PLA0	PLB3	PLB3	I/O-A0
5	PLA1	PLB3	PLC3	PLC3	I/O
6	See Note	PLB2	PLC2	PLC2	I/O
7	PLA0	PLB0	PLC0	PLC0	I/O-A1
8	PLB3	PLC3	PLD3	PLD0	I/O-A2
9	PLB2	PLC2	PLD2	PLE2	I/O
10	PLB1	PLC1	PLD1	PLE1	I/O
11	PLB0	PLC0	PLD0	PLE0	I/O-A3
12	VDD	VDD	VDD	VDD	VDD
13	PLC3	PLD3	PLE3	PLF3	I/O
14	PLC2	PLD2	PLE2	PLF2	I/O
15	PLC1	PLD1	PLE1	PLF1	I/O
16	PLC0	PLD0	PLE0	PLF0	I/O-A4
17	PLD3	PLE3	PLF3	PLG3	I/O-A5
18	PLD2	PLE2	PLF2	PLG2	I/O
19	PLD1	PLE1	PLF1	PLG1	I/O
20	PLD0	PLE0	PLF0	PLG0	I/O-A6
21	VSS	VSS	VSS	VSS	VSS
22	PLE3	PLF3	PLG3	PLH3	I/O
23	PLE2	PLF2	PLG2	PLH2	I/O
24	PLE1	PLF1	PLG1	PLH1	I/O
25	PLE0	PLF0	PLG0	PLH0	I/O-A7
26	VDD	VDD	VDD	VDD	VDD
27	PLF3	PLG3	PLH3	PLI3	I/O
28	PLF2	PLG2	PLH2	PLI2	I/O
29	PLF1	PLG1	PLH1	PLI1	I/O
30	PLF0	PLG0	PLH0	PLI0	I/O-A8
31	VSS	VSS	VSS	VSS	VSS
32	PLG3	PLH3	PLI3	PLJ3	I/O-A9
33	PLG2	PLH2	PLI2	PLJ2	I/O
34	PLG1	PLH1	PLI1	PLJ1	I/O
35	PLG0	PLH0	PLI0	PLJ0	I/O-A10
36	PLH3	PLI3	PLJ3	PLK3	I/O
37	PLH2	PLI2	PLJ2	PLK2	I/O
38	PLH1	PLI1	PLJ1	PLK1	I/O
39	PLH0	PLI0	PLJ0	PLK0	I/O-A11
40	VDD	VDD	VDD	VDD	VDD
41	PLI3	PLJ3	PLK3	PLL3	I/O-A12
42	PLI2	PLJ2	PLK2	PLL2	I/O

Note: The ATT1C03 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 19. ATT1C03, ATT1C05, ATT1C07, and ATT1C09 208-Pin SQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	1C07 Pad	1C09 Pad	Function
43	PLI1	PLJ1	PLK1	PLL1	I/O
44	PLI0	PLJ0	PLK0	PLM3	I/O-A13
45	See Note	PLK3	PLL3	PLM1	I/O
46	PLJ3	PLK0	PLL0	PLN2	I/O-A14
47	See Note	PLL3	PLM3	PLO3	I/O
48	PLJ2	PLL2	PLM0	PLO0	I/O
49	PLJ1	PLL1	PLN3	PLP3	I/O
50	PLJ0	PLL0	PLN0	PLP0	I/O-A15
51	VSS	VSS	VSS	VSS	VSS
52	CCLK	CCLK	CCLK	CCLK	CCLK
53	VSS	VSS	VSS	VSS	VSS
54	VSS	VSS	VSS	VSS	VSS
55	PBA0	PBA0	PBA0	PBA0	I/O-A16
56	See Note	PBA1	PBA3	PBA3	I/O
57	PBA1	PBA2	PBB0	PBB0	I/O
58	PBA2	PBA3	PBB3	PBB3	I/O
59	PBA3	PBB0	PBC0	PBC1	I/O-A17
60	See Note	PBB3	PBC3	PBD3	I/O
61	PBB0	PBC0	PBD0	PBE0	I/O
62	PBB1	PBC1	PBD1	PBE1	I/O
63	PBB2	PBC2	PBD2	PBE2	I/O
64	PBB3	PBC3	PBD3	PBE3	I/O
65	VDD	VDD	VDD	VDD	VDD
66	PBC0	PBD0	PBE0	PBF0	I/O
67	PBC1	PBD1	PBE1	PBF1	I/O
68	PBC2	PBD2	PBE2	PBF2	I/O
69	PBC3	PBD3	PBE3	PBF3	I/O
70	PBD0	PBE0	PBF0	PBG0	I/O
71	PBD1	PBE1	PBF1	PBG1	I/O
72	PBD2	PBE2	PBF2	PBG2	I/O
73	PBD3	PBE3	PBF3	PBG3	I/O
74	VSS	VSS	VSS	VSS	VSS
75	PBE0	PBF0	PBG0	PBH0	I/O
76	PBE1	PBF1	PBG1	PBH1	I/O
77	PBE2	PBF2	PBG2	PBH2	I/O
78	PBE3	PBF3	PBG3	PBH3	I/O
79	VSS	VSS	VSS	VSS	VSS
80	PBF0	PBG0	PBH0	PBI0	I/O
81	PBF1	PBG1	PBH1	PBI1	I/O
82	PBF2	PBG2	PBH2	PBI2	I/O
83	PBF3	PBG3	PBH3	PBI3	I/O
84	VSS	VSS	VSS	VSS	VSS

Note: The ATT1C03 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 19. ATT1C03, ATT1C05, ATT1C07, and ATT1C09 208-Pin SQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	1C07 Pad	1C09 Pad	Function
85	PBG0	PBH0	PBI0	PBJ0	I/O
86	PBG1	PBH1	PBI1	PBJ1	I/O
87	PBG2	PBH2	PBI2	PBJ2	I/O
88	PBG3	PBH3	PBI3	PBJ3	I/O
89	PBH0	PBI0	PBJ0	PBK0	I/O-HDC
90	PBH1	PBI1	PBJ1	PBK1	I/O
91	PBH2	PBI2	PBJ2	PBK2	I/O
92	PBH3	PBI3	PBJ3	PBK3	I/O
93	VDD	VDD	VDD	VDD	VDD
94	PBI0	PBJ0	PBK0	PBL0	I/O-$\overline{\text{LDC}}$
95	PBI1	PBJ1	PBK3	PBM0	I/O
96	PBI2	PBJ2	PBL0	PBM1	I/O
97	PBI3	PBJ3	PBL1	PBM2	I/O
98	PBJ0	PBK0	PBL2	PBM3	I/O-$\overline{\text{INIT}}$
99	PBJ1	PBK2	PBL3	PBN0	I/O
100	PBJ2	PBK3	PBM0	PBO0	I/O
101	PBJ3	PBL0	PBM3	PBO3	I/O
102	See Note	PBL3	PBN3	PBP3	I/O
103	VSS	VSS	VSS	VSS	VSS
104	DONE	DONE	DONE	DONE	DONE
105	VSS	VSS	VSS	VSS	VSS
106	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
107	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
108	PRJ0	PRL0	PRN0	PRP0	I/O-M0
109	PRJ1	PRL3	PRM0	PRO0	I/O
110	PRJ2	PRK0	PRM3	PRO3	I/O
111	PRJ3	PRK1	PRL0	PRN0	I/O
112	PRI0	PRJ0	PRK0	PRM1	I/O-M1
113	PRI1	PRJ1	PRK1	PRM2	I/O
114	PRI2	PRJ2	PRK2	PRL0	I/O
115	PRI3	PRJ3	PRK3	PRL1	I/O
116	VDD	VDD	VDD	VDD	VDD
117	PRH0	PRI0	PRJ0	PRK0	I/O-M2
118	PRH1	PRI1	PRJ1	PRK1	I/O
119	PRH2	PRI2	PRJ2	PRK2	I/O
120	PRH3	PRI3	PRJ3	PRK3	I/O
121	PRG0	PRH0	PRI0	PRJ0	I/O-M3
122	PRG1	PRH1	PRI1	PRJ1	I/O
123	PRG2	PRH2	PRI2	PRJ2	I/O
124	PRG3	PRH3	PRI3	PRJ3	I/O
125	VSS	VSS	VSS	VSS	VSS
126	PRF0	PRG0	PRH0	PRI0	I/O

Note: The ATT1C03 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 19. ATT1C03, ATT1C05, ATT1C07, and ATT1C09 208-Pin SQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	1C07 Pad	1C09 Pad	Function
127	PRF1	PRG1	PRH1	PRI1	I/O
128	PRF2	PRG2	PRH2	PRI2	I/O
129	PRF3	PRG3	PRH3	PRI3	I/O
130	VDD	VDD	VDD	VDD	VDD
131	PRE0	PRF0	PRG0	PRH0	I/O
132	PRE1	PRF1	PRG1	PRH1	I/O
133	PRE2	PRF2	PRG2	PRH2	I/O
134	PRE3	PRF3	PRG3	PRH3	I/O
135	VSS	VSS	VSS	VSS	VSS
136	PRD0	PRE0	PRF0	PRG0	I/O
137	PRD1	PRE1	PRF1	PRG1	I/O
138	PRD2	PRE2	PRF2	PRG2	I/O
139	PRD3	PRE3	PRF3	PRG3	I/O
140	PRC0	PRD0	PRE0	PRF0	I/O-CS1
141	PRC1	PRD1	PRE1	PRF1	I/O
142	PRC2	PRD2	PRE2	PRF2	I/O
143	PRC3	PRD3	PRE3	PRF3	I/O
144	VDD	VDD	VDD	VDD	VDD
145	PRB0	PRC0	PRD0	PRE0	I/O-$\overline{CS0}$
146	PRB1	PRC1	PRD1	PRD1	I/O
147	PRB2	PRC2	PRD2	PRD2	I/O
148	PRB3	PRC3	PRD3	PRD3	I/O
149	PRA0	PRB0	PRC0	PRC0	I/O-$\overline{RD}$
150	PRA1	PRB2	PRC2	PRC2	I/O
151	PRA2	PRB3	PRC3	PRC3	I/O
152	PRA3	PRA0	PRB0	PRB0	I/O-$\overline{WR}$
153	See Note	PRA2	PRB3	PRB3	I/O
154	See Note	PRA3	PRA0	PRA0	I/O
155	VSS	VSS	VSS	VSS	VSS
156	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
157	VSS	VSS	VSS	VSS	VSS
158	VSS	VSS	VSS	VSS	VSS
159	PTJ3	PTL3	PTN3	PTP3	I/O
160	PTJ2	PTL0	PTM3	PTO3	I/O-RDY/RCLK
161	PTJ1	PTK3	PTM0	PTO0	I/O
162	PTJ0	PTK2	PTL3	PTN3	I/O
163	PTI3	PTK0	PTL2	PTM3	I/O-D7
164	PTI2	PTJ3	PTL0	PTM1	I/O
165	PTI1	PTJ2	PTK3	PTM0	I/O
166	See Note	PTJ1	PTK2	PTL3	I/O
167	PTI0	PTJ0	PTK1	PTL1	I/O-D6
168	VDD	VDD	VDD	VDD	VDD

Note: The ATT1C03 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 19. ATT1C03, ATT1C05, ATT1C07, and ATT1C09 208-Pin SQFP Pinout (continued)

Pin	1C03 Pad	1C05 Pad	1C07 Pad	1C09 Pad	Function
169	PTH3	PTI3	PTJ3	PTK3	I/O
170	PTH2	PTI2	PTJ2	PTK2	I/O
171	PTH1	PTI1	PTJ1	PTK1	I/O
172	PTH0	PTI0	PTJ0	PTK0	I/O-D5
173	PTG3	PTH3	PTI3	PTJ3	I/O
174	PTG2	PTH2	PTI2	PTJ2	I/O
175	PTG1	PTH1	PTI1	PTJ1	I/O
176	PTG0	PTH0	PTI0	PTJ0	I/O-D4
177	Vss	Vss	Vss	Vss	Vss
178	PTF3	PTG3	PTH3	PTI3	I/O
179	PTF2	PTG2	PTH2	PTI2	I/O
180	PTF1	PTG1	PTH1	PTI1	I/O
181	PTF0	PTG0	PTH0	PTI0	I/O-D3
182	Vss	Vss	Vss	Vss	Vss
183	PTE3	PTF3	PTG3	PTH3	I/O
184	PTE2	PTF2	PTG2	PTH2	I/O
185	PTE1	PTF1	PTG1	PTH1	I/O
186	PTE0	PTF0	PTG0	PTH0	I/O-D2
187	Vss	Vss	Vss	Vss	Vss
188	PTD3	PTE3	PTF3	PTG3	I/O-D1
189	PTD2	PTE2	PTF2	PTG2	I/O
190	PTD1	PTE1	PTF1	PTG1	I/O
191	PTD0	PTE0	PTF0	PTG0	I/O-D0/DIN
192	PTC3	PTD3	PTE3	PTF3	I/O
193	PTC2	PTD2	PTE2	PTF2	I/O
194	PTC1	PTD1	PTE1	PTF1	I/O
195	PTC0	PTD0	PTE0	PTF0	I/O-DOUT
196	VDD	VDD	VDD	VD	VDD
197	PTB3	PTC3	PTD3	PTE3	I/O
198	PTB2	PTC2	PTD2	PTE0	I/O
199	PTB1	PTC1	PTD1	PTD3	I/O
200	PTB0	PTC0	PTD0	PTD0	I/O-TDI
201	See Note	PTB3	PTC3	PTC3	I/O
202	PTA3	PTB0	PTC0	PTC0	I/O-TMS
203	See Note	PTA3	PTB3	PTB3	I/O
204	PTA2	PTA2	PTB0	PTB0	I/O
205	PTA1	PTA1	PTA3	PTA3	I/O
206	PTA0	PTA0	PTA0	PTA0	I/O-TCK
207	Vss	Vss	Vss	Vss	Vss
208	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/TDO

Note: The ATT1C03 does not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

Pin Information (continued)

Table 20. ATT1C03 and ATT1C05 225-Pin CPGA/PPGA Pinout

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
A1	CCLK	CCLK	CCLK	C9	Vss	Vss	Vss
A2	PLJ1	PLL2	I/O	C10	PLE3	PLF3	I/O
A3	See Note	PLK3	I/O	C11	PLC0	PLD0	I/O-A4
A4	PLI3	PLJ3	I/O-A12	C12	PLB1	PLC1	I/O
A5	PLH2	PLI2	I/O	C13	See Note	PLB1	I/O
A6	PLG0	PLH0	I/O-A10	C14	PLA2	PLA0	I/O-A0
A7	PLG2	PLH2	I/O	C15	See Note	PTA1	I/O
A8	PLF3	PLG3	I/O	C16	See Note	PTB1	I/O
A9	PLE0	PLF0	I/O-A7	C17	See Note	PTB3	I/O
A10	PLE2	PLF2	I/O	D1	See Note	PBB2	I/O
A11	PLD3	PLE3	I/O-A5	D2	PBA3	PBB0	I/O-A17
A12	PLC1	PLD1	I/O	D3	See Note	PBB1	I/O
A13	PLB0	PLC0	I/O-A3	D4	Vss	Vss	Vss
A14	PLA0	PLB0	I/O-A1	D5	PLJ2	PLL3	I/O
A15	See Note	PLA1	I/O	D6	See Note	PLK2	I/O
A16	PLA3	PLA3	I/O	D7	PLH1	PLI1	I/O
A17	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO	D8	PLG3	PLH3	I/O-A9
B1	See Note	PBA1	I/O	D9	PLE1	PLF1	I/O
B2	PLJ0	PLL0	I/O-A15	D10	PLD0	PLE0	I/O-A6
B3	See Note	PLK1	I/O	D11	PLC2	PLD2	I/O
B4	PLI1	PLJ1	I/O	D12	PLB3	PLC3	I/O-A2
B5	PLH0	PLI0	I/O-A11	D13	PLA1	PLB3	I/O
B6	PLI2	PLJ2	I/O	D14	Vss	Vss	Vss
B7	PLG1	PLH1	I/O	D15	PTA2	PTA3	I/O
B8	PLF1	PLG1	I/O	D16	PTB1	PTC1	I/O
B9	PLF2	PLG2	I/O	D17	PTB3	PTC3	I/O
B10	PLD1	PLE1	I/O	E1	PBB2	PBC2	I/O
B11	PLD2	PLE2	I/O	E2	PBB0	PBC0	I/O
B12	PLC3	PLD3	I/O	E3	PBB1	PBC1	I/O
B13	PLB2	PLC2	I/O	E4	See Note	PBB3	I/O
B14	See Note	PLB2	I/O	E5	VDD	VDD	VDD
B15	See Note	PLA2	I/O	E7	Vss	Vss	Vss
B16	PTA0	PTA0	I/O-TCK	E8	VDD	VDD	VDD
B17	PTA1	PTA2	I/O	E9	Vss	Vss	Vss
C1	PBA2	PBA3	I/O	E10	VDD	VDD	VDD
C2	PBA1	PBA2	I/O	E11	Vss	Vss	Vss
C3	PBA0	PBA0	I/O-A16	E14	PTA3	PTB0	I/O-TMS
C4	See Note	PLL1	I/O	E15	See Note	PTB2	I/O
C5	PLJ3	PLK0	I/O-A14	E16	PTC0	PTD0	I/O-DOUT
C6	PLI0	PLJ0	I/O-A13	E17	PTC2	PTD2	I/O
C7	PLH3	PLI3	I/O	F1	PBC3	PBD3	I/O
C8	PLF0	PLG0	I/O-A8	F2	PBC1	PBD1	I/O

Note: The ATT1C03 does not have bond pads connected to 225-pin CPGA/PPGA package pin numbers A3, A15, B1, B3, B14, B15, C4, C13, C15, C16, C17, D1, D3, D6, E4, and E15, as well as several other pin numbers identified in this table.

Pin Information (continued)

Table 20. ATT1C03 and ATT1C05 225-Pin CPGA/PPGA Pinout (continued)

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
F3	PBC0	PBD0	I/O	K16	PTG1	PTH1	I/O
F4	PBB3	PBC3	I/O	K17	PTF2	PTG2	I/O
F14	PTB0	PTC0	I/O-TDI	L1	PBG0	PBH0	I/O
F15	PTB2	PTC2	I/O	L2	PBH1	PBI1	I/O
F16	PTC1	PTD1	I/O	L3	PBH3	PBI3	I/O
F17	PTD0	PTE0	I/O-D0/DIN	L4	VDD	VDD	VDD
G1	PBD1	PBE1	I/O	L14	VDD	VDD	VDD
G2	PBD2	PBE2	I/O	L15	PTH2	PTI2	I/O
G3	PBD0	PBE0	I/O	L16	PTH0	PTI0	I/O-D5
G4	PBC2	PBD2	I/O	L17	PTG3	PTH3	I/O
G14	PTC3	PTD3	I/O	M1	PBG2	PBH2	I/O
G15	PTD1	PTE1	I/O	M2	PBI0	PBJ0	I/O-$\overline{\text{LDC}}$
G16	PTD3	PTE3	I/O-D1	M3	PBI2	PBJ2	I/O
G17	PTD2	PTE2	I/O	M4	PBJ0	PBK0	I/O-$\overline{\text{INIT}}$
H1	PBE0	PBF0	I/O	M14	PTI2	PTJ3	I/O
H2	PBD3	PBE3	I/O	M15	See Note	PTJ1	I/O
H3	PBE3	PBF3	I/O	M16	PTH3	PTI3	I/O
H4	PBE1	PBF1	I/O	M17	PTH1	PTI1	I/O
H5	VSS	VSS	VSS	N1	PBH0	PBI0	I/O-HDC
H13	VSS	VSS	VSS	N2	PBH2	PBI2	I/O
H14	PTE0	PTF0	I/O-D2	N3	PBJ1	PBK2	I/O
H15	PTE2	PTF2	I/O	N4	See Note	PBL1	I/O
H16	PTE1	PTF1	I/O	N7	VSS	VSS	VSS
H17	PTE3	PTF3	I/O	N8	VDD	VDD	VDD
J1	PBE2	PBF2	I/O	N9	VSS	VSS	VSS
J2	PBF2	PBG2	I/O	N10	VDD	VDD	VDD
J3	VSS	VSS	VSS	N11	VSS	VSS	VSS
J4	PBF0	PBG0	I/O	N14	PTJ1	PTK3	I/O
J5	VDD	VDD	VDD	N15	See Note	PTK1	I/O
J13	VDD	VDD	VDD	N16	PTI1	PTJ2	I/O
J14	PTF1	PTG1	I/O	N17	PTI0	PTJ0	I/O-D6
J15	VSS	VSS	VSS	P1	PBI1	PBJ1	I/O
J16	PTF3	PTG3	I/O	P2	PBI3	PBJ3	I/O
J17	PTF0	PTG0	I/O-D3	P3	See Note	PBL3	I/O
K1	PBF1	PBG1	I/O	P4	VSS	VSS	VSS
K2	PBF3	PBG3	I/O	P5	PRJ1	PRL3	I/O
K3	PBG1	PBH1	I/O	P6	PRJ3	PRK2	I/O
K4	PBG3	PBH3	I/O	P7	PRI2	PRJ2	I/O
K5	VSS	VSS	VSS	P8	PRG1	PRH1	I/O
K13	VSS	VSS	VSS	P9	PRF2	PRG2	I/O
K14	PTG2	PTH2	I/O	P10	PRE3	PRF3	I/O
K15	PTG0	PTH0	I/O-D4	P11	PRC0	PRD0	I/O-CS1

Note: The ATT1C03 does not have bond pads connected to 225-pin CPGA/PPGA package pin numbers M15, N4, N15, and P3, as well as several other pin numbers identified in this table.

Pin Information (continued)

Table 20. ATT1C03 and ATT1C05 225-Pin CPGA/PPGA Pinout (continued)

Pin	1C03 Pad	1C05 Pad	Function	Pin	1C03 Pad	1C05 Pad	Function
P12	PRB3	PRC3	I/O	T7	PRH3	PRI3	I/O
P13	PRA2	PRB3	I/O	T8	PRG2	PRH2	I/O
P14	Vss	Vss	Vss	T9	PRF0	PRG0	I/O
P15	PTJ2	PTL0	I/O-RDY/RCLK	T10	PRE2	PRF2	I/O
P16	PTJ0	PTK2	I/O	T11	PRD0	PRE0	I/O
P17	PTI3	PTK0	I/O-D7	T12	PRC2	PRD2	I/O
R1	See Note	PBK1	I/O	T13	PRC3	PRD3	I/O
R2	PBJ2	PBK3	I/O	T14	PRB2	PRC2	I/O
R3	DONE	DONE	DONE	T15	PRA1	PRB2	I/O
R4	See Note	PRL1	I/O	T16	See Note	PRA3	I/O
R5	See Note	PRK0	I/O	T17	PTJ3	PTL3	I/O
R6	PRI0	PRJ0	I/O-M1	U1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
R7	PRH1	PRI1	I/O	U2	PRJ0	PRL0	I/O-M0
R8	PRG3	PRH3	I/O	U3	See Note	PRL2	I/O
R9	Vss	Vss	Vss	U4	See Note	PRK3	I/O
R10	PRE1	PRF1	I/O	U5	PRI3	PRJ3	I/O
R11	PRD2	PRE2	I/O	U6	PRH2	PRI2	I/O
R12	PRB1	PRC1	I/O	U7	PRG0	PRH0	I/O-M3
R13	See Note	PRB1	I/O	U8	PRF1	PRG1	I/O
R14	PRA3	PRA0	I/O-$\overline{\text{WR}}$	U9	PRF3	PRG3	I/O
R15	See Note	PRA2	I/O	U10	PRE0	PRF0	I/O
R16	See Note	PTL2	I/O	U11	PRD1	PRE1	I/O
R17	See Note	PTL1	I/O	U12	PRD3	PRE3	I/O
T1	PBJ3	PBL0	I/O	U13	PRC1	PRD1	I/O
T2	See Note	PBL2	I/O	U14	PRB0	PRC0	I/O-$\overline{\text{CS0}}$
T3	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	U15	PRA0	PRB0	I/O-$\overline{\text{RD}}$
T4	PRJ2	PRK1	I/O	U16	See Note	PRA1	I/O
T5	PRI1	PRJ1	I/O	U17	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$
T6	PRH0	PRI0	I/O-M2	—	—	—	—

Note: The ATT1C03 does not have bond pads connected to 225-pin CPGA/PPGA package pin numbers R1, R4, R5, R13, R15, R16, R17, T2, T16, U3, U4, and U16, as well as other pin numbers identified in this table.

Pin Information (continued)

Table 21. ATT1C05, ATT1C07, and ATT1C09 240-Pin SQFP Pinout

Pin	1C05 Pad	1C07 Pad	1C09 Pad	Function
1	VSS	VSS	VSS	VSS
2	VDD	VDD	VDD	VDD
3	PLA3	PLA3	PLA3	I/O
4	PLA2	PLA1	PLA1	I/O
5	PLA1	PLA0	PLA0	I/O
6	PLA0	PLB3	PLB3	I/O-A0
7	VSS	VSS	VSS	VSS
8	PLB3	PLC3	PLC3	I/O
9	PLB2	PLC2	PLC2	I/O
10	PLB1	PLC1	PLC1	I/O
11	PLB0	PLC0	PLC0	I/O-A1
12	PLC3	PLD3	PLD0	I/O-A2
13	PLC2	PLD2	PLE2	I/O
14	PLC1	PLD1	PLE1	I/O
15	PLC0	PLD0	PLE0	I/O-A3
16	VDD	VDD	VDD	VDD
17	PLD3	PLE3	PLF3	I/O
18	PLD2	PLE2	PLF2	I/O
19	PLD1	PLE1	PLF1	I/O
20	PLD0	PLE0	PLF0	I/O-A4
21	PLE3	PLF3	PLG3	I/O-A5
22	PLE2	PLF2	PLG2	I/O
23	PLE1	PLF1	PLG1	I/O
24	PLE0	PLF0	PLG0	I/O-A6
25	VSS	VSS	VSS	VSS
26	PLF3	PLG3	PLH3	I/O
27	PLF2	PLG2	PLH2	I/O
28	PLF1	PLG1	PLH1	I/O
29	PLF0	PLG0	PLH0	I/O-A7
30	VDD	VDD	VDD	VDD
31	PLG3	PLH3	PLI3	I/O
32	PLG2	PLH2	PLI2	I/O
33	PLG1	PLH1	PLI1	I/O
34	PLG0	PLH0	PLI0	I/O-A8
35	VSS	VSS	VSS	VSS
36	PLH3	PLI3	PLJ3	I/O-A9
37	PLH2	PLI2	PLJ2	I/O
38	PLH1	PLI1	PLJ1	I/O
39	PLH0	PLI0	PLJ0	I/O-A10
40	PLI3	PLJ3	PLK3	I/O
41	PLI2	PLJ2	PLK2	I/O
42	PLI1	PLJ1	PLK1	I/O

Note: The ATT1C07 and ATT1C09 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT1C05, ATT1C07, and ATT1C09 240-Pin SQFP Pinout (continued)

Pin	1C05 Pad	1C07 Pad	1C09 Pad	Function
43	PLI0	PLJ0	PLK0	I/O-A11
44	VDD	VDD	VDD	VDD
45	PLJ3	PLK3	PLL3	I/O-A12
46	PLJ2	PLK2	PLL2	I/O
47	PLJ1	PLK1	PLL1	I/O
48	PLJ0	PLK0	PLM3	I/O-A13
49	PLK3	PLL3	PLM1	I/O
50	PLK2	PLL2	PLM0	I/O
51	PLK1	PLL1	PLN3	I/O
52	PLK0	PLL0	PLN2	I/O-A14
53	VSS	VSS	VSS	VSS
54	PLL3	PLM3	PLO3	I/O
55	PLL2	PLM0	PLO0	I/O
56	PLL1	PLN3	PLP3	I/O
57	PLL0	PLN0	PLP0	I/O-A15
58	VSS	VSS	VSS	VSS
59	CCLK	CCLK	CCLK	CCLK
60	VDD	VDD	VDD	VDD
61	VSS	VSS	VSS	VSS
62	VSS	VSS	VSS	VSS
63	PBA0	PBA0	PBA0	I/O-A16
64	PBA1	PBA3	PBA3	I/O
65	PBA2	PBB0	PBB0	I/O
66	PBA3	PBB3	PBB3	I/O
67	VSS	VSS	VSS	VSS
68	PBB0	PBC0	PBC1	I/O-A17
69	PBB1	PBC1	PBD1	I/O
70	PBB2	PBC2	PBD2	I/O
71	PBB3	PBC3	PBD3	I/O
72	PBC0	PBD0	PBE0	I/O
73	PBC1	PBD1	PBE1	I/O
74	PBC2	PBD2	PBE2	I/O
75	PBC3	PBD3	PBE3	I/O
76	VDD	VDD	VDD	VDD
77	PBD0	PBE0	PBF0	I/O
78	PBD1	PBE1	PBF1	I/O
79	PBD2	PBE2	PBF2	I/O
80	PBD3	PBE3	PBF3	I/O
81	PBE0	PBF0	PBG0	I/O
82	PBE1	PBF1	PBG1	I/O
83	PBE2	PBF2	PBG2	I/O
84	PBE3	PBF3	PBG3	I/O

Note: The ATT1C07 and ATT1C09 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT1C05, ATT1C07, and ATT1C09 240-Pin SQFP Pinout (continued)

Pin	1C05 Pad	1C07 Pad	1C09 Pad	Function
85	VSS	VSS	VSS	VSS
86	PBF0	PBG0	PBH0	I/O
87	PBF1	PBG1	PBH1	I/O
88	PBF2	PBG2	PBH2	I/O
89	PBF3	PBG3	PBH3	I/O
90	VSS	VSS	VSS	VSS
91	PBG0	PBH0	PBI0	I/O
92	PBG1	PBH1	PBI1	I/O
93	PBG2	PBH2	PBI2	I/O
94	PBG3	PBH3	PBI3	I/O
95	VSS	VSS	VSS	VSS
96	PBH0	PBI0	PBJ0	I/O
97	PBH1	PBI1	PBJ1	I/O
98	PBH2	PBI2	PBJ2	I/O
99	PBH3	PBI3	PBJ3	I/O
100	PBI0	PBJ0	PBK0	I/O-HDC
101	PBI1	PBJ1	PBK1	I/O
102	PBI2	PBJ2	PBK2	I/O
103	PBI3	PBJ3	PBK3	I/O
104	VDD	VDD	VDD	VDD
105	PBJ0	PBK0	PBL0	I/O-$\overline{\text{LDC}}$
106	PBJ1	PBK3	PBM0	I/O
107	PBJ2	PBL0	PBM1	I/O
108	PBJ3	PBL1	PBM2	I/O
109	PBK0	PBL2	PBM3	I/O-$\overline{\text{INIT}}$
110	PBK1	PBL3	PBN0	I/O
111	PBK2	PBM0	PBO0	I/O
112	PBK3	PBM1	PBO1	I/O
113	VSS	See Note	See Note	VSS
114	PBL0	PBM3	PBO3	I/O
115	PBL1	PBN0	PBP0	I/O
116	PBL2	PBN1	PBP1	I/O
117	PBL3	PBN3	PBP3	I/O
118	VSS	VSS	VSS	VSS
119	DONE	DONE	DONE	DONE
120	VDD	VDD	VDD	VDD
121	VSS	VSS	VSS	VSS
122	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
123	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
124	PRL0	PRN0	PRP0	I/O-M0
125	PRL1	PRN3	PRP3	I/O
126	PRL2	PRM0	PRO0	I/O

Note: The ATT1C07 and ATT1C09 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT1C05, ATT1C07, and ATT1C09 240-Pin SQFP Pinout (continued)

Pin	1C05 Pad	1C07 Pad	1C09 Pad	Function
127	PRL3	PRM3	PRO3	I/O
128	VSS	VSS	VSS	VSS
129	PRK0	PRL0	PRN0	I/O
130	PRK1	PRL1	PRN2	I/O
131	PRK2	PRL2	PRN3	I/O
132	PRK3	PRL3	PRM0	I/O
133	PRJ0	PRK0	PRM1	I/O-M1
134	PRJ1	PRK1	PRM2	I/O
135	PRJ2	PRK2	PRL0	I/O
136	PRJ3	PRK3	PRL1	I/O
137	VDD	VDD	VDD	VDD
138	PRI0	PRJ0	PRK0	I/O-M2
139	PRI1	PRJ1	PRK1	I/O
140	PRI2	PRJ2	PRK2	I/O
141	PRI3	PRJ3	PRK3	I/O
142	PRH0	PRI0	PRJ0	I/O-M3
143	PRH1	PRI1	PRJ1	I/O
144	PRH2	PRI2	PRJ2	I/O
145	PRH3	PRI3	PRJ3	I/O
146	VSS	VSS	VSS	VSS
147	PRG0	PRH0	PRI0	I/O
148	PRG1	PRH1	PRI1	I/O
149	PRG2	PRH2	PRI2	I/O
150	PRG3	PRH3	PRI3	I/O
151	VDD	VDD	VDD	VDD
152	PRF0	PRG0	PRH0	I/O
153	PRF1	PRG1	PRH1	I/O
154	PRF2	PRG2	PRH2	I/O
155	PRF3	PRG3	PRH3	I/O
156	VSS	VSS	VSS	VSS
157	PRE0	PRF0	PRG0	I/O
158	PRE1	PRF1	PRG1	I/O
159	PRE2	PRF2	PRG2	I/O
160	PRE3	PRF3	PRG3	I/O
161	PRD0	PRE0	PRF0	I/O-CS1
162	PRD1	PRE1	PRF1	I/O
163	PRD2	PRE2	PRF2	I/O
164	PRD3	PRE3	PRF3	I/O
165	VDD	VDD	VDD	VDD
166	PRC0	PRD0	PRE0	I/O-$\overline{CS0}$
167	PRC1	PRD1	PRD1	I/O
168	PRC2	PRD2	PRD2	I/O

Note: The ATT1C07 and ATT1C09 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT1C05, ATT1C07, and ATT1C09 240-Pin SQFP Pinout (continued)

Pin	1C05 Pad	1C07 Pad	1C09 Pad	Function
169	PRC3	PRD3	PRD3	I/O
170	PRB0	PRC0	PRC0	I/O-$\overline{RD}$
171	PRB1	PRC1	PRC1	I/O
172	PRB2	PRC2	PRC2	I/O
173	PRB3	PRC3	PRC3	I/O
174	VSS	VSS	VSS	VSS
175	PRA0	PRB0	PRB0	I/O-$\overline{WR}$
176	PRA1	PRB3	PRB3	I/O
177	PRA2	PRA0	PRA0	I/O
178	PRA3	PRA3	PRA3	I/O
179	VSS	VSS	VSS	VSS
180	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
181	VSS	VSS	VSS	VSS
182	VDD	VDD	VDD	VDD
183	VSS	VSS	VSS	VSS
184	PTL3	PTN3	PTP3	I/O
185	PTL2	PTN2	PTP2	I/O
186	PTL1	PTN0	PTP0	I/O
187	PTL0	PTM3	PTO3	I/O-RDY/RCLK
188	VSS	See Note	See Note	VSS
189	PTK3	PTM1	PTO1	I/O
190	PTK2	PTM0	PTO0	I/O
191	PTK1	PTL3	PTN3	I/O
192	PTK0	PTL2	PTM3	I/O-D7
193	PTJ3	PTL0	PTM1	I/O
194	PTJ2	PTK3	PTM0	I/O
195	PTJ1	PTK2	PTL3	I/O
196	PTJ0	PTK1	PTL1	I/O-D6
197	VDD	VDD	VDD	VDD
198	PTI3	PTJ3	PTK3	I/O
199	PTI2	PTJ2	PTK2	I/O
200	PTI1	PTJ1	PTK1	I/O
201	PTI0	PTJ0	PTK0	I/O-D5
202	PTH3	PTI3	PTJ3	I/O
203	PTH2	PTI2	PTJ2	I/O
204	PTH1	PTI1	PTJ1	I/O
205	PTH0	PTI0	PTJ0	I/O-D4
206	VSS	VSS	VSS	VSS
207	PTG3	PTH3	PTI3	I/O
208	PTG2	PTH2	PTI2	I/O
209	PTG1	PTH1	PTI1	I/O
210	PTG0	PTH0	PTI0	I/O-D3

Note: The ATT1C07 and ATT1C09 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 21. ATT1C05, ATT1C07, and ATT1C09 240-Pin SQFP Pinout (continued)

Pin	1C05 Pad	1C07 Pad	1C09 Pad	Function
211	VSS	VSS	VSS	VSS
212	PTF3	PTG3	PTH3	I/O
213	PTF2	PTG2	PTH2	I/O
214	PTF1	PTG1	PTH1	I/O
215	PTF0	PTG0	PTH0	I/O-D2
216	VSS	VSS	VSS	VSS
217	PTE3	PTF3	PTG3	I/O-D1
218	PTE2	PTF2	PTG2	I/O
219	PTE1	PTF1	PTG1	I/O
220	PTE0	PTF0	PTG0	I/O-D0/DIN
221	PTD3	PTE3	PTF3	I/O
222	PTD2	PTE2	PTF2	I/O
223	PTD1	PTE1	PTF1	I/O
224	PTD0	PTE0	PTF0	I/O-DOUT
225	VDD	VDD	VDD	VDD
226	PTC3	PTD3	PTE3	I/O
227	PTC2	PTD2	PTE0	I/O
228	PTC1	PTD1	PTD3	I/O
229	PTC0	PTD0	PTD0	I/O-TDI
230	PTB3	PTC3	PTC3	I/O
231	PTB2	PTC2	PTC2	I/O
232	PTB1	PTC1	PTC1	I/O
233	PTB0	PTC0	PTC0	I/O-TMS
234	VSS	VSS	VSS	VSS
235	PTA3	PTB3	PTB3	I/O
236	PTA2	PTB0	PTB0	I/O
237	PTA1	PTA3	PTA3	I/O
238	PTA0	PTA0	PTA0	I/O-TCK
239	VSS	VSS	VSS	VSS
240	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO

Note: The ATT1C07 and ATT1C09 do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

Pin Information (continued)

Table 22. ATT1C07 280-Pin CPGA Pinout

Pin	1C07 Pad	Function	Pin	1C07 Pad	Function
A1	See Note	No Connect	C5	PLL2	I/O
A2	See Note	No Connect	C6	PLK2	I/O
A3	PLN2	I/O	C7	PLJ1	I/O
A4	PLM2	I/O	C8	PLJ3	I/O
A5	PLL3	I/O	C9	PLH2	I/O
A6	PLK3	I/O-A12	C10	PLH3	I/O
A7	PLJ2	I/O	C11	PLG1	I/O
A8	PLI0	I/O-A10	C12	PLE0	I/O-A4
A9	PLH1	I/O	C13	PLE2	I/O
A10	See Note	No Connect	C14	PLD1	I/O
A11	PLG2	I/O	C15	PLC1	I/O
A12	PLF3	I/O-A5	C16	PLB2	I/O
A13	PLE1	I/O	C17	Vss	Vss
A14	PLD0	I/O-A3	C18	PTA0	I/O-TCK
A15	PLC0	I/O-A1	C19	PTA2	I/O
A16	PLB1	I/O	D1	PBB2	I/O
A17	PLA1	I/O	D2	PBB0	I/O
A18	See Note	No Connect	D3	PBB1	I/O
A19	See Note	No Connect	D4	Vss	Vss
B1	See Note	No Connect	D5	PLN1	I/O
B2	CCLK	CCLK	D6	PLM3	I/O
B3	PLN0	I/O-A15	D7	PLK0	I/O-A13
B4	PLM0	I/O	D8	VDD	VDD
B5	PLL1	I/O	D9	PLI3	I/O-A9
B6	PLK1	I/O	D10	VDD	VDD
B7	PLJ0	I/O-A11	D11	PLF0	I/O-A6
B8	PLH0	I/O-A8	D12	VDD	VDD
B9	PLI2	I/O	D13	PLD3	I/O-A2
B10	PLG0	I/O-A7	D14	PLB0	I/O
B11	PLF1	I/O	D15	PLA2	I/O
B12	PLG3	I/O	D16	Vss	Vss
B13	PLE3	I/O	D17	PTB1	I/O
B14	PLD2	I/O	D18	PTB0	I/O
B15	PLC2	I/O	D19	PTB2	I/O
B16	PLB3	I/O-A0	E1	PBC3	I/O
B17	PLA3	I/O	E2	PBC1	I/O
B18	RD_DATA/TDO	RD_DATA/TDO	E3	PBC2	I/O
B19	See Note	No Connect	E4	PBA1	I/O
C1	PBA2	I/O	E5	VDD	VDD
C2	PBA0	I/O-A16	E6	PLN3	I/O
C3	Vss	Vss	E7	PLL0	I/O-A14
C4	PLM1	I/O	E8	Vss	Vss

Note: The ATT1C07 does not have bond pads connected to 280-pin CPGA package pin numbers A1, A2, A10, A18, A19, B1, and B19, as well as other pin numbers identified in this table.

Pin Information (continued)

Table 22. ATT1C07 280-Pin CPGA Pinout (continued)

Pin	1C07 Pad	Function	Pin	1C07 Pad	Function
E9	PLI1	I/O	J2	PBF2	I/O
E10	VSS	VSS	J3	PBG2	I/O
E11	PLF2	I/O	J4	PBF3	I/O
E12	VSS	VSS	J5	PBF1	I/O
E13	PLC3	I/O	J15	PTF1	I/O
E14	PLA0	I/O	J16	PTF3	I/O-D1
E15	VDD	VDD	J17	PTG2	I/O
E16	PTA1	I/O	J18	PTF2	I/O
E17	PTC2	I/O	J19	PTG1	I/O
E18	PTC1	I/O	K1	See Note	No Connect
E19	PTC3	I/O	K2	PBG3	I/O
F1	PBD3	I/O	K3	PBH0	I/O
F2	PBD1	I/O	K4	VDD	VDD
F3	PBD2	I/O	K5	VSS	VSS
F4	PBB3	I/O	K15	VSS	VSS
F5	PBA3	I/O	K16	VDD	VDD
F6	See Note	No Connect	K17	PTG3	I/O
F15	PTA3	I/O	K18	PTH0	I/O-D3
F16	PTB3	I/O	K19	See Note	No Connect
F17	PTD2	I/O	L1	PBH2	I/O
F18	PTD1	I/O	L2	PBI1	I/O
F19	PTD3	I/O	L3	PBH1	I/O
G1	PBE2	I/O	L4	PBI0	I/O
G2	PBE0	I/O	L5	PBI2	I/O
G3	PBE1	I/O	L15	PTI2	I/O
G4	PBD0	I/O	L16	PTI0	I/O-D4
G5	PBC0	I/O-A17	L17	PTH1	I/O
G15	PTC0	I/O-TMS	L18	PTI1	I/O
G16	PTD0	I/O-TDI	L19	PTH2	I/O
G17	PTE1	I/O	M1	PBI3	I/O
G18	PTE0	I/O-DOUT	M2	PBH3	I/O
G19	PTE2	I/O	M3	PBJ0	I/O-HDC
H1	PBF0	I/O	M4	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
H2	PBG0	I/O	M5	VSS	VSS
H3	PBE3	I/O	M15	VSS	VSS
H4	VDD	VDD	M16	VDD	VDD
H5	VSS	VSS	M17	PTJ0	I/O-D5
H15	VSS	VSS	M18	PTH3	I/O
H16	See Note	No Connect	M19	PTI3	I/O
H17	PTE3	I/O	N1	PBJ1	I/O
H18	PTG0	I/O-D2	N2	PBJ3	I/O
H19	PTF0	I/O-D0/DIN	N3	PBJ2	I/O
J1	PBG1	I/O	N4	PBK3	I/O

Note: The ATT1C07 does not have bond pads connected to 280-pin CPGA package pin numbers F6, H16, K1, and K19, as well as other pin numbers identified in this table.

Pin Information (continued)

Table 22. ATT1C07 280-Pin CPGA Pinout (continued)

Pin	1C07 Pad	Function	Pin	1C07 Pad	Function
N5	PBL3	I/O	T8	VDD	VDD
N15	PTL3	I/O	T9	PRI1	I/O
N16	PTK3	I/O	T10	VDD	VDD
N17	PTJ2	I/O	T11	PRF0	I/O
N18	PTJ3	I/O	T12	VDD	VDD
N19	PTJ1	I/O	T13	PRD3	I/O
P1	PBK0	I/O-$\overline{LDC}$	T14	PRB0	I/O-$\overline{WR}$
P2	PBK2	I/O	T15	PRA2	I/O
P3	PBK1	I/O	T16	VSS	VSS
P4	PBM0	I/O	T17	PTM2	I/O
P5	PBN0	I/O	T18	PTM3	I/O-RDY/RCLK
P15	PTN0	I/O	T19	PTM1	I/O
P16	PTM0	I/O	U1	PBN1	I/O
P17	PTK1	I/O-D6	U2	PBN3	I/O
P18	PTK2	I/O	U3	VSS	VSS
P19	PTK0	I/O	U4	PRM1	I/O
R1	PBL0	I/O	U5	PRL0	I/O
R2	PBL2	I/O-$\overline{INIT}$	U6	PRK0	I/O-M1
R3	PBL1	I/O	U7	PRK2	I/O
R4	PBN2	I/O	U8	PRJ1	I/O
R5	VDD	VDD	U9	PRH0	I/O
R6	PRN3	I/O	U10	PRG0	I/O
R7	$\overline{RESET}$	$\overline{RESET}$	U11	PRG1	I/O
R8	VSS	VSS	U12	PRE0	I/O-CS1
R9	PRJ3	I/O	U13	PRE2	I/O
R10	VSS	VSS	U14	PRD1	I/O
R11	PRF2	I/O	U15	PRC1	I/O
R12	VSS	VSS	U16	PRB2	I/O
R13	PRC3	I/O	U17	VSS	VSS
R14	PRA0	I/O	U18	PTN3	I/O
R15	VDD	VDD	U19	PTN1	I/O
R16	PTN2	I/O	V1	See Note	No Connect
R17	PTL1	I/O	V2	DONE	DONE
R18	PTL2	I/O-D7	V3	PRN0	I/O-M0
R19	PTL0	I/O	V4	PRM0	I/O
T1	PBM1	I/O	V5	PRL1	I/O
T2	PBM3	I/O	V6	PRK1	I/O
T3	PBM2	I/O	V7	PRJ0	I/O-M2
T4	VSS	VSS	V8	PRI3	I/O
T5	PRN1	I/O	V9	PRI2	I/O
T6	PRM3	I/O	V10	PRH3	I/O
T7	PRL2	I/O	V11	PRF1	I/O

Note: The ATT1C07 does not have a bond pad connected to 280-pin CPGA package pin number V1, as well as other pin numbers identified in this table.

Pin Information (continued)

Table 22. ATT1C07 280-Pin CPGA Pinout (continued)

Pin	1C07 Pad	Function	Pin	1C07 Pad	Function
V12	PRG3	I/O	W7	PRJ2	I/O
V13	PRE3	I/O	W8	PRI0	I/O-M3
V14	PRD2	I/O	W9	PRH1	I/O
V15	PRC2	I/O	W10	PRH2	I/O
V16	PRB3	I/O	W11	PRG2	I/O
V17	PRA3	I/O	W12	PRF3	I/O
V18	$\overline{\text{RD\_CFGN}}$	$\overline{\text{RD\_CFGN}}$	W13	PRE1	I/O
V19	See Note	No Connect	W14	PRD0	I/O-$\overline{\text{CS0}}$
W1	See Note	No Connect	W15	PRC0	I/O-$\overline{\text{RD}}$
W2	See Note	No Connect	W16	PRB1	I/O
W3	PRN2	I/O	W17	PRA1	I/O
W4	PRM2	I/O	W18	See Note	No Connect
W5	PRL3	I/O	W19	See Note	No Connect
W6	PRK3	I/O	—	—	—

Note: The ATT1C07 does not have bond pads connected to 280-pin CPGA package pin numbers V19, W1, W2, W18, and W19, as well as other pin numbers identified in this table.

Pin Information (continued)

Table 23. ATT1C07 and ATT1C09 304-Pin SQFP Pinout

Pin	1C07 Pad	1C09 Pad	Function	Pin	1C07 Pad	1C09 Pad	Function
1	VSS	VSS	VSS	43	PLH0	PLI0	I/O-A8
2	VDD	VDD	VDD	44	VSS	VSS	VSS
3	VSS	VSS	VSS	45	PLI3	PLJ3	I/O-A9
4	PLA3	PLA3	I/O	46	PLI2	PLJ2	I/O
5	PLA2	PLA2	I/O	47	PLI1	PLJ1	I/O
6	PLA1	PLA1	I/O	48	PLI0	PLJ0	I/O-A10
7	PLA0	PLA0	I/O	49	PLJ3	PLK3	I/O
8	PLB3	PLB3	I/O-A0	50	PLJ2	PLK2	I/O
9	PLB2	PLB2	I/O	51	PLJ1	PLK1	I/O
10	PLB1	PLB1	I/O	52	PLJ0	PLK0	I/O-A11
11	PLB0	PLB0	I/O	53	VDD	VDD	VDD
12	VSS	VSS	VSS	54	PLK3	PLL3	I/O-A12
13	PLC3	PLC3	I/O	55	PLK2	PLL2	I/O
14	PLC2	PLC2	I/O	56	PLK1	PLL1	I/O
15	PLC1	PLC1	I/O	57	See Note	PLL0	I/O
16	PLC0	PLC0	I/O-A1	58	PLK0	PLM3	I/O-A13
17	See Note	PLD3	I/O	59	See Note	PLM2	I/O
18	See Note	PLD2	I/O	60	PLL3	PLM1	I/O
19	See Note	PLD1	I/O	61	PLL2	PLM0	I/O
20	PLD3	PLD0	I/O-A2	62	PLL1	PLN3	I/O
21	See Note	PLE3	I/O	63	PLL0	PLN2	I/O-A14
22	PLD2	PLE2	I/O	64	See Note	PLN0	I/O
23	PLD1	PLE1	I/O	65	VSS	VSS	VSS
24	PLD0	PLE0	I/O-A3	66	PLM3	PLO3	I/O
25	VDD	VDD	VDD	67	PLM2	PLO2	I/O
26	PLE3	PLF3	I/O	68	PLM1	PLO1	I/O
27	PLE2	PLF2	I/O	69	PLM0	PLO0	I/O
28	PLE1	PLF1	I/O	70	PLN3	PLP3	I/O
29	PLE0	PLF0	I/O-A4	71	PLN2	PLP2	I/O
30	PLF3	PLG3	I/O-A5	72	PLN1	PLP1	I/O
31	PLF2	PLG2	I/O	73	PLN0	PLP0	I/O-A15
32	PLF1	PLG1	I/O	74	VSS	VSS	VSS
33	PLF0	PLG0	I/O-A6	75	CCLK	CCLK	CCLK
34	VSS	VSS	VSS	76	VDD	VDD	VDD
35	PLG3	PLH3	I/O	77	VSS	VSS	VSS
36	PLG2	PLH2	I/O	78	VDD	VDD	VDD
37	PLG1	PLH1	I/O	79	VSS	VSS	VSS
38	PLG0	PLH0	I/O-A7	80	PBA0	PBA0	I/O-A16
39	VDD	VDD	VDD	81	PBA1	PBA1	I/O
40	PLH3	PLI3	I/O	82	PBA2	PBA2	I/O
41	PLH2	PLI2	I/O	83	PBA3	PBA3	I/O
42	PLH1	PLI1	I/O	84	PBB0	PBB0	I/O

Note: The ATT1C07 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT1C07 and ATT1C09 304-Pin SQFP Pinout (continued)

Pin	1C07 Pad	1C09 Pad	Function	Pin	1C07 Pad	1C09 Pad	Function
85	PBB1	PBB1	I/O	127	PBJ2	PBK2	I/O
86	PBB2	PBB2	I/O	128	PBJ3	PBK3	I/O
87	PBB3	PBB3	I/O	129	VDD	VDD	VDD
88	VSS	VSS	VSS	130	PBK0	PBL0	I/O-$\overline{LDC}$
89	See Note	PBC0	I/O	131	See Note	PBL1	I/O
90	PBC0	PBC1	I/O-A17	132	PBK1	PBL2	I/O
91	See Note	PBC2	I/O	133	PBK2	PBL3	I/O
92	See Note	PBC3	I/O	134	PBK3	PBM0	I/O
93	See Note	PBD0	I/O	135	PBL0	PBM1	I/O
94	PBC1	PBD1	I/O	136	PBL1	PBM2	I/O
95	PBC2	PBD2	I/O	137	PBL2	PBM3	I/O-$\overline{INIT}$
96	PBC3	PBD3	I/O	138	See Note	PBN0	I/O
97	PBD0	PBE0	I/O	139	PBL3	PBN1	I/O
98	PBD1	PBE1	I/O	140	See Note	PBN3	I/O
99	PBD2	PBE2	I/O	141	VSS	VSS	VSS
100	PBD3	PBE3	I/O	142	PBM0	PBO0	I/O
101	VDD	VDD	VDD	143	PBM1	PBO1	I/O
102	PBE0	PBF0	I/O	144	PBM2	PBO2	I/O
103	PBE1	PBF1	I/O	145	PBM3	PBO3	I/O
104	PBE2	PBF2	I/O	146	PBN0	PBP0	I/O
105	PBE3	PBF3	I/O	147	PBN1	PBP1	I/O
106	PBF0	PBG0	I/O	148	PBN2	PBP2	I/O
107	PBF1	PBG1	I/O	149	PBN3	PBP3	I/O
108	PBF2	PBG2	I/O	150	VSS	VSS	VSS
109	PBF3	PBG3	I/O	151	DONE	DONE	DONE
110	VSS	VSS	VSS	152	VDD	VDD	VDD
111	PBG0	PBH0	I/O	153	VSS	VSS	VSS
112	PBG1	PBH1	I/O	154	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$
113	PBG2	PBH2	I/O	155	$\overline{PRGM}$	$\overline{PRGM}$	$\overline{PRGM}$
114	PBG3	PBH3	I/O	156	PRN0	PRP0	I/O-M0
115	VSS	VSS	VSS	157	PRN1	PRP1	I/O
116	PBH0	PBI0	I/O	158	PRN2	PRP2	I/O
117	PBH1	PBI1	I/O	159	PRN3	PRP3	I/O
118	PBH2	PBI2	I/O	160	PRM0	PRO0	I/O
119	PBH3	PBI3	I/O	161	PRM1	PRO1	I/O
120	VSS	VSS	VSS	162	PRM2	PRO2	I/O
121	PBI0	PBJ0	I/O	163	PRM3	PRO3	I/O
122	PBI1	PBJ1	I/O	164	VSS	VSS	VSS
123	PBI2	PBJ2	I/O	165	PRL0	PRN0	I/O
124	PBI3	PBJ3	I/O	166	PRL1	PRN2	I/O
125	PBJ0	PBK0	I/O-HDC	167	PRL2	PRN3	I/O
126	PBJ1	PBK1	I/O	168	PRL3	PRM0	I/O

Note: The ATT1C07 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT1C07 and ATT1C09 304-Pin SQFP Pinout (continued)

Pin	1C07 Pad	1C09 Pad	Function	Pin	1C07 Pad	1C09 Pad	Function
169	PRK0	PRM1	I/O-M1	211	PRD2	PRD2	I/O
170	PRK1	PRM2	I/O	212	PRD3	PRD3	I/O
171	See Note	PRM3	I/O	213	PRC0	PRC0	I/O-$\overline{RD}$
172	PRK2	PRL0	I/O	214	PRC1	PRC1	I/O
173	PRK3	PRL1	I/O	215	PRC2	PRC2	I/O
174	See Note	PRL2	I/O	216	PRC3	PRC3	I/O
175	See Note	PRL3	I/O	217	VSS	VSS	VSS
176	VDD	VDD	VDD	218	PRB0	PRB0	I/O-$\overline{WR}$
177	PRJ0	PRK0	I/O-M2	219	PRB1	PRB1	I/O
178	PRJ1	PRK1	I/O	220	PRB2	PRB2	I/O
179	PRJ2	PRK2	I/O	221	PRB3	PRB3	I/O
180	PRJ3	PRK3	I/O	222	PRA0	PRA0	I/O
181	PRI0	PRJ0	I/O-M3	223	PRA1	PRA1	I/O
182	PRI1	PRJ1	I/O	224	PRA2	PRA2	I/O
183	PRI2	PRJ2	I/O	225	PRA3	PRA3	I/O
184	PRI3	PRJ3	I/O	226	VSS	VSS	VSS
185	VSS	VSS	VSS	227	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
186	PRH0	PRI0	I/O	228	VDD	VDD	VDD
187	PRH1	PRI1	I/O	229	VSS	VSS	VSS
188	PRH2	PRI2	I/O	230	VDD	VDD	VDD
189	PRH3	PRI3	I/O	231	VSS	VSS	VSS
190	VDD	VDD	VDD	232	PTN3	PTP3	I/O
191	PRG0	PRH0	I/O	233	PTN2	PTP2	I/O
192	PRG1	PRH1	I/O	234	PTN1	PTP1	I/O
193	PRG2	PRH2	I/O	235	PTN0	PTP0	I/O
194	PRG3	PRH3	I/O	236	PTM3	PTO3	I/O-RDY/RCLK
195	VSS	VSS	VSS	237	PTM2	PTO2	I/O
196	PRF0	PRG0	I/O	238	PTM1	PTO1	I/O
197	PRF1	PRG1	I/O	239	PTM0	PTO0	I/O
198	PRF2	PRG2	I/O	240	VSS	VSS	VSS
199	PRF3	PRG3	I/O	241	PTL3	PTN3	I/O
200	PRE0	PRF0	I/O-CS1	242	See Note	PTN1	I/O
201	PRE1	PRF1	I/O	243	See Note	PTN0	I/O
202	PRE2	PRF2	I/O	244	PTL2	PTM3	I/O-D7
203	PRE3	PRF3	I/O	245	PTL1	PTM2	I/O
204	VDD	VDD	VDD	246	PTL0	PTM1	I/O
205	PRD0	PRE0	I/O-$\overline{CS0}$	247	PTK3	PTM0	I/O
206	See Note	PRE1	I/O	248	PTK2	PTL3	I/O
207	See Note	PRE2	I/O	249	See Note	PTL2	I/O
208	See Note	PRE3	I/O	250	PTK1	PTL1	I/O-D6
209	See Note	PRD0	I/O	251	PTK0	PTL0	I/O
210	PRD1	PRD1	I/O	252	VDD	VDD	VDD

Note: The ATT1C07 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Pin Information (continued)

Table 23. ATT1C07 and ATT1C09 304-Pin SQFP Pinout (continued)

Pin	1C07 Pad	1C09 Pad	Function	Pin	1C07 Pad	1C09 Pad	Function
253	PTJ3	PTK3	I/O	279	PTE0	PTF0	I/O-DOUT
254	PTJ2	PTK2	I/O	280	VDD	VDD	VDD
255	PTJ1	PTK1	I/O	281	PTD3	PTE3	I/O
256	PTJ0	PTK0	I/O-D5	282	See Note	PTE2	I/O
257	PTI3	PTJ3	I/O	283	See Note	PTE1	I/O
258	PTI2	PTJ2	I/O	284	PTD2	PTE0	I/O
259	PTI1	PTJ1	I/O	285	PTD1	PTD3	I/O
260	PTI0	PTJ0	I/O-D4	286	See Note	PTD2	I/O
261	VSS	VSS	VSS	287	See Note	PTD1	I/O
262	PTH3	PTI3	I/O	288	PTD0	PTD0	I/O-TDI
263	PTH2	PTI2	I/O	289	PTC3	PTC3	I/O
264	PTH1	PTI1	I/O	290	PTC2	PTC2	I/O
265	PTH0	PTI0	I/O-D3	291	PTC1	PTC1	I/O
266	VSS	VSS	VSS	292	PTC0	PTC0	I/O-TMS
267	PTG3	PTH3	I/O	293	VSS	VSS	VSS
268	PTG2	PTH2	I/O	294	PTB3	PTB3	I/O
269	PTG1	PTH1	I/O	295	PTB2	PTB2	I/O
270	PTG0	PTH0	I/O-D2	296	PTB1	PTB1	I/O
271	VSS	VSS	VSS	297	PTB0	PTB0	I/O
272	PTF3	PTG3	I/O-D1	298	PTA3	PTA3	I/O
273	PTF2	PTG2	I/O	299	PTA2	PTA2	I/O
274	PTF1	PTG1	I/O	300	PTA1	PTA1	I/O
275	PTF0	PTG0	I/O-D0/DIN	301	PTA0	PTA0	I/O-TCK
276	PTE3	PTF3	I/O	302	VSS	VSS	VSS
277	PTE2	PTF2	I/O	303	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO
278	PTE1	PTF1	I/O	304	VDD	VDD	VDD

Note: The ATT1C07 does not have bond pads connected to 304-pin SQFP package pin numbers 17, 18, 19, 21, 57, 59, 64, 89, 91—93, 131, 138, 140, 171, 174, 175, 206—209, 242, 243, 249, 282, 283, 286, and 287.

Package Thermal Characteristics

When silicon die junction temperature is below the recommended junction temperature of 125 °C, the temperature-activated failure mechanisms are minimized. There are four major factors that affect the thermal resistance value: silicon device size/paddle size, board mounting configuration (board density, multilayer nature of board), package type and size, and system airflow over the package. The values in the tables below reflect the capability of the various package types to dissipate heat at given airflow rates. The numbers represent the delta °C/W between the ambient temperature and the device junction temperature.

To test package thermal characteristics, a single package containing a 0.269 in. sq. test IC of each configuration is mounted at the center of a printed-circuit board (PCB) measuring 8 in. x 13 in. x 0.062 in. The assembled PCB is mounted vertically in the center of the rectangular test section of a wind tunnel. The walls of the wind tunnel simulate adjacent boards in the electronic rack and can be adjusted to study the effects of PCB spacing. Forced air at room temperature is supplied by a pair of push-pull blowers which can be regulated to supply the desired air velocities. The air velocity is measured with a hot-wire anemometer at the center of the channel, 3 in. upstream from the package.

A typical test consists of regulating the wind tunnel blowers to obtain the desired air velocity and applying power to the test IC. The power to the IC is adjusted until the maximum junction temperature (as measured by its diodes) reaches 115 °C to 120 °C. The thermal resistance Θ_{JA} (°C/W) is computed by using the power supplied to the IC, junction temperature, ambient temperature, and air velocity.

$$\Theta_{JA} = \frac{T_J - T_A}{Q_C}$$

where:

T_J = peak temperature on the active surface of the IC.

T_A = ambient air temperature.

Q_C = IC power.

The tests are repeated at several velocities from 0 fpm (feet per minute) to 1000 fpm.

The junction to case thermal resistance Θ_{JC} is:

$$\Theta_{JC} = \frac{T_J - T_C}{Q_C}$$

where:

T_C = temperature measured to the thermocouple at the top dead center of the package.

The actual Θ_{JC} measurement performed at AT&T, Θ_{J-TDC}, uses a different package mounting arrangement than the one defined for Θ_{JC} in MIL-STD-883D and SEMI standards. Please contact AT&T for a diagram.

The maximum power dissipation for a package is calculated from the maximum junction temperature, maximum operating temperature, and the junction to ambient characteristic Θ_{JA}. The maximum power dissipation for commercial grade ICs is calculated as follows: max power (W) = (125 °C – 70 °C) x ($1/\Theta_{JA}$), where 125 °C is the maximum junction temperature. Table 24 lists the plastic *ORCA* package thermal characteristics, and Table 25 reflects the thermal characteristics found in the *ORCA* ceramic packages.

Package Thermal Characteristics (continued)

Table 24. *ORCA* Plastic Package Thermal Characteristics

Package	ΘJA (°C/W)			ΘJC (°C/W)	Max Power (70 °C—0 fpm)
	0 fpm	200 fpm	400 fpm		
84-Pin PLCC	40	35	32	9	1.38 W
100-Pin TQFP	61	49	46	6	0.9 W
132-Pin BQFP	42	33	29	9	1.30 W
144-Pin TQFP	52	39	36	4	1.05 W
208-Pin SQFP	37	33	29	8	1.49 W
225-Pin PPGA	35	31	28	—	1.57 W
240-Pin SQFP	35	31	28	7	1.57 W
304-Pin SQFP	33	30	27	6	1.67 W

Table 25. *ORCA* Ceramic Package Thermal Characteristics

Package	ΘJA (°C/W)			ΘJC (°C/W)	Max Power (70 °C—0 fpm)
	0 fpm	200 fpm	400 fpm		
225-Pin CPGA	19	16	14	2.3	2.90 W
280-Pin CPGA	18	16	14	2.3	3.05 W

Package Coplanarity

The coplanarity of AT&T postmolded packages is 4 mils. The coplanarity of selected packages is scheduled to be reduced to 3.1 mils. All AT&T *ORCA* Series FPGA ceramic packages are through-hole mount.

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 26 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_W and L_L, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead, and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead.

The parasitic values in Table 26 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C1 and C2 capacitors. The PGAs contain power and ground planes that will make the inductance value for power and ground leads the minimum value listed. The PGAs also have a significant range of parasitic values. This is due to the large variation in internal trace lengths and is also due to two signal metal layers that are separated from the ground plane by different distances. The upper signal layer is more inductive but less capacitive than the closer, lower signal layer.

Package Parasitics (continued)

Table 26. Package Parasitics

Package Type	Lw	Mw	Rw	C1	C2	CM	LL	ML
84-Pin PLCC	3	1	160	1	1	0.5	7—11	3—6
100-Pin TQFP	3	1	160	0.7	0.7	0.4	3—4	1.5—2
132-Pin BQFP	3.5	1.5	175	0.8	0.8	0.5	5—8	2—3
144-Pin TQFP	3.5	1.5	175	1	1	0.6	4—6	2—2.5
208-Pin SQFP	4	2	200	1	1	1	7—10	4—6
225-Pin CPGA	2	1	800	1—2.5	1—2.5	0.2—0.6	2—12*	1—4
225-Pin PPGA	2	1	150	0.5—1	0.5—1	0.1—0.3	2—12*	1—4
240-Pin SQFP	4	2	200	2	2	1	8—12	5—8
280-Pin CPGA	2	1	1200	1—2.5	1—2.5	0.5—1	2—15*	1—5
304-Pin SQFP	5	2	200	1	1	1	12—18	7—12

* Leads designated as ground (power) can be connected to the ground plane, reducing the trace inductance to the minimum value listed.

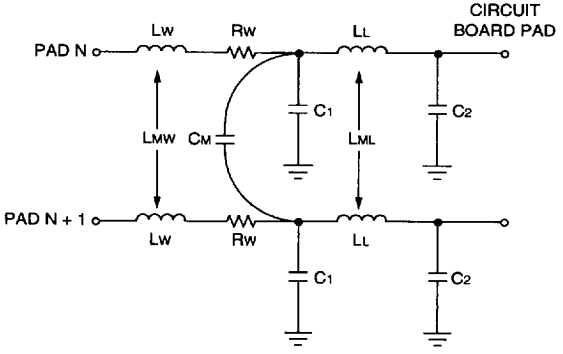


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Figure 41. Package Parasitics

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

The AT&T *ORCA* Series FPGAs include circuitry designed to protect the chips from damaging substrate injection currents and prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

2

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Supply Voltage with Respect to Ground	V_{DD}	–0.5	7.0	V
Input Signal with Respect to Ground	—	–0.5	V_{DD} + 0.3	V
Signal Applied to High-impedance Output	—	–0.5	V_{DD} + 0.3	V
Maximum Soldering Temperature	—	—	260	°C

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Commercial	0 °C to 70 °C	5 V ± 5%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Table 27. Electrical Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage:		Inputs configured as CMOS			
High	V_{IH}		70% V_{DD}	V_{DD} + 0.3	V
Low	V_{IL}		GND – 0.5	20% V_{DD}	V
Input Voltage:		Inputs configured as TTL			
High	V_{IH}		2.0	V_{DD} + 0.3	V
Low	V_{IL}		–0.5	0.8	V
Output Voltage:					
High	V_{OH}	V_{DD} = min, I_{OH} = 6 mA or 3 mA	2.4	—	V
Low	V_{OL}	V_{DD} = min, I_{OL} = 12 mA or 6 mA	—	0.4	V
Input Leakage Current	I_L	V_{DD} = max, V_{IN} = V_{SS} or V_{DD}	–10	10	µA
Standby Current:	I_{DDSB}	T_A = 25 °C, V_{DD} = 5.0 V,			
1C03		internal oscillator running,	—	2.5	mA
1C05		no output loads, inputs at V_{DD}	—	3.0	mA
1C07		or GND	—	3.5	mA
1C09			—	4.0	mA
Standby Current:	I_{DDSB}	T_A = 25 °C, V_{DD} = 5.0 V,			
1C03		internal oscillator stopped,	—	1.0	mA
1C05		no output loads, inputs at V_{DD} or	—	1.2	mA
1C07		GND	—	1.4	mA
1C09			—	1.6	mA
Data Retention Voltage	V_{DR}	T_A = 25 °C	2.3	—	V
Input Capacitance	C_{IN}	T_A = 25 °C, V_{DD} = 5.0 V Test frequency = 1 MHz	—	10	pF
Output Capacitance	C_{OUT}	T_A = 25 °C, V_{DD} = 5.0 V Test frequency = 1 MHz	—	10	pF
DONE Pull-up Resistor	R_{DONE}	—	100K	—	Ω
M3, M2, M1, and M0 Pull-up Resistors	R_M	—	100K	—	Ω
I/O Pad Static Pull-up Current	I_{PU}	V_{DD} = 5.25 V, V_{IN} = V_{SS}, T_A = 0 °C	14.4	50.9	µA
I/O Pad Static Pull-down Current	I_{PD}	V_{DD} = 5.25 V, V_{IN} = V_{DD}, T_A = 0 °C	26	103	µA
I/O Pad Pull-up Resistor	R_{PU}	V_{DD} = 5.25 V, V_{IN} = V_{SS}, T_A = 0 °C	100K	—	Ω
I/O Pad Pull-down Resistor	R_{PD}	V_{DD} = 5.25 V, V_{IN} = V_{DD}, T_A = 0 °C	50K	—	Ω

Timing Characteristics

Table 28. PFU Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Speed						Unit
		–0		–1		–2		
		Min	Max	Min	Max	Min	Max	
Input Requirements								
Clock Low Time	TCL	4.0	—	3.1	—	2.8	—	ns
Clock High Time	TCH	4.0	—	3.1	—	2.8	—	ns
Global S/R Pulse Width (gsrn)	TRW	3.3	—	2.6	—	2.5	—	ns
Local S/R Pulse Width	TPW	3.4	—	2.6	—	2.6	—	ns
Combinatorial Setup Times:								
Four Input Variables to Clock (a[4:0], b[4:0] to ck)	F4*_SET	7.2	—	5.3	—	3.3	—	ns
Five Input Variables to Clock (a[4:0], b[4:0] to ck)	F5*_SET	7.5	—	5.4	—	3.5	—	ns
PFUMUX to Clock (a[4:0], b[4:0] to ck)	MUX_SET	10.3	—	7.5	—	5.3	—	ns
PFUMUX to Clock (c0 to ck)	C0MUX_SET	4.9	—	3.5	—	2.3	—	ns
PFUNAND to Clock (a[4:0], b[4:0] to ck)	ND_SET	9.7	—	7.1	—	4.9	—	ns
PFUNAND to Clock (c0 to ck)	C0ND_SET	5.0	—	3.6	—	2.3	—	ns
PFUXOR to Clock (a[4:0], b[4:0] to ck)	XOR_SET	11.7	—	8.6	—	6.2	—	ns
PFUXOR to Clock (c0 to ck)	C0XOR_SET	4.9	—	3.6	—	2.3	—	ns
Data In to Clock (wd[3:0] to ck)	D*_SET	1.1	—	0.9	—	1.0	—	ns
Clock Enable to Clock (ce to ck)	CKEN_SET	2.0	—	1.4	—	1.5	—	ns
Local Set/Reset (synchronous) (lsr to ck)	LSR_SET	2.9	—	2.2	—	2.1	—	ns
Data Select to Clock (sel to ck)	SELECT_SET	2.6	—	1.8	—	1.9	—	ns
Combinatorial Hold Times:								
Data In (wd[3:0] from ck)	D*_HLD	0.5	—	0.5	—	0.5	—	ns
Clock Enable (ce from ck)	CKEN_HLD	0.5	—	0.5	—	0.5	—	ns
Local Set/Reset (synchronous) (lsr from ck)	LSR_HLD	0.5	—	0.5	—	0.5	—	ns
Data Select (sel from ck)	SELECT_HLD	0.5	—	0.5	—	0.5	—	ns
All Others	—	0.0	—	0.0	—	0.0	—	ns
Output Characteristics								
Combinatorial Delays:								
Four Input Variables (a[4:0], b[4:0] to o[4:0])	F4*_DEL	—	9.5	—	7.0	—	5.2	ns
Five Input Variables (a[4:0], b[4:0] to o[4:0])	F5*_DEL	—	9.8	—	7.1	—	5.4	ns
PFUMUX (a[4:0], b[4:0] to o[4:0])	MUX_DEL	—	12.6	—	9.2	—	7.1	ns
PFUMUX (c0 to o[4:0])	C0MUX_DEL	—	7.2	—	5.2	—	4.2	ns
PFUNAND (a[4:0], b[4:0] to o[4:0])	ND_DEL	—	12.0	—	8.8	—	6.7	ns
PFUNAND (c0 to o[4:0])	C0ND_DEL	—	7.3	—	5.3	—	4.2	ns
PFUXOR (a[4:0], b[4:0] to o[4:0])	XOR_DEL	—	14.0	—	10.3	—	8.0	ns
PFUXOR (c0 to o[4:0])	C0XOR_DEL	—	7.2	—	5.3	—	4.2	ns
Sequential Delays:								
Local S/R (async) to PFU Out (lsr to o[4:0])	LSR_DEL	—	6.6	—	4.9	—	4.2	ns
Global S/R to PFU Out (gsrn to o[4:0])	GSR_DEL	—	5.3	—	4.0	—	3.4	ns
Clock to PFU Out (ck to o[4:0]) — Register	REG_DEL	—	5.6	—	4.2	—	3.4	ns
Clock to PFU Out (ck to o[4:0]) — Latch	LTCH_DEL	—	5.7	—	4.2	—	3.4	ns
Latch Combinatorial Delay (wd[3:0] to o[4:0])	LTCH_CMB	—	6.8	—	5.1	—	4.4	ns

Timing Characteristics (continued)

Table 28. PFU Timing Characteristics (continued)

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Speed						Unit
		–0		–1		–2		
		Min	Max	Min	Max	Min	Max	
Ripple Mode Characteristics								
Ripple Setup Times:								
Operands to Clock (a[3:0], b[3:0] to ck)	RIP_SET	11.6	—	8.4	—	6.3	—	ns
Carry-in to Clock (cin to ck)	CIN_SET	8.0	—	5.9	—	4.2	—	ns
Add/Subtract to Clock (a4 to ck)	AS_SET	15.1	—	10.9	—	8.2	—	ns
Ripple Hold Times (All)	TH	0.0	—	0.0	—	0.0	—	ns
Ripple Delays:								
Operands to Carry-out (a[3:0], b[3:0] to cout)	RIP_CODEL	—	7.7	—	5.6	—	4.4	ns
Operands to Carry-out (o4) (a[3:0], b[3:0] to o4)	RIP_O4DEL	—	11.2	—	8.2	—	6.6	ns
Operands to PFU Out (a[3:0], b[3:0] to o[4:0])	RIP_DEL	—	13.9	—	10.1	—	8.1	ns
Carry-in to Carry-out (cin to cout)	CIN_CODEL	—	4.3	—	3.2	—	2.5	ns
Carry-in to Carry-out (o4) (cin to o4)	CIN_O4DEL	—	7.8	—	5.7	—	4.6	ns
Carry-in to PFU Out (cin to o[4:0])	CIN_DEL	—	10.3	—	7.6	—	6.0	ns
Add/Subtract to Carry-out (a4 to cout)	AS_CODEL	—	9.9	—	7.3	—	5.9	ns
Add/Subtract to Carry-out (o4) (a4 to o4)	AS_O4DEL	—	13.0	—	9.6	—	7.8	ns
Add/Subtract to PFU Out (a4 to o[4:0])	AS_DEL	—	17.4	—	12.6	—	10.0	ns
Read/Write Memory Characteristics								
Read Operation								
Read Cycle Time	TRC	9.5	—	7.0	—	5.2	—	ns
Data Valid after Address (a[3:0], b[3:0] to o[4:0])	MEM*_ADEL	—	9.5	—	7.0	—	5.2	ns
Read Operation, Clocking Data into Latch/Flip-Flop								
Address to Clock Setup Time (a[3:0], b[3:0] to ck)	MEM*_ASET	7.2	—	5.2	—	3.3	—	ns
Clock to PFU Out (ck to o[4:0]) — Register	REG_DEL	—	5.6	—	4.2	—	3.4	ns
Write Operation								
Write Cycle Time	TWC	6.3	—	4.9	—	4.3	—	ns
Write Enable Pulse Width (a4/b4)	TPW	3.8	—	2.9	—	2.6	—	ns
Setup Time:								
Address to wren (a[3:0]/b[3:0] to a4/b4)	MEM*_AWRSET	0.0	—	0.0	—	0.0	—	ns
Data to wren (wd[3:0] to a4/b4)	MEM*_DWRSET	0.0	—	0.0	—	0.0	—	ns
Hold Time:								
Address from wren (a[3:0]/b[3:0] to a4/b4)	MEM*_WRAHLD	2.5	—	2.0	—	1.7	—	ns
Data from wren (wd[3:0] to a4/b4)	MEM*_WRDHLD	1.7	—	1.4	—	1.2	—	ns

Timing Characteristics (continued)

Table 28. PFU Timing Characteristics (continued)

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Speed						Unit
		–0		–1		–2		
		Min	Max	Min	Max	Min	Max	
Read During Write Operation								
Write Enable to PFU Output Delay (a4/b4 to o[4:0])	MEM*_WRDEL	—	10.0	—	7.4	—	6.0	ns
Data to PFU Output Delay (wd[3:0] to o[4:0])	MEM*_DDEL	—	8.2	—	6.2	—	4.5	ns
Read During Write, Clocking Data into Latch/Flip-Flop								
Setup Time: Write Enable to Clock (a4/b4 to ck) Data (wd[3:0] to ck)	 MEM*_WRSET MEM*_DSET	 7.7 5.9	 — —	 5.7 4.5	 — —	 4.1 2.6	 — —	 ns ns
Hold Time (All)	T_H	0.0	—	0.0	—	0.0	—	ns
Clock to PFU Out (ck to o[4:0]) — Register	REG_DEL	—	5.6	—	4.2	—	3.4	ns

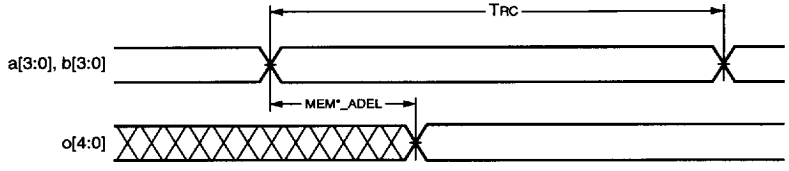

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Figure 41. Read Operation—Flip-Flop Bypass

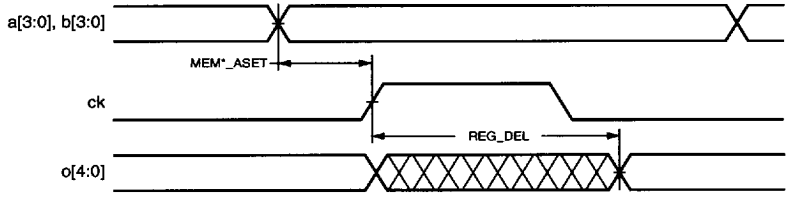

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Figure 42. Read Operation—LUT Memory Loading Flip-Flops

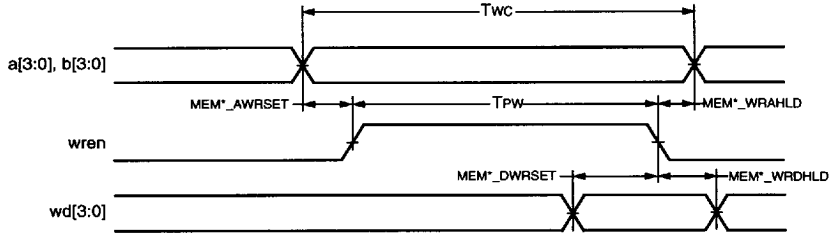

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Figure 43. Write Operation

Timing Characteristics (continued)

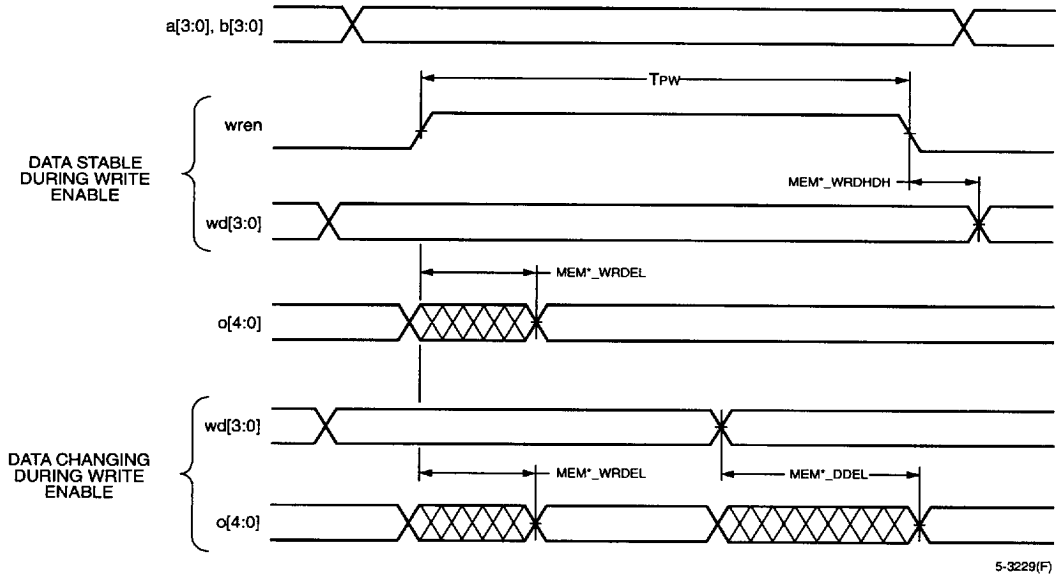


Figure 44. Read During Write

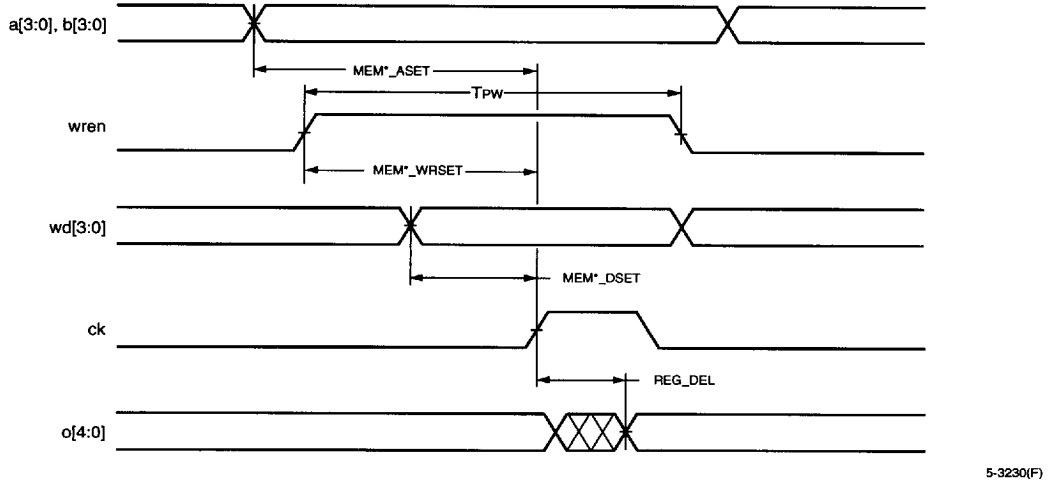


Figure 45. Read During Write—Clocking Data into Flip-Flop

Timing Characteristics (continued)

Table 29. PLC BIDI and Direct Routing Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Speed						Unit
		–0		–1		–2		
		Min	Max	Min	Max	Min	Max	
PLC 3-Statable BIDIs								
BIDI Propagation Delay	TRI_DEL	—	1.9	—	1.5	—	1.2	ns
BIDI 3-State Enable/Disable Delay	TRIEN_DEL	—	2.8	—	2.3	—	1.7	ns
Direct Routing								
PFU to PFU Delay (xsw)	DIR_DEL	—	2.3	—	1.7	—	1.4	ns
PFU Feedback (xsw)	FDBK_DEL	—	1.7	—	1.3	—	1.0	ns

Table 30. Clock Delay

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Speed						Unit
		–0		–1		–2		
		Min	Max	Min	Max	Min	Max	
1C03 Clock Delay	CLK_DEL	—	10.9	—	8.4	—	6.7	ns
1C05 Clock Delay	CLK_DEL	—	11.1	—	8.6	—	6.9	ns
1C07 Clock Delay	CLK_DEL	—	11.4	—	8.8	—	7.0	ns
1C09 Clock Delay	CLK_DEL	—	11.6	—	9.0	—	7.2	ns

Table 31. Programmable I/O Cell Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Speed						Unit
		–0		–1		–2		
		Min	Max	Min	Max	Min	Max	
Inputs								
Input Rise Time	TR	—	500	—	500	—	500	ns
Input Fall Time	TF	—	500	—	500	—	500	ns
Pad to In Delay	FASTIN_G_DEL	—	4.9	—	3.7	—	2.6	ns
Pad toTRIDI Delay	FASTIN_L_DEL	—	4.1	—	3.1	—	2.2	ns
Pad to In Delay (delay mode)	DLYIN_G_DEL	—	13.4	—	9.8	—	8.0	ns
Pad to TRIDI Delay (delay mode)	DLYIN_L_DEL	—	3.9	—	2.9	—	2.0	ns
Pad to Nearest PFU Latch Output Delay	CHIP_LATCH	—	14.0	—	10.5	—	8.3	ns
Setup Time:								
Pad to Nearest PFU ck	CHIP_SET	8.3	—	6.3	—	4.9	—	ns
Pad to Nearest PFU ck (delay mode)*	DLY_CHP_SET	16.8	—	12.4	—	10.3	—	ns
Outputs								
PFU ck to Pad Delay (dout[3:0] to pad):								
Fast	DOUT_DEL(F)	—	10.5	—	7.5	—	5.6	ns
Slewlim	DOUT_DEL(SL)	—	12.6	—	9.3	—	7.2	ns
Sinklim	DOUT_DEL(SI)	—	18.7	—	14.0	—	11.1	ns
Output to Pad Delay (out[3:0] to pad):								
Fast	OUT_DEL(F)	—	6.4	—	4.9	—	3.7	ns
Slewlim	OUT_DEL(SL)	—	8.5	—	6.7	—	5.3	ns
Sinklim	OUT_DEL(SI)	—	14.6	—	11.3	—	9.2	ns
3-state Enable Delay (ts[3:0] to pad):								
Fast	TS_DEL(F)	—	8.4	—	5.9	—	4.8	ns
Slewlim	TS_DEL(SL)	—	10.4	—	7.7	—	6.4	ns
Sinklim	TS_DEL(SI)	—	16.6	—	12.3	—	10.3	ns

* If the input buffer is in delay mode, the chip hold time to the nearest PFU latch is guaranteed to be 0 if the clock is routed using the primary clock network.

Timing Characteristics (continued)

Table 32. General Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
All Configuration Modes				
M[3:0] Setup Time to $\overline{\text{INIT}}$ High	TSMODE	50	—	ns
M[3:0] Hold Time from $\overline{\text{INIT}}$ High	THMODE	600	—	ns
$\overline{\text{RESET}}$ Pulse Width Low	TRW	50	—	ns
$\overline{\text{PRGM}}$ Pulse Width Low	TPGW	50	—	ns
Master and Asynchronous Peripheral Modes				
Power-on Reset Delay	TPO	16.24	43.80	ms
CCLK Period (M3 = 0)	TCCLK	62.00	167.00	ns
(M3 = 1)		496.00	1336.00	ns
Configuration Latency (noncompressed)	TCL			
ATT1C03 (M3 = 0)		3.20	8.64*	ms
(M3 = 1)		25.60	69.12*	ms
ATT1C05 (M3 = 0)		4.40	11.86*	ms
(M3 = 1)		35.20	94.88*	ms
ATT1C07 (M3 = 0)		5.78	15.59*	ms
(M3 = 1)		46.24	124.72*	ms
ATT1C09 (M3 = 0)		7.35	19.82*	ms
(M3 = 1)		58.85	158.53*	ms
Slave Serial and Synchronous Peripheral Modes				
Power-on Reset Delay	TPO	4.06	10.95	ms
CCLK Period	TCCLK	100.00	—	ns
Configuration Latency (noncompressed)	TCL			
ATT1C03		5.17	—	ms
ATT1C05		7.10	—	ms
ATT1C07		9.33	—	ms
ATT1C09		11.86	—	ms
Slave Parallel Mode				
Power-on Reset Delay	TPO	4.06	10.95	ms
CCLK Period	TCCLK	100.00	—	ns
Configuration Latency (noncompressed)	TCL			
ATT1C03		0.64	—	ms
ATT1C05		0.89	—	ms
ATT1C07		1.17	—	ms
ATT1C09		1.48	—	ms

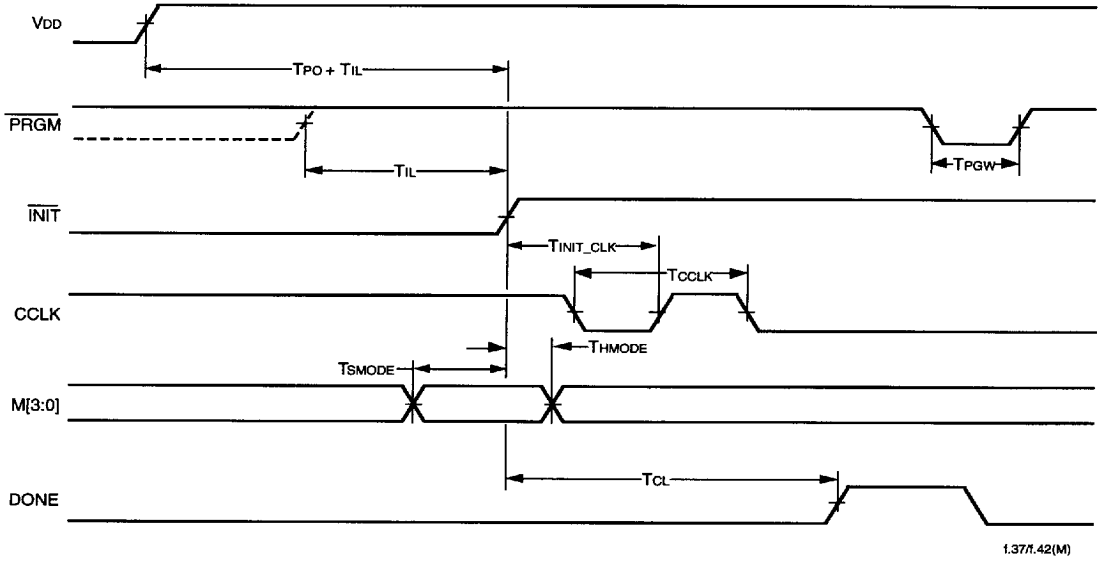
* Not applicable to asynchronous peripheral mode.

Timing Characteristics (continued)

Table 32. General Configuration Mode Timing Characteristics (continued)

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
$\overline{INIT}$ Timing				
$\overline{INIT}$ High to CCLK Delay	TINIT_CCLK			
Slave Parallel		1.00	—	µs
Slave Serial		1.00	—	µs
Synchronous Peripheral		1.00	—	µs
Master Serial				
M3 = 1		1.00	2.90	µs
M3 = 0		0.50	0.70	µs
Master Parallel				
M3 = 1		4.90	13.60	µs
M3 = 0		1.00	2.90	µs
$\overline{INIT}$ High to $\overline{WR}$, Asynchronous Peripheral	TINIT_WR	1.50	—	µs
Initialization Latency ($\overline{PRGM}$ high to $\overline{INIT}$ high):	TIL			
ATT1C03		55.30	150.97	µs
ATT1C05		65.72	179.03	µs
ATT1C07		76.13	207.08	µs
ATT1C09		86.55	235.14	µs



Note: T_{PO} is triggered when V_{DD} reaches between 3.0 V to 4.0 V.

Figure 46. General Configuration Mode Timing Diagram

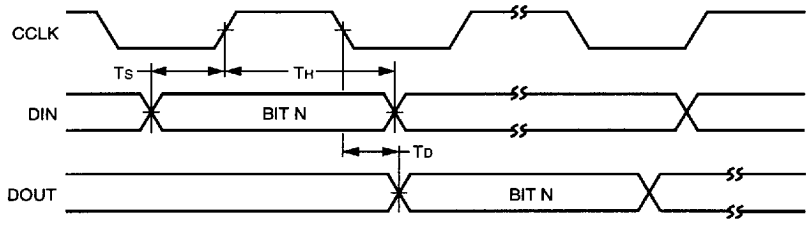
Timing Characteristics (continued)

Table 33. Master Serial Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Nom	Max	Units
DIN Setup Time	T_S	60.0	—	—	ns
DIN Hold Time	T_H	0	—	—	ns
CCLK Frequency (M3 = 0)	Fc	6.0	10.0	16.0	MHz
CCLK Frequency (M3 = 1)	Fc	0.75	1.25	2.0	MHz
CCLK to DOUT Delay	T_D	—	—	30	ns

Note: Serial data is transmitted out on DOUT on the falling edge of CCLK after it is input DIN.



f.38/f.43(M)

Figure 47. Master Serial Configuration Mode Timing Diagram

Timing Characteristics (continued)

Table 34. Master Parallel Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
RCLK to Address Valid	T_{AV}	0	200	ns
D[7:0] Setup Time to RCLK	T_S	60	—	ns
D[7:0] Hold Time to RCLK	T_H	0	—	ns
RCLK Low Time (M3 = 0)	T_{CL}	434	1169	ns
RCLK High Time (M3 = 0)	T_{CH}	62	167	ns
RCLK Low Time (M3 = 1)	T_{CL}	3472	9352	ns
RCLK High Time (M3 = 1)	T_{CH}	496	1336	ns
CCLK to DOUT	T_D	—	30	ns

Notes:
The RCLK period consists of seven CCLKs for RCLK low, and one CCLK for RCLK high.
Serial data is transmitted out on DOUT 1.5 CCLK cycles after the byte is input D[7:0].

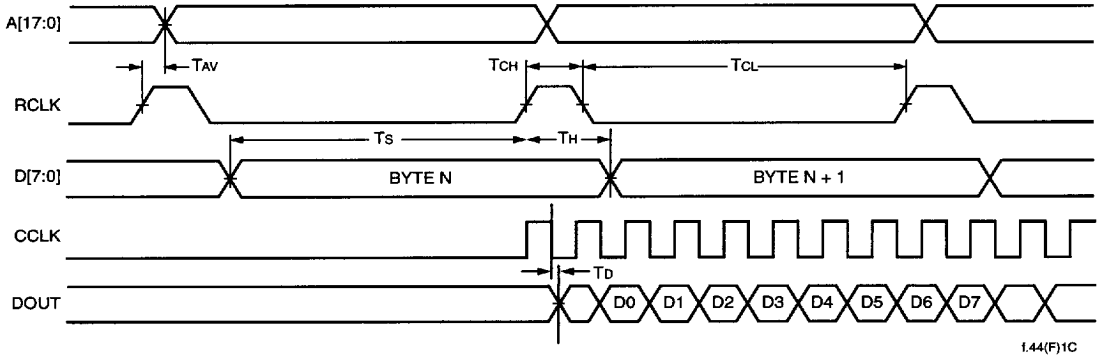


Figure 48. Master Parallel Configuration Mode Timing Diagram

Timing Characteristics (continued)

Table 35. Asynchronous Peripheral Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
$\overline{CS0}$, CS1, and WR Pulse Width	T_{WR}	100	—	ns
D[7:0] Setup Time	T_S	20	—	ns
D[7:0] Hold Time	T_H	0	—	ns
RDY/$\overline{BUSY}$ Delay	T_{RDY}	—	60	ns
RDY/$\overline{BUSY}$ Low	T_B	2	9	CCLK Periods
Earliest $\overline{WR}$ After End of $\overline{BUSY}$	T_{WR2}	0	—	ns
CCLK to DOUT	T_D	—	30	ns

Note: Serial data is transmitted out on DOUT on the falling CCLK edge after the byte is input D[7:0].

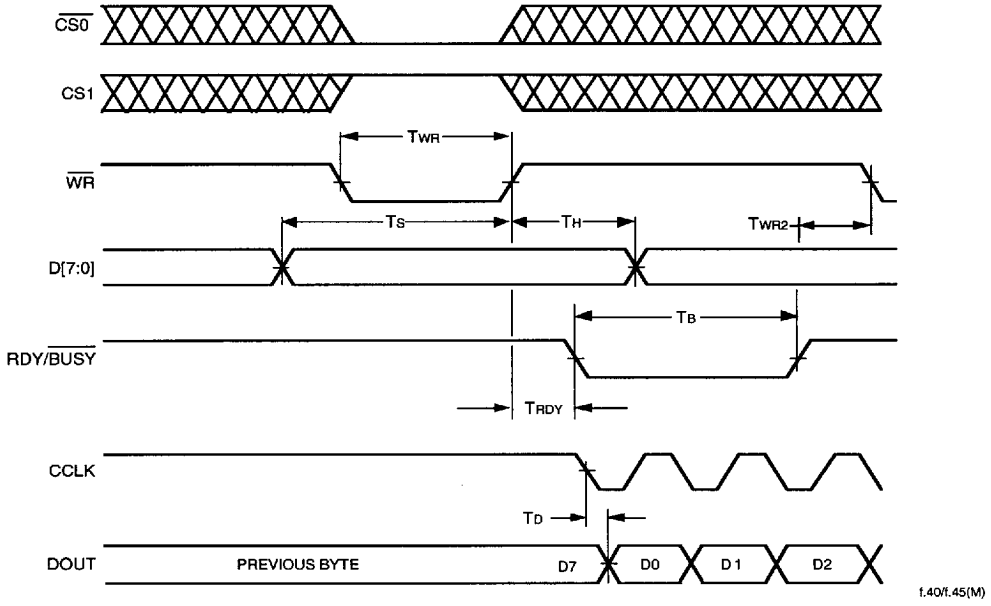


Figure 49. Asynchronous Peripheral Configuration Mode Timing Diagram

Timing Characteristics (continued)

Table 36. Synchronous Peripheral Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
D[7:0] Setup Time	T_S	20	—	ns
D[7:0] Hold Time	T_H	0	—	ns
CCLK High Time	T_{CH}	50	—	ns
CCLK Low Time	T_{CL}	50	—	ns
CCLK Frequency	F_C	—	10	MHz
CCLK to DOUT	T_D	—	30	ns

Note: Serial data is transmitted out on DOUT 1.5 clock cycles after the byte is input D[7:0].

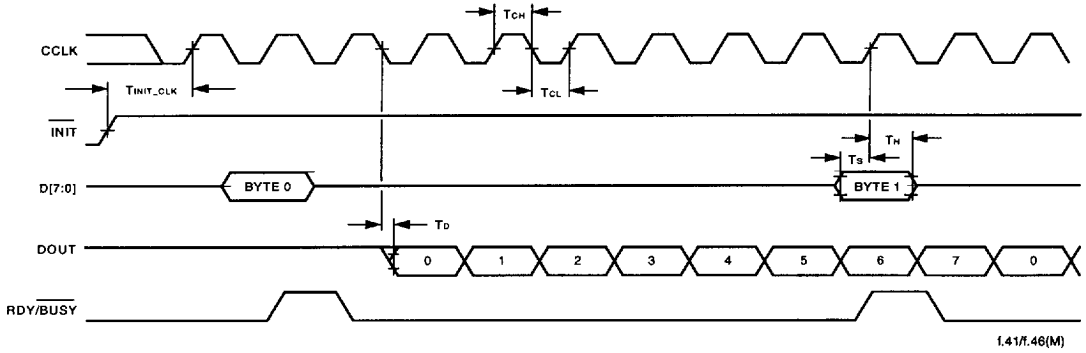


Figure 50. Synchronous Peripheral Configuration Mode Timing Diagram

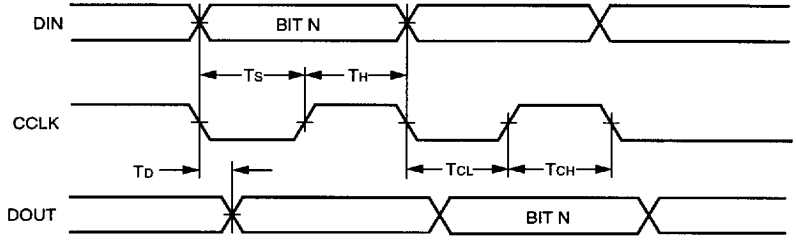
Timing Characteristics (continued)

Table 37. Slave Serial Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
DIN Setup Time	T_S	20	—	ns
DIN Hold Time	T_H	0	—	ns
CCLK High Time	T_{CH}	50	—	ns
CCLK Low Time	T_{CL}	50	—	ns
CCLK Frequency	F_C	—	10	MHz
CCLK to DOUT	T_D	—	30	ns

Note: Serial data is transmitted out on DOUT on the falling edge of CCLK after it is input on DIN.



1.42/1.47(M)

Figure 51. Slave Serial Configuration Mode Timing Diagram

Timing Characteristics (continued)

Table 38. Slave Parallel Configuration Mode Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.

Parameter	Symbol	Min	Max	Units
$\overline{CS0}$, CS1, $\overline{WR}$ Setup Time	T_{S1}	60	—	ns
$\overline{CS0}$, CS1, $\overline{WR}$ Hold Time	T_{H1}	20	—	ns
D[7:0] Setup Time	T_{S2}	20	—	ns
D[7:0] Hold Time	T_{H2}	0	—	ns
CCLK High Time	T_{CH}	50	—	ns
CCLK Low Time	T_{CL}	50	—	ns
CCLK Frequency	F_C	—	10	MHz

Note: Daisy-chaining of FPGAs is not possible in this mode.

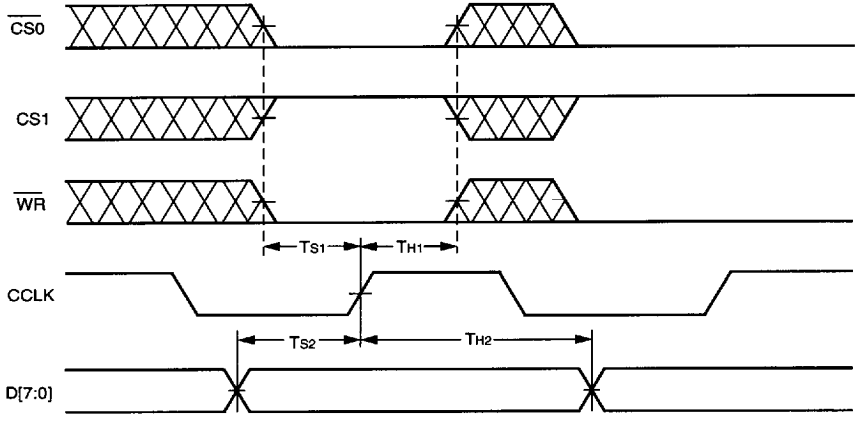


Figure 52. Slave Parallel Configuration Mode Timing Diagram

Timing Characteristics (continued)

Table 39. Readback Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
$\overline{RD\_CFGN}$ to CCLK Setup Time	T_S	50	—	ns
$\overline{RD\_CFGN}$ High Width to Abort Readback	T_{RBA}	2	—	CCLKs
CCLK Low Time	T_{CL}	50	—	ns
CCLK High Time	T_{CH}	50	—	ns
CCLK Frequency	F_C	—	10	MHz
CCLK to RD_DATA Delay	T_D	—	50	ns

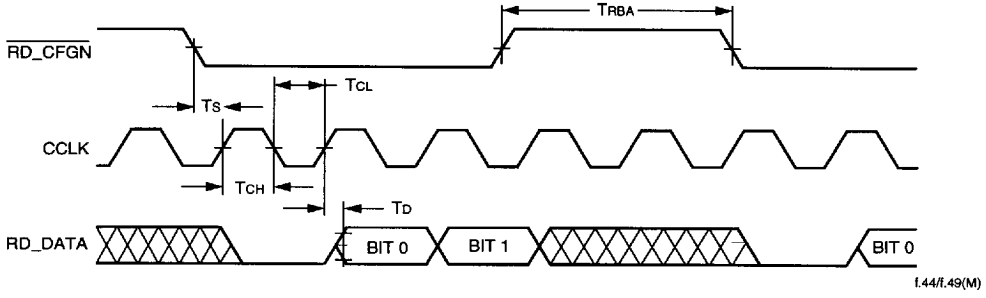


Figure 53. Readback Timing Diagram

Timing Characteristics (continued)

Table 40. Boundary-Scan Timing Characteristics

Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C; C_L = 50 pF.

Parameter	Symbol	Min	Max	Units
TDI/TMS to TCK Setup Time	T_S	25	—	ns
TDI/TMS Hold Time from TCK	T_H	0	—	ns
TCK Low Time	T_{CL}	50	—	ns
TCK High Time	T_{CH}	50	—	ns
TCK to TDO Delay	T_D	—	20	ns
TCK Frequency	T_{TCK}	—	10	MHz

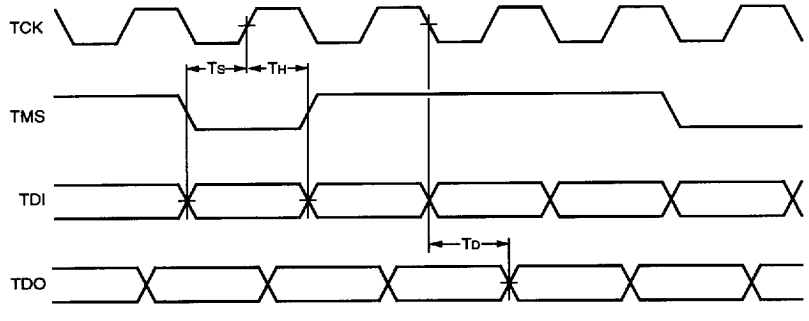
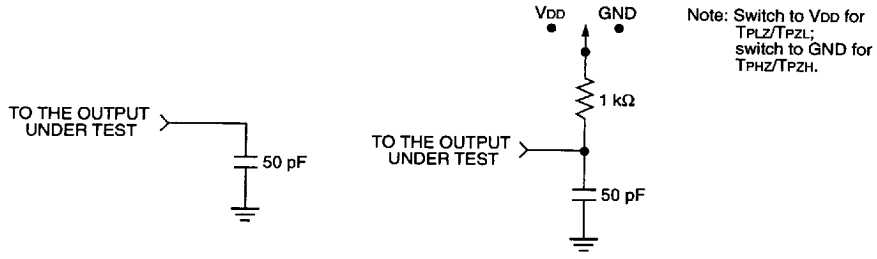


Figure 54. Boundary-Scan Timing Diagram

Measurement Conditions



A. Load Used to Measure Propagation Delay **B. Load Used to Measure Rising/Falling Edges**

Figure 55. ac Test Loads

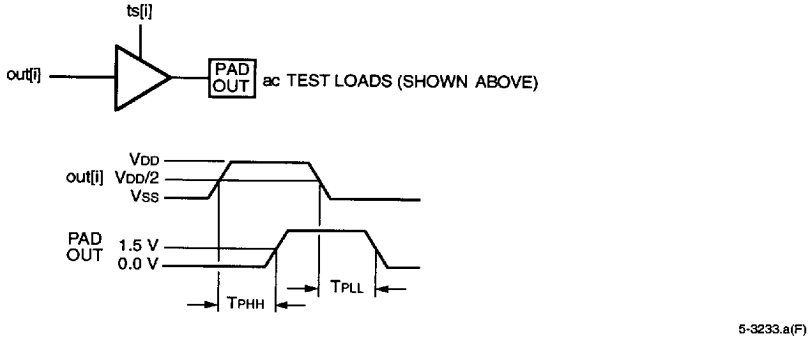


Figure 56. Output Buffer Delays

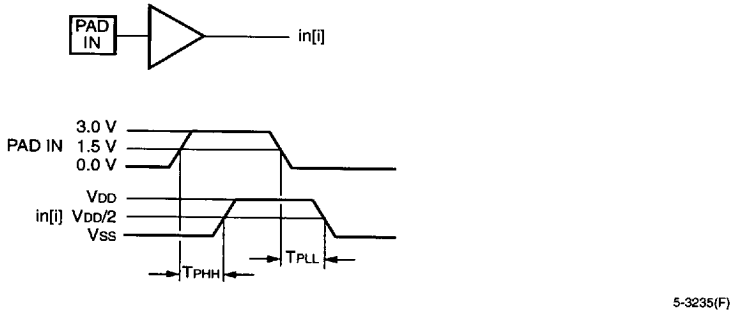
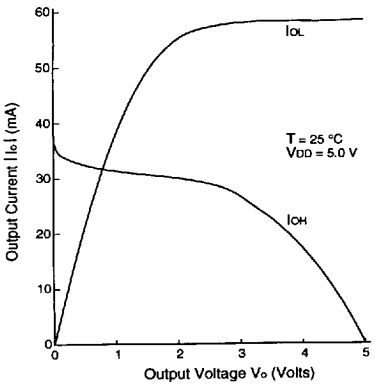
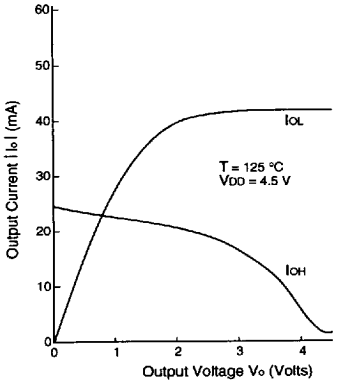


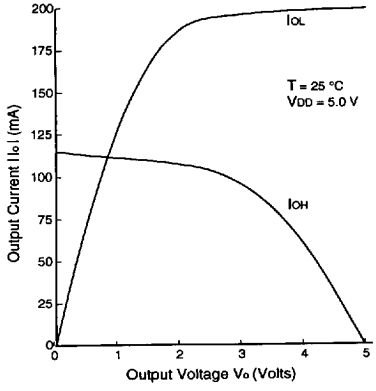
Figure 57. Input Buffer Delays

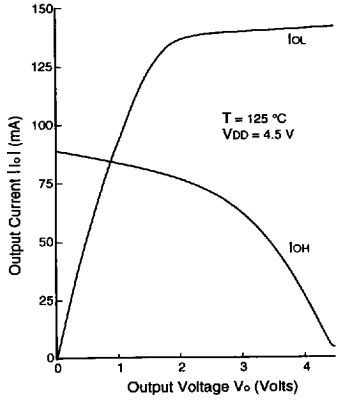
Output Buffer Characteristics



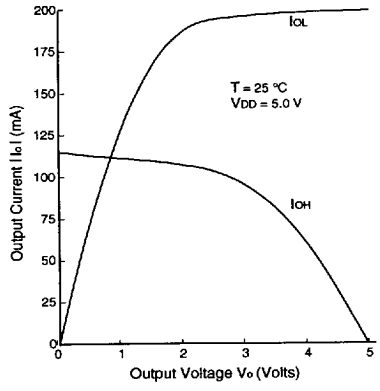


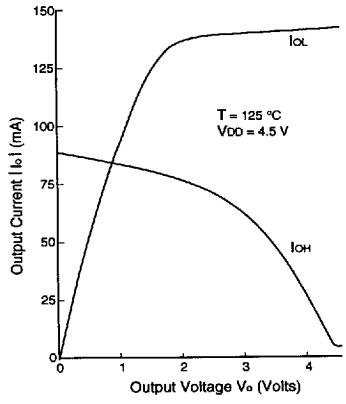
Sinklim





Slewlim

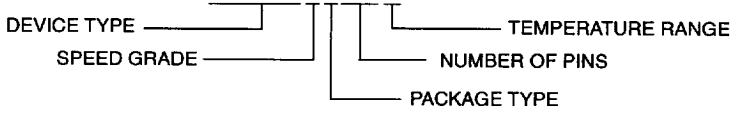




Fast

Ordering Information

Example: **ATT1C07-1R280**



ATT1C07, –1 Speed Grade, 280-pin Ceramic PGA, Commercial Temperature

Table 41. FPGA Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 42. FPGA Package Options

Symbol	Description
F	JEDEC Plastic Quad Flat Pack
H	Plastic Pin Grid Array
M	Plastic Leaded Chip Carrier
R	Ceramic Pin Grid Array
S	Shrink Quad Flat Pack
T	Thin Quad Flat Pack

Table 43. *ORCA* 1C Series Package Matrix

Packages	84-Pin PLCC	100-Pin TQFP	132-Pin JEDEC BQFP	144-Pin TQFP	208-Pin EIAJ SQFP	225-Pin		240-Pin EIAJ SQFP	280-Pin Ceramic PGA	304-Pin EIAJ SQFP
						Plastic PGA	Ceramic PGA			
Devices	**M84**	**T100**	**F132**	**T144**	**S208**	**H225**	**R225**	**S240**	**R280**	**S304**
ATT1C03	CI	CI	CI	CI	CI	CI	CI	—	—	—
ATT1C05	CI	CI	CI	CI	CI	CI	CI	CI	—	—
ATT1C07	—	—	—	—	CI	—	—	CI	CI	CI
ATT1C09	—	—	—	—	CI	—	—	CI	—	CI

Key: C = commercial, I = industrial.