3.3V 1:8 LVCMOS PLL Clock Generator

Features

- 1:8 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3V power supply
- Generates clock signals up to 125MHz
- PLL guaranteed to lock down to 145MHz, output frequency = 36.25MHz
- Maximum output skew of 150 pS
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 16 clock lines
- 32 lead LQFP & TQFP Packages
- Industrial temperature range
- Pin and function compatible to the MPC953,MPC9653A and MPC9653

Functional Description

The PCS5I9653A utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the PCS5I9653A requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 25 to 62.5MHz or 50 to 125MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-4 or divide-by-8) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the PCS5I9653A is running at either 4x or 8x of the reference clock frequency. The PCS5I9653A is guaranteed to lock in a low power PLL mode in the high frequency range (VCO_SEL = 0) down to PLL = 145 MHz or Fref = 36.25MHz.

The PCS5I9653A has a differential LVPECL reference input long with an external feedback input. The device is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance. The PLL_EN and BYPASS controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/OE pin. Asserting MR/OE also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/OE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The PCS5I9653A is fully 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50Ω transmission lines. For series terminated transmission lines, each of the PCS5I9653A outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm2 32-lead LQFP & TQFP Packages.

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Block Diagram

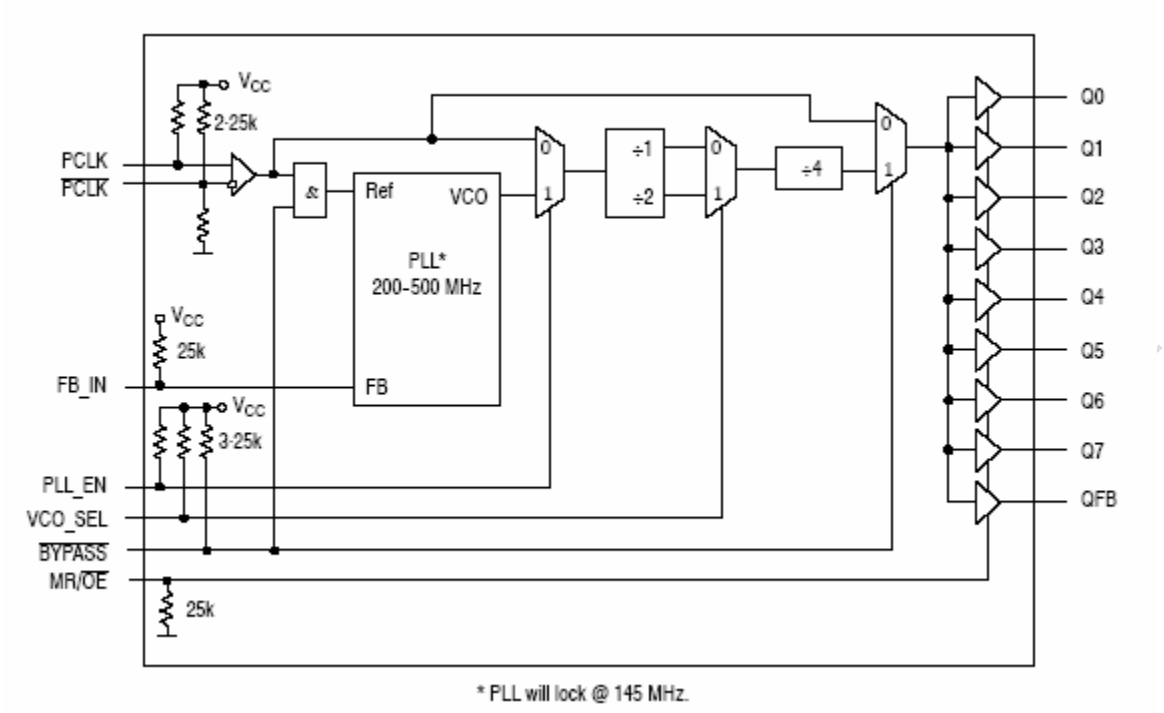


Figure 1. PCS5I9653A Logic Diagram

Pin Configuration

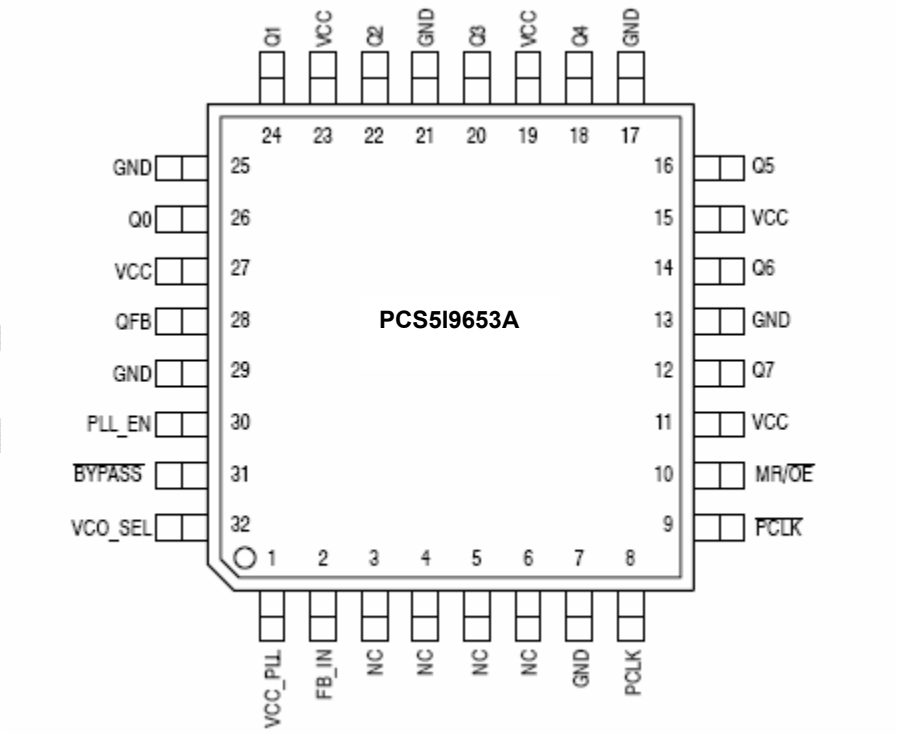


Figure 2. PCS5I9653A 32-Lead Package Pinout (Top View)

Table 1: Pin Configuration

Pin #	Pin Name	I/O	Type	Function
8,9	PCLK, $\overline{PCLK}$	Input	LVPECL	PECL reference clock signal
2	FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
32	VCO_SEL	Input	LVCMOS	Operating frequency range select
31	$\overline{BYPASS}$	Input	LVCMOS	PLL and output divider bypass select
30	PLL_EN	Input	LVCMOS	PLL enable/disable
10	MR/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
26,24,22,20,18,16,14,12	Q0-7	Output	LVCMOS	Clock outputs
28	QFB	Output	LVCMOS	Clock output for PLL feedback, connect to FB_IN
7,13,17,21,25,29	GND	Supply	Ground	Negative power supply (GND)
1	VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin VCC_PLL. Please see applications section for details
11,15,19,23,27	VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation
3,4,5,6	NC	-	-	No Connect

Table 2: Function Table

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. PCS5I9653A is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output[1]
$\overline{BYPASS}$	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. PCS5I9653A is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). fREF =fQ0-7 =4 . fVCO	VCO ÷ 2 (Low output range). fREF =fQ0-7 =8 . fVCO
MR/OE	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

Note: 1 PLL operation requires BYPASS=1 and PLL_EN=1.

Table 3: General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VTT	Output Termination Voltage		VCC÷2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
CPD	Power Dissipation Capacitance		10		pF	Per output
CIN	Input Capacitance		4.0		pF	Inputs

Table 4: Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
VCC	Supply Voltage	-0.3	3.9	V	
VIN	DC Input Voltage	-0.3	VCC+0.3	V	
VOUT	DC Output Voltage	-0.3	VCC+0.3	V	
IIN	DC Input Current		±20	mA	
IOUT	DC Output Current		±50	mA	
TS	Storage Temperature	-65	125	°C	

Table 5: DC CHARACTERISTICS (VCC = 3.3V ± 5%, TA =-40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VIH	Input high voltage	2.0		VCC +0.3	V	LVCMOS
VIL	Input low voltage			0.8	V	LVCMOS
VPP	Peak-to-peak input voltage (PCLK)	300			mV	LVPECL
VCMR[2]	Common Mode Range (PCLK)	1.0		VCC-0.6	V	LVPECL
VOH	Output High Voltage	2.4			V	IOH=-24 mA[3]
VOL	Output Low Voltage			0.55 0.30	V V	IOL=24mA IOL=12mA
ZOUT	Output impedance		14 -17		Ω	
IIN	Input Current[4]			±200	µA	VIN=VCC or GND
ICC_PLL	Maximum PLL Supply Current		10	15	mA	VCC_PLL Pin
ICCQ[5]	Maximum Quiescent Supply Current			15	mA	All VCC Pins

[1] Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

[2] VCMR (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the VCMR range and the input swing lies within the VPP (DC) specification.

[3] The PCS3P9653A is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of VTT. Alternatively, the device drives up to two 50 Ω series terminated transmission lines. The PCS3P9653A meets the VOH and VOL specification of the PCS3P953 (VOH > VCC-0.6V at IOH=-20mA and VOL > 0.6V at IOL=20mA).

[4] Inputs have pull-down or pull-up resistors affecting the input current.

[5] OE/MR=1 (outputs in high-impedance state).

Table 6: AC CHARACTERISTICS (VCC = 3.3V ± 5%, TA = -40°C to +85°C)[6]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
fREF	Input reference frequency ÷4 feedback[7]	50		125	MHz	PLL locked
	PLL mode, external feedback ÷8 feedback[8]	25		62.5	MHz	PLL locked
	Input reference frequency in PLL bypass mode[9]	0		200	MHz	
fVCO	VCO operating frequency range[10,11]	200		500	MHz	
fVCOlock	VCO lock frequency range[12]	145		500	MHz	
fMAX	Output Frequency ÷4 feedback[8]	50		125	MHz	PLL locked
	÷8 feedback[9]	25		62.5	MHz	PLL locked
VPP	Peak-to-peak input voltage PCLK	450		1000	mV	LVPECL
VCMR[13]	Common Mode Range PCLK	1.2		VCC-0.75	V	LEPVCL
tPW,MIN	Input Reference Pulse Width[14]	2			nS	
t(Ø)	Propagation Delay (static phase offset)[15] PCLK to FB_IN	-75		125	pS	PLL locked
tPD	Propagation Delay					
	PLL and divider bypass ($\overline{BYPASS}$=0), PCLK to Q0-7	1.2		3.3	nS	
	PLL disable (BYPASS=1 and PLL_EN=0), PCLK to Q0-7	3.0		7.0	nS	
tsk(O)	Output-to-output Skew[16]			150	pS	
tsk(PP)	Device-to-device Skew in PLL and divider bypass[17]			1.5	nS	$\overline{BYPASS}$=0
DC	Output duty cycle	45	50	55	%	PLL locked
tR,tF	Output Rise/Fall Time	0.1		1.0	nS	0.55 to 2.4V
tPLZ, HZ	Output Disable Time			7.0	nS	
tPZL, LZ	Output Enable Time			6.0	nS	
tJIT(CC)	Cycle-to-cycle jitter			100	pS	
tJIT(PER)	Period Jitter			100	pS	
tJIT(Ø)	I/O Phase Jitter[18]					
	RMS (1 σ)			25	pS	
BW	PLL closed loop bandwidth[19] ÷ 4 feedback[8]		0.8-4		MHz	
	PLL mode, external feedback ÷8 feedback[9]		0.5 -1.3			
tLOCK	Maximum PLL Lock Time			10	mS	

[6] AC characteristics apply for parallel output termination of 50Ω to VTT.
[7] ÷4 PLL feedback (high frequency range) requires VCO_SEL=0, PLL_EN=1, BYPASS=1 and MR/$\overline{OE}$=0.
[8] ÷8 PLL feedback (low frequency range) requires VCO_SEL=1, PLL_EN=1, $\overline{BYPASS}$=1 and MR/$\overline{OE}$=0.
[9] In bypass mode, the PCS3P9653A divides the input reference clock.
[10] The input frequency fREF must match the VCO frequency range divided by the feedback divider ratio FB: fREF = fVCO ÷ FB.
[11] fVCO is frequency range where AC parameters are guaranteed.
[12] fVCOlock is frequency range that the PLL guaranteed to lock, AC parameters only guaranteed over fVCO.
[13] VCMR (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the VCMR range and the input swing lies within the VPP (AC) specification. Violation of VCMR or VPP impacts static phase offset t(Ø).
[14] Calculation of reference duty cycle limits: DCREF,MIN = tPW,MIN . fREF . 100% and DCREF,MAX = 100% - DCREF,MIN. E.g. at fREF=100 MHz the input duty cycle range is 20% < DC < 80%.
[15] Valid for fREF=50 MHz and FB=÷8 (VCO_SEL=1). For other reference frequencies: t(Ø) [ps] = 50 ps ± (1÷(120 . fREF)).
[16] See application section for part-to-part skew calculation in PLL zero-delay mode.
[17] For a specified temperature and voltage, includes output skew.
[18] I/O phase jitter is reference frequency dependent. See application section for details.
[19] -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Driving Transmission Lines

The PCS5I9653A supports output clock frequencies from 25 to 125MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (V_{CO_SEL}) should be used to situate the VCO in the frequency lock range between 200 and 500MHz for stable and optimal operation. Two operating frequency ranges are supported : 25 to 62.5MHz and 50 to 125MHz. Table 9 illustrates the configurations supported by the PCS5I9653A. PLL zero-delay is supported if BYPASS=1, PLL_EN=1 and the input frequency is within the specified PLL reference frequency range.

BYPASS	PLL_ EN	VCO_ SEL	Operation	Frequency		
				Ratio	Output range (fQ0-7)	VCO
0	X	X	Test mode: PLL and divider bypass	fQ0-7 =fREF	0-200MHz	n/a
1	0	0	Test mode: PLL bypass	fQ0-7 =fREF ÷ 4	0-50MHz	n/a
1	0	1	Test mode: PLL bypass	fQ0-7 =fREF ÷ 8	0-25MHz	n/a
1	1	0	PLL mode (high frequency range)	fQ0-7 =fREF	50 to 125MHz	fVCO =fREF 4
1	1	1	PLL mode (low frequency range)	fQ0-7 =fREF	25 to 62.5MHz	fVCO =fREF 8

Power Supply Filtering

The PCS5I9653A is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The PCS5I9653A provides separate power supplies for the output buffers (VCC) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the VCC_PLL pin for the PCS5I9653A. Figure 3 illustrates a typical power supply filter scheme. The PCS5I9653A frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the ICCA current (the current sourced through the V_{CC_PLL} pin) is typically 10 mA (15 mA maximum), assuming that a minimum of 2.985V must be maintained on the V_{CC_PLL} pin.

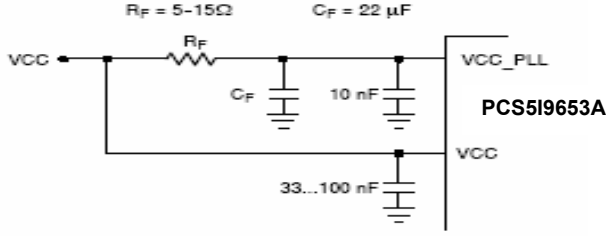


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide attenuation greater than 40 dB for noise whose spectral content is above 100kHz. In the example RC filter shown in Figure 3. "VCC_PLL Power Supply Filter", the filter cut-off frequency is around 4 kHz and the noise attenuation at 100kHz is better than 42 dB. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the PCS5I9653A has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the PCS5I9653A in zero-delay applications

Nested clock trees are typical applications for the PCS5I9653A. Designs using the PCS5I9653A as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the PCS5I9653A clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

rev 0.3

Calculation of part-to-part skew

The PCS5I9653A zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more PCS5I9653A are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is: *tSK(PP) = t(Ø) + tSK(O) + tPD, LINE(FB) + tJIT(Ø) ¡ CF* This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

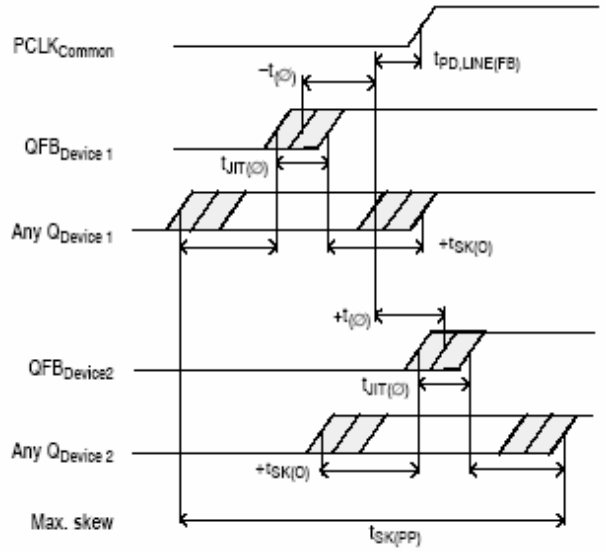


Figure 4. PCS5I9653A max device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10: Confidence Factor C_F

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -197 pS to 297 pS (at 125MHz reference frequency) relative to PCLK:

tSK(PP) = [-17pS...117pS] + [-150pS...150pS] + [(10pS . -3)...(10pS . 3)] + tPD, LINE(FB)
tSK(PP) = [-197pS...297pS] + tPD, LINE(FB)

Due to the frequency dependence of the I/O jitter, Figure 5. .Max. I/O Jitter versus frequency. can be used for a more precise timing performance analysis.

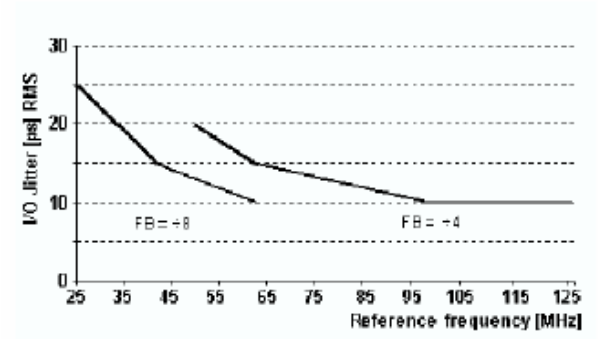


Figure 5. Maximum I/O Jitter vs Frequency

Driving Transmission Lines

The PCS5I9653A clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PCS5I9653A clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6 “Single versus Dual Transmission Lines” Illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the PCS5I9653A clock driver is effectively doubled due to its capability to drive multiple lines.

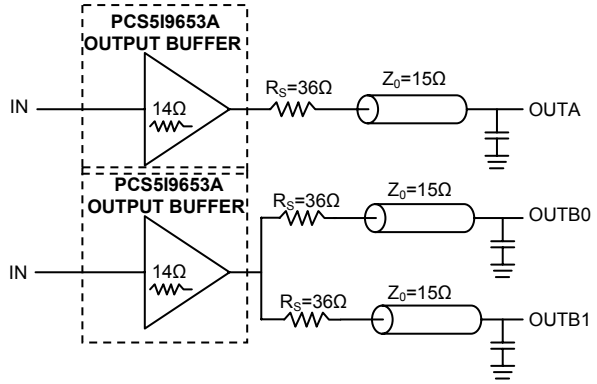


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 .Single versus Dual Line Termination Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the PCS5I9653A output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCS5I9653A. The output waveform in Figure 7 Single versus Dual Line Termination Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$
$Z_0 = 50\Omega \,||\, 50\Omega$
$R_S = 36\ \Omega \,||\, 36\ \Omega$
$R_0 = 14\ \Omega$
$V_L = 3.0 (25 \mid (18+14+25)$
$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0nS).

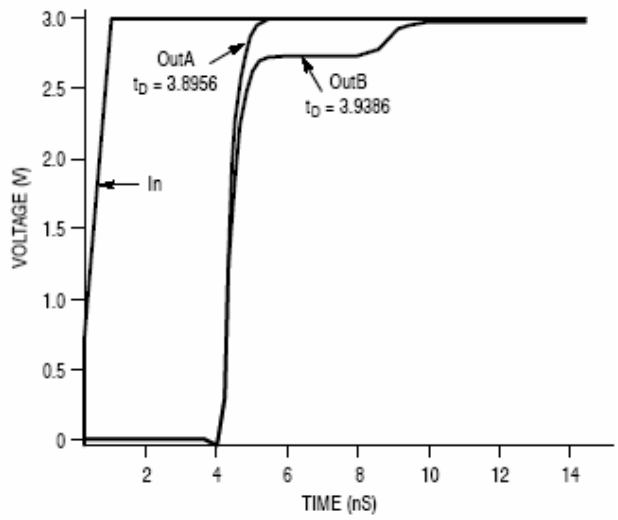
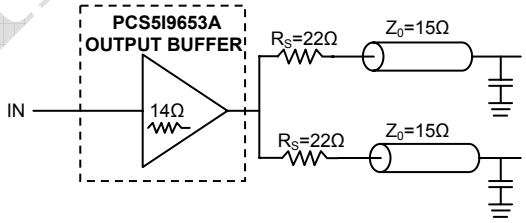


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 .Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \_ 22\Omega = 50\Omega \_ 50\Omega$
$25\Omega = 25\Omega$

Figure 8. Optimized Dual Line Termination

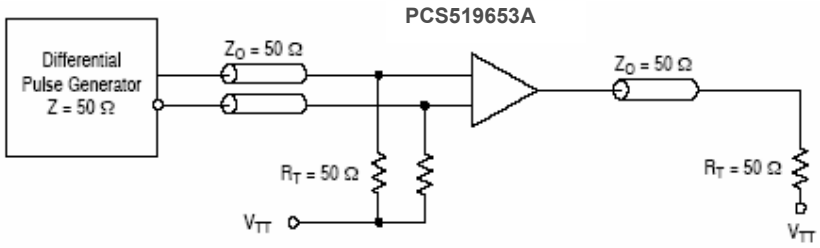
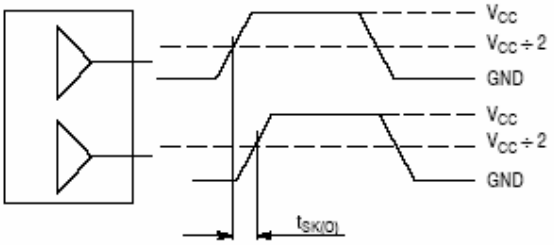


Figure 9. PCLK PCS5I9653A AC test reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-output Skew $t_{SK(O)}$

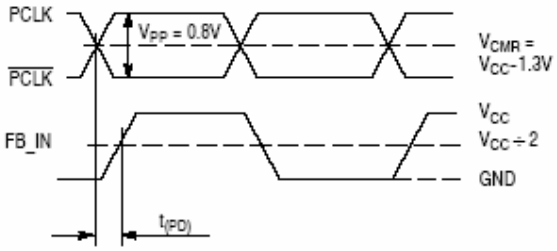
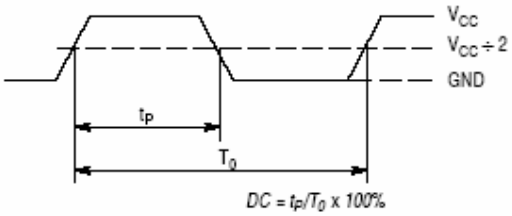
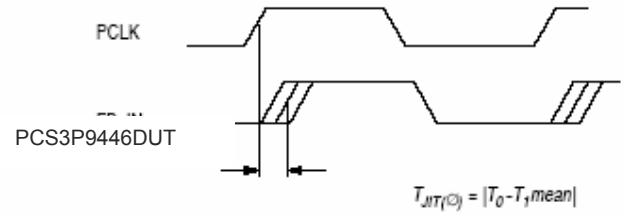


Figure 11. Propagation delay ($t_{(PD)}$, static phase offset) test reference



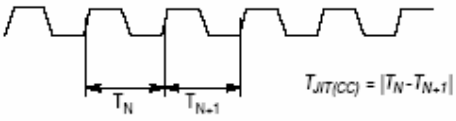
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



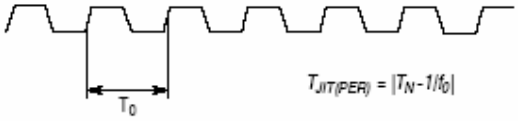
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

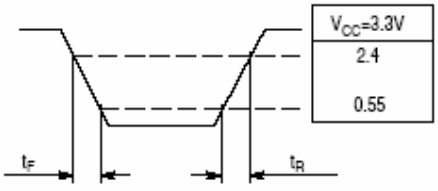
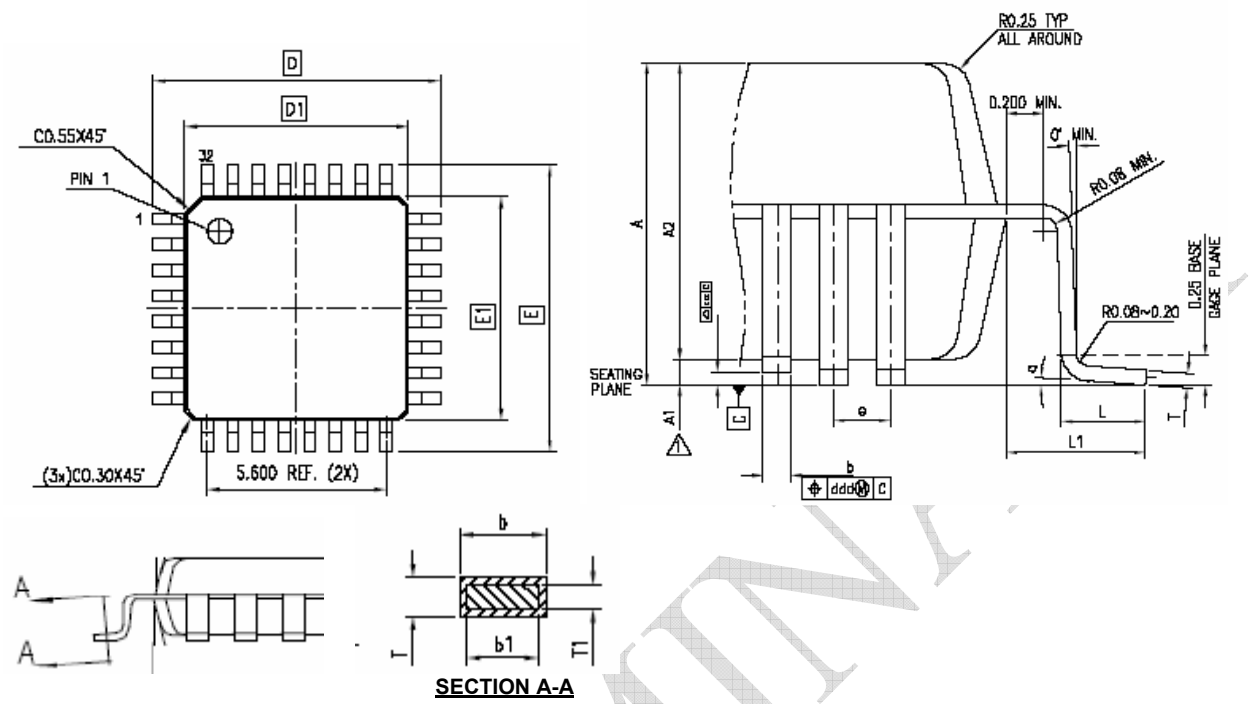


Figure 16. Output Transition Time Test Reference

rev 0.3

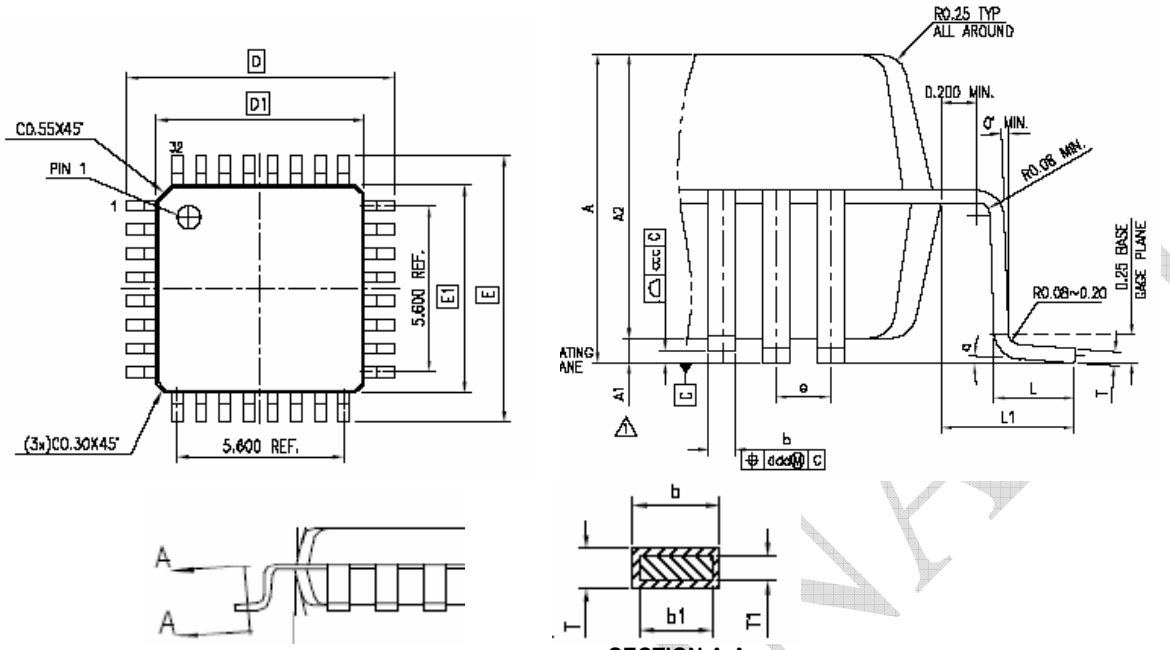
Package Diagram

32-lead TQFP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0472	…	1.2
A1	0.0020	0.0059	0.05	0.15
A2	0.0374	0.0413	0.95	1.05
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.2
a	0°	7°	0°	7°
e	0.031 BASE		0.8 BASE	

32-lead LQFP Package



SECTION A-A

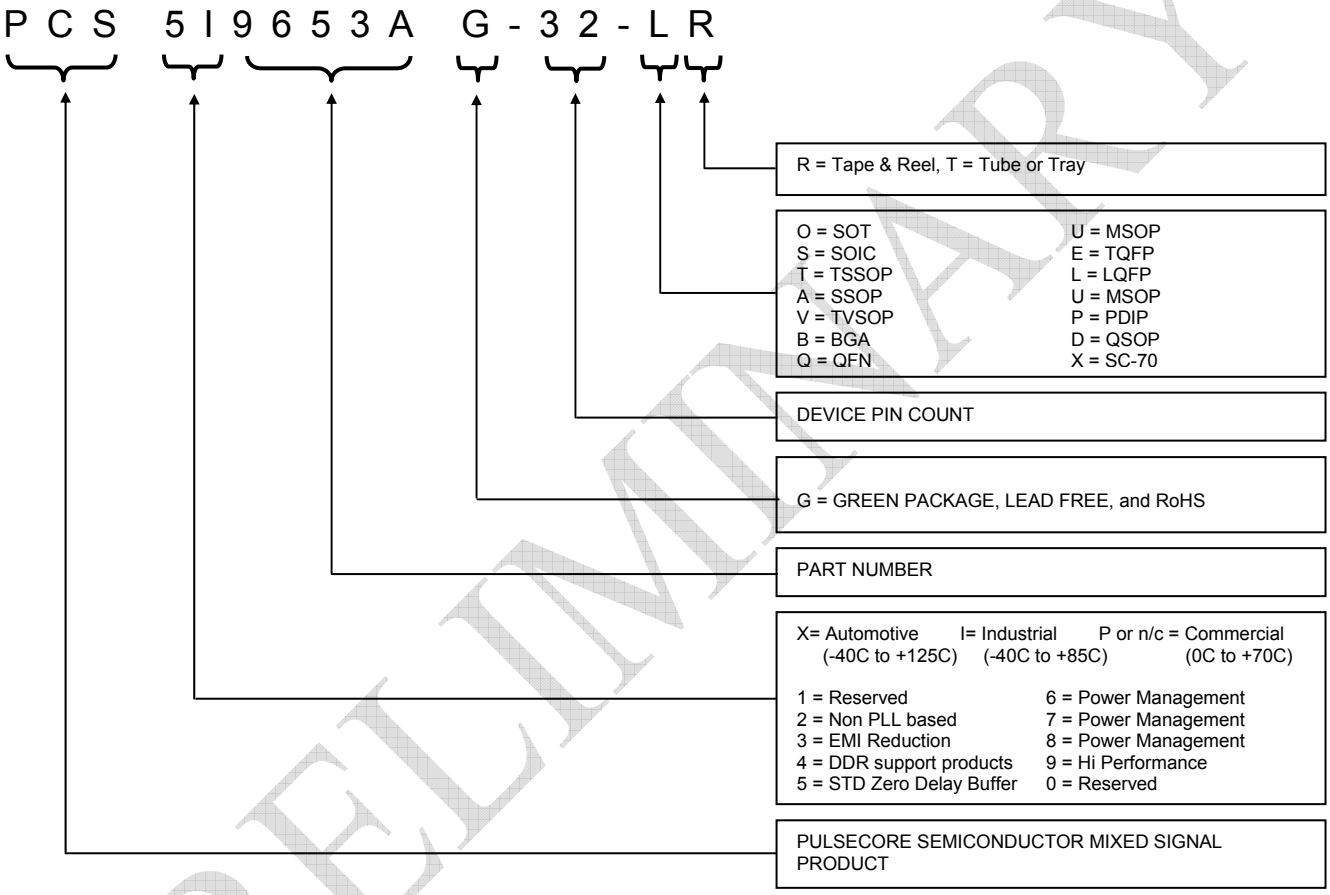
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.0630	…	1.6
A1	0.0020	0.0059	0.05	0.15
A2	0.0531	0.0571	1.35	1.45
D	0.3465	0.3622	8.8	9.2
D1	0.2717	0.2795	6.9	7.1
E	0.3465	0.3622	8.8	9.2
E1	0.2717	0.2795	6.9	7.1
L	0.0177	0.0295	0.45	0.75
L1	0.03937 REF		1.00 REF	
T	0.0035	0.0079	0.09	0.2
T1	0.0038	0.0062	0.097	0.157
b	0.0118	0.0177	0.30	0.45
b1	0.0118	0.0157	0.30	0.40
R0	0.0031	0.0079	0.08	0.20
e	0.031 BASE		0.8 BASE	
a	0°	7°	0°	7°

rev 0.3

Ordering Information

Part Number	Marking	Package Type	Operating Range
PCS5I9653AG-32-ER	PCS5I9653AG	32-pin TQFP, Green	Industrial
PCS5I9653AG-32-LR	PCS5I9653AG	32-pin LQFP –Tape and Reel, Green	Industrial

Device Ordering Information



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Preliminary Information
Part Number: PCS5I9653A
Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003