

# FDMS3662

## N-Channel Power Trench® MOSFET

### 100V, 49A, 14.8mΩ

#### Features

- Max  $r_{DS(on)}$  = 14.8mΩ at  $V_{GS} = 10V$ ,  $I_D = 8.9A$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$
- MSL1 robust package design
- 100% UIL Tested
- RoHS Compliant

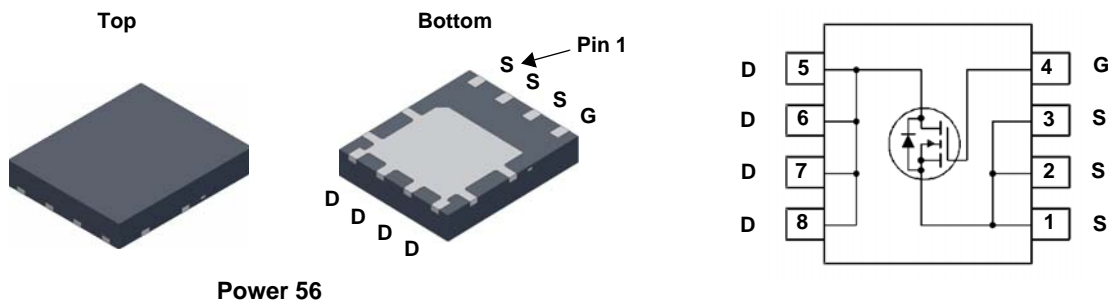


#### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

#### Application

- DC - DC Conversion



#### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	49	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	57	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	8.9	
	-Pulsed	90	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	384	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	104	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS3662	FDMS3662	Power 56	13"	12mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		74		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = 80\text{V}$ ,			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.5	3.5	4.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-10.8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 8.9\text{A}$ $V_{GS} = 10\text{V}, I_D = 8.9\text{A}, T_J = 125^\circ\text{C}$		11.4 19.0	14.8 24.7	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\text{V}, I_D = 8.9\text{A}$		37		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		3470	4620	pF
$C_{oss}$	Output Capacitance			245	325	pF
$C_{rss}$	Reverse Transfer Capacitance			110	165	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$		1.4		$\Omega$

### Switching Characteristics

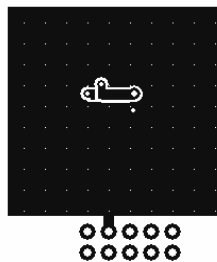
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}, I_D = 8.9\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		25	40	ns
$t_r$	Rise Time			15	26	ns
$t_{d(off)}$	Turn-Off Delay Time			32	52	ns
$t_f$	Fall Time			6	10	ns
$Q_g$	Total Gate Charge at 10V			54	75	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 50\text{V},$ $I_D = 8.9\text{A}$		18		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			15		nC

### Drain-Source Diode Characteristics

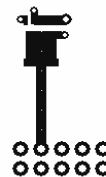
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 8.9\text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{V}, I_S = 2.1\text{A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 8.9\text{A}, di/dt = 100\text{A}/\mu\text{s}$		45	73	ns
$Q_{rr}$	Reverse Recovery Charge			71	115	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.

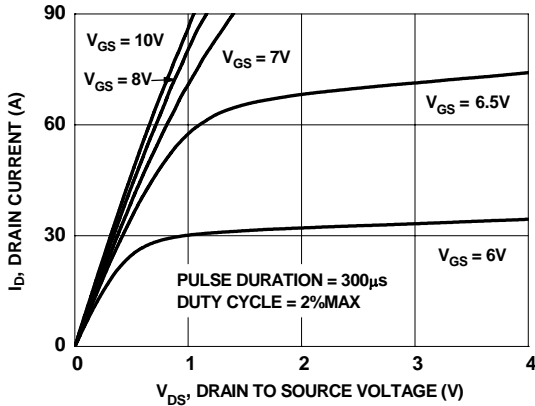


b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

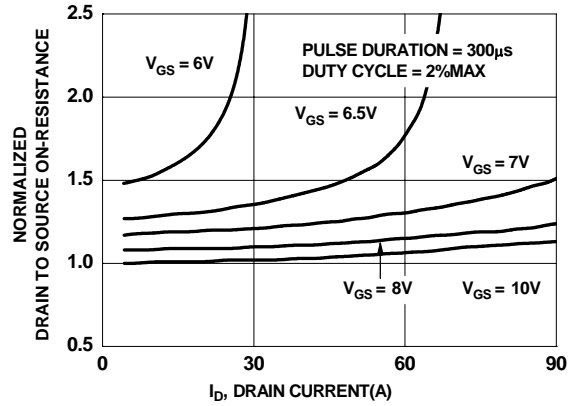
2. Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 16\text{A}$ ,  $V_{DD} = 100\text{V}$ ,  $V_{GS} = 10\text{V}$

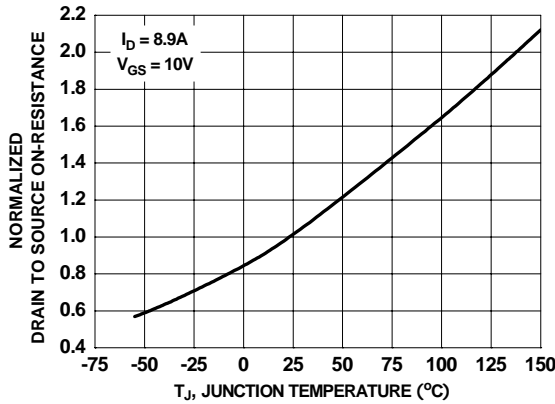
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



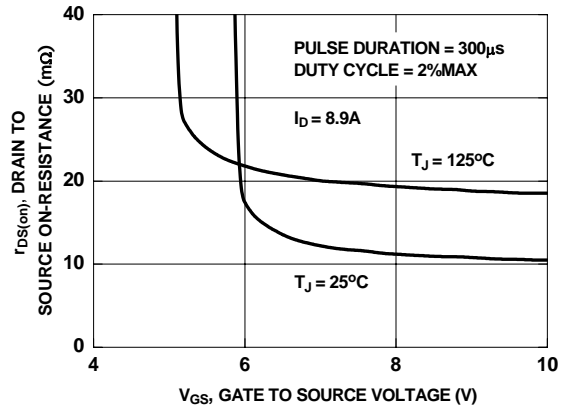
**Figure 1. On-Region Characteristics**



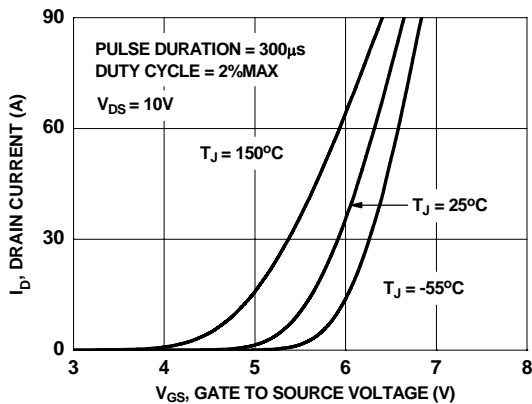
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



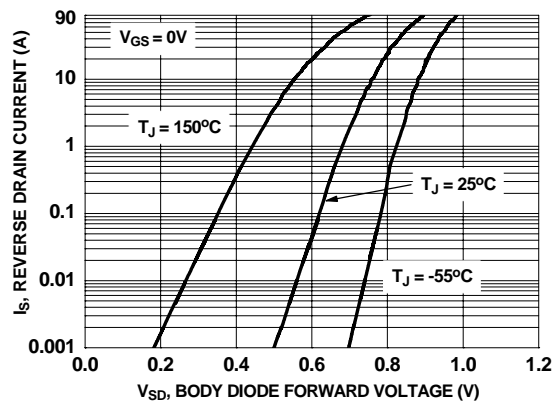
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

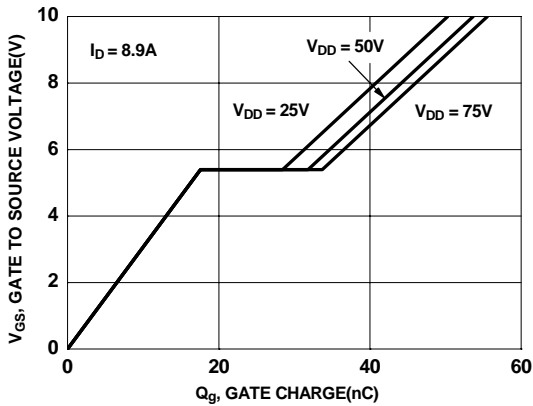


**Figure 5. Transfer Characteristics**

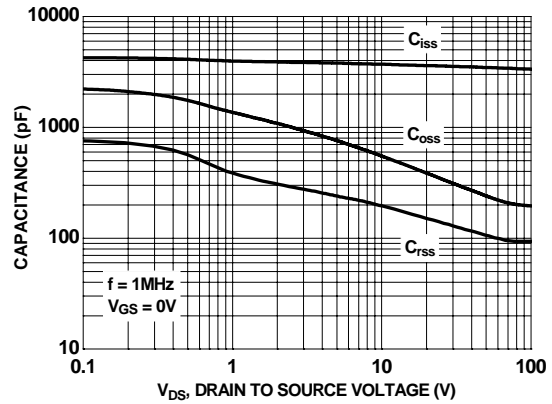


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

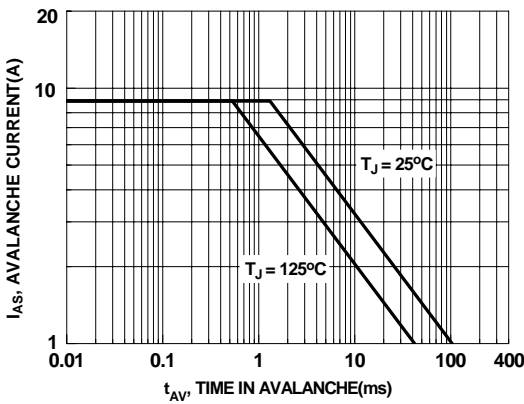
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



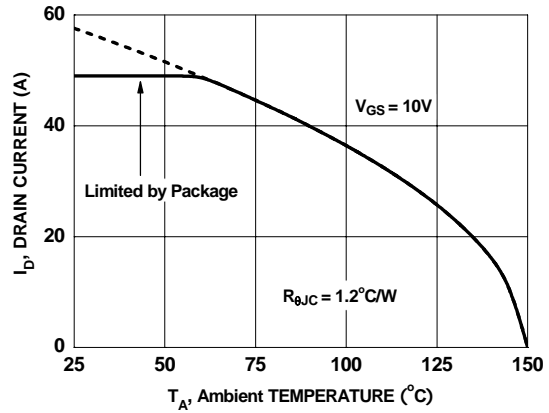
**Figure 7. Gate Charge Characteristics**



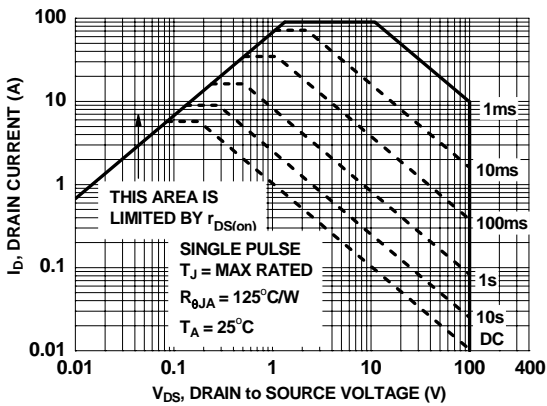
**Figure 8. Capacitance vs Drain to Source Voltage**



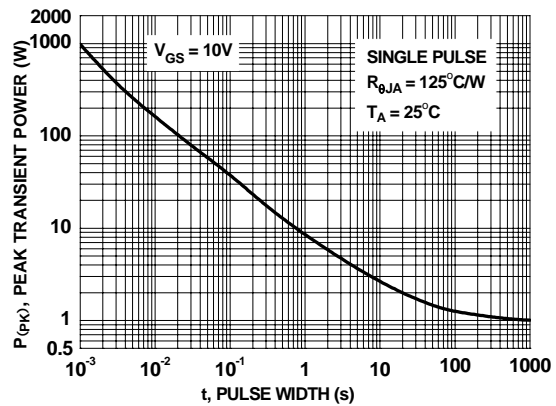
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

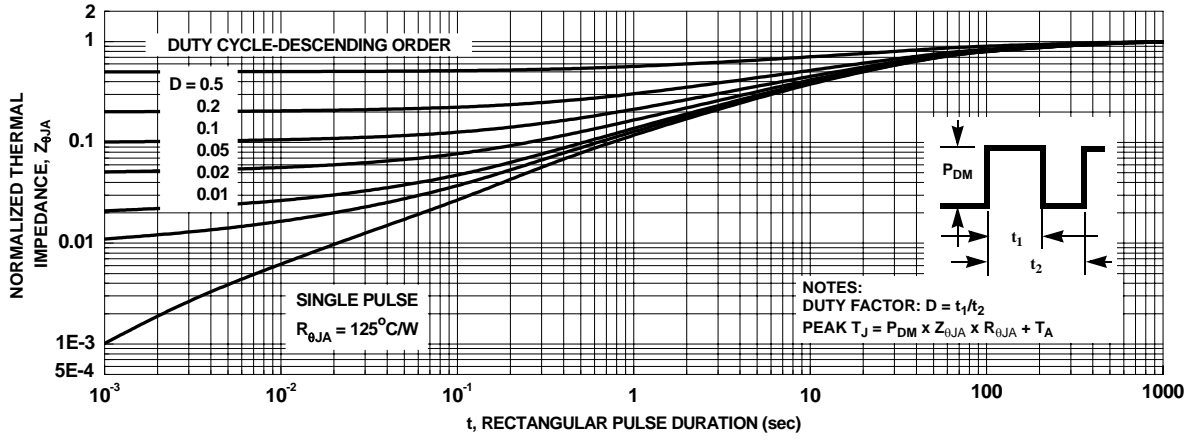


**Figure 11. Forward Bias Safe Operating Area**



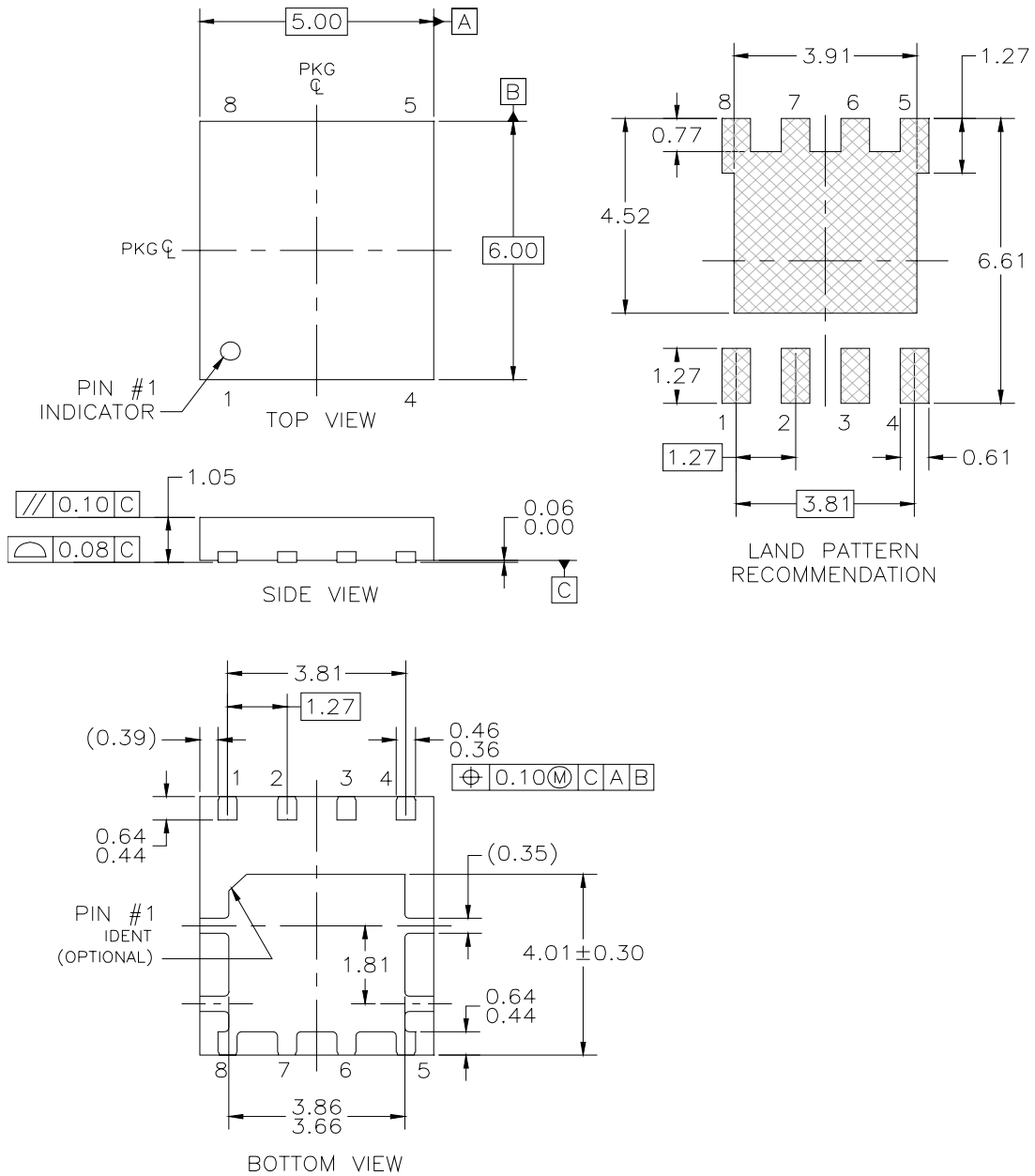
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout








- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) NO JEDEC REFERENCE AS OF FEBRUARY 2006
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994

PQFN08AREVA



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |   |   |   |
|---|---|---|---|
| ACEx®   | FPS™  | PDP-SPM™  | The Power Franchise®  |
| Build it Now™   | F-PFS™  | Power-SPM™  | <b>power</b><br>the franchise   |
| CorePLUS™   | FRFET®  | PowerTrench®  | TinyBoost™  |
| CorePOWER™  | Global Power ResourceSM   | Programmable Active Droop™  | TinyBuck™   |
| CROSSVOLT™  | Green FPS™  | QFET®   | TinyLogic®  |
| CTL™  | Green FPS™ e-Series™  | QS™   | TINYOPTO™   |
| Current Transfer Logic™   | GTO™  | Quiet Series™   | TinyPower™  |
| EcoSPARK®   | IntelliMAX™   | RapidConfigure™   | TinyPVM™  |
| EfficientMax™   | ISOPLANAR™  | Saving our world 1mW at a time™   | TinyWire™   |
| EZSWITCH™ *   | MegaBuck™   | SmartMax™   | µSerDes™  |
|  | MICROCOUPLER™   | SMART START™  |  |
|  | MicroFET™   | SPM®  | UHC®  |
| Fairchild®  | MicroPak™   | STEALTH™  | Ultra FRFET™  |
| Fairchild Semiconductor®  | MillerDrive™  | SuperFET™   | UniFET™   |
| FACT Quiet Series™  | MotionMax™  | SuperSOT™-3   | VCX™  |
| FACT®   | Motion-SPM™   | SuperSOT™-6   | VisualMax™  |
| FAST®   | OPTOLOGIC®  | SuperSOT™-8   |   |
| FastvCore™  | OPTOPLANAR®   | SuperMOS™   |   |
| FlashWriter® *  |  |  |   |

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34