RF25H

Tx ASIC for PCS Applications

The RF25H Tx Application-Specific Integrated Circuit (ASIC) is a single-mode transmitter intended to be used in the Personal Communications System (PCS) band.

The RF25H device includes the following functional blocks:

- Upconverter with RF gain control.
- Power Amplifier (PA) driver.

The RF25H Tx ASIC is available in both a 48-pin Thin Quad Flat Pack (TQFP) package and a 32-pin Land Grid Array (LGA) 5x5 package. The device package and pinout for the 48-pin TQFP are shown in Figure 1. Figure 2 shows the device pinout for the 32-pin LGA. A block diagram of the RF25H is shown in Figure 3.

Features

- Power saving operation in gated output power mode.
- 14 dB RF gain control to compensate for the gain variation of off-chip components.
- PCS band driver.
- 48-pin TQFP package with downset paddle. Optional 32-pin LGA 5x5 package.

Applications

- Code Division Multiple Access (CDMA) mode in the PCS band:
  - US-PCS
  - K-PCS

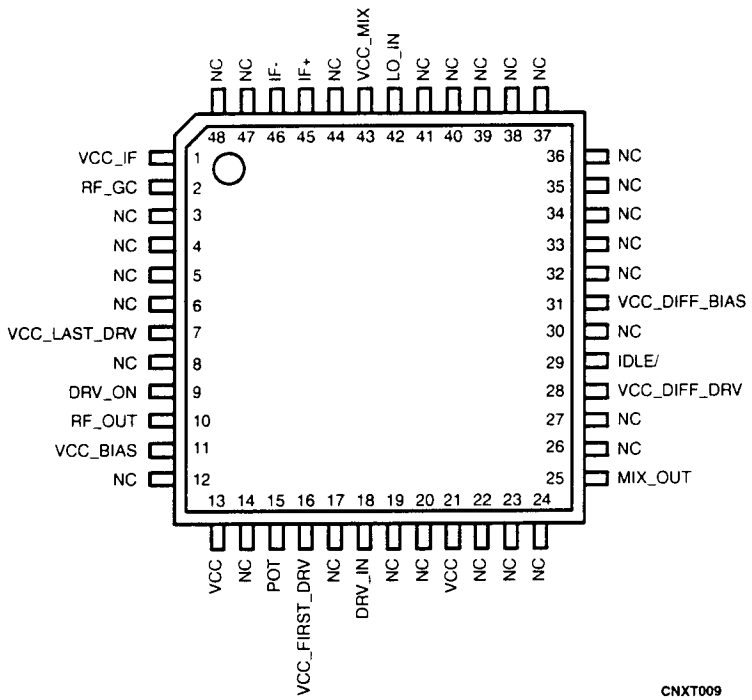


Figure 1. RF25H Tx ASIC Pinout – 48-Pin TQFP Package

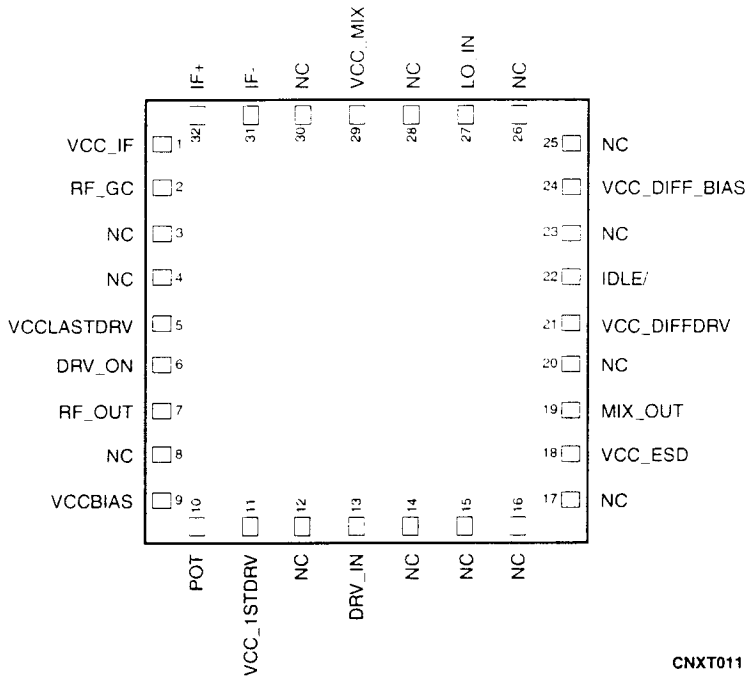


Figure 2. RF25H Tx ASIC Pinout – 32-Pin LGA 5x5 Package

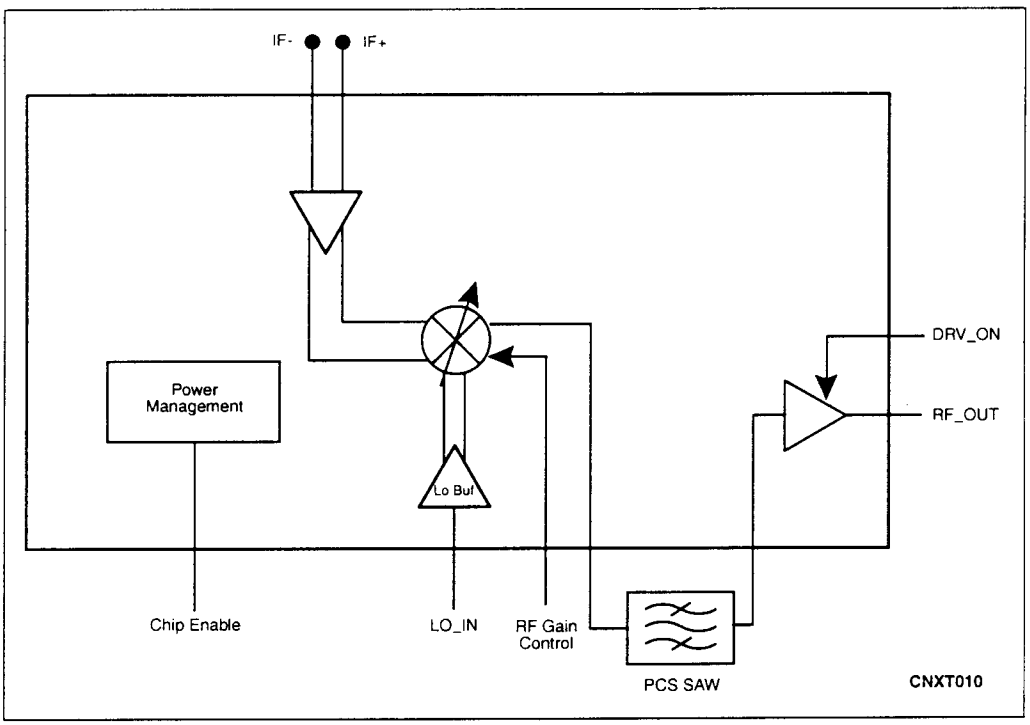


Figure 3. RF25H Tx ASIC Block Diagram

Technical Description

The RF25H is a CDMA transmitter for the PCS band. The chip consists of a variable gain upconverter and a PA driver.

Upconverter. The PCS variable gain upconverter receives the IF signal from the VGA after passing through an external filter. The upconverter uses an external LO controlled by an external PLL. The conversion gain control in the upconverter can be used to calibrate out any part-to-part and temperature gain variation in the transmit path. The DRV_ON command deactivates the driver during no transmission status. The output RF signal is sent to an output pin to be filtered before driver amplification.

PA Driver. The PA driver takes its input from the upconverter after passing through an image rejection filter. The driver amplifies the signal and sends it to an external PA.

The DRV_ON command is used during gated output power mode to deactivate the drivers in periods of no transmission. A Surface Acoustic Wave (SAW) filter for noise and image rejection should be placed between the driver and the external PA.

Electrical and Mechanical Specifications

The signal pin assignments and functional pin descriptions for the 48-pin TQFP and 32-pin LGA package are found in Tables 1 and 2, respectively. The absolute maximum ratings of the RF25H are provided in Table 3, the recommended operating conditions are specified in Table 4, and electrical specifications are provided in Table 5. The package dimensions for the 48-pin TQFP and the 32-pin LGA are provided in Figures 4 and 5, respectively. Figure 6 provides the tape and reel dimensions for the 48-pin TQFP and Figure 7 provides the tape and reel dimensions for the 32-pin LGA..

ESD Sensitivity

The RF25H is a Class 1 device. The following extreme Electrostatic Discharge (ESD) precautions are required according to the Human Body Model (HBM):

- Protective outer garments.
- Handle device in ESD safeguarded work area.
- Transport device in ESD shielded containers.
- Monitor and test all ESD protection equipment.

The HBM ESD withstand threshold value, with respect to ground, is ±2.5 kV. The HBM ESD withstand threshold value, with respect to VDD (the positive power supply terminal) is also ±2.5 kV.

Table 1. RF25H Signal Description – 48-Pin TQFP (1 of 2)

Pin #	Name	Description
1	VCC_IF	Supply voltage for the IF mux and bias circuitry.
2	RF_GC	The gain control pin for RF upconverter. A DC voltage of 1 to 2.2 V is needed to cover the mixer RF range.
3	NC	No connection.
4	NC	No connection.
5	NC	No connection.
6	NC	No connection.
7	VCC_LAST_DRV	Supply voltage for the PCS driver amplifier. This pin can be used to turn the last driver on and off for a 24 dB gain step.
8	NC	No connection.
9	DRV_ON	This is the driver control signal. When the pin is low, the driver is deactivated during no transmission. During transmission the pin should be high to enable the driver.
10	RF_OUT	This is the output pin for the PCS RF signal. The pin is connected to the output of the PCS driver amplifier. Impedance matching is required.
11	VCC_BIAS	Supply voltage for biasing circuits of various blocks.
12	NC	No connection.
13	VCC	Connect to high (VCC).
14	NC	No connection.
15	POT	This pin is connected to an external resistor. The value of the resistor varies the bias current of the PCS driver, which affects gain and ACPR.
16	VCC_FIRST_DRV	Supply voltage for the first amplifier in the PCS driver block.
17	NC	No connection.
18	DRV_IN	The PCS driver input pin connected to the RF input of the PCS band driver. The input signal should pass through a SAW filter before being connected to the driver. Impedance matching is required.
19	NC	No connection.
20	NC	No connection.
21	VCC	Supply voltage for ESD diodes.
22	NC	No connection.
23	NC	No connection.
24	NC	No connection.

Table 1. RF25H Signal Description – 48-Pin TQFP (2 of 2)

Pin #	Name	Description
25	MIX_OUT	This pin is connected to the RF output of the PCS upconverter. This pin needs impedance matching. The RF output signal should be routed through an image rejection filter before being connected to the driver input.
26	NC	No connection.
27	NC	No connection.
28	VCC_DIFF_DRV	Supply voltage for a differential amplifier in the upconverter block.
29	IDLE/	This is the upconverter enable signal. When the input is low, the chip is disabled. When the input is high, the chip is enabled.
30	NC	No connection.
31	VCC_DIFF_BIAS	Supply voltage.
32	NC	No connection.
33	NC	No connection.
34	NC	No connection.
35	NC	No connection.
36	NC	No connection.
37	NC	No connection.
38	NC	No connection.
39	NC	No connection.
40	NC	No connection.
41	NC	No connection.
42	LO_IN	This is the input pin for the local oscillator for the PCS band. It is internally matched.
43	VCC_MIX	Supply voltage for the mixer in the upconverter block and for the LO buffer.
44	NC	No connection.
45	IF+	This is the balanced input to the upconverter. The DC bias is set internally.
46	IF-	Same as pin 45, except a complementary input.
47	NC	No connection.
48	NC	No connection.

Table 2. RF25H Signal Description – 32-Pin 5x5 LGA

Pin #	Name	Description
1	VCC_IF	Supply voltage for the IF mux and bias circuitry.
2	RF_GC	The gain control pin for RF upconverter. A DC voltage of 1 to 2.2 V is needed to cover the mixer RF range.
3	NC	No connection.
4	NC	No connection.
5	VCC_LAST_DRV	Supply voltage for the PCS driver amplifier. This pin can be used to turn the last driver on and off for a 24 dB gain step.
6	DRV_ON	This is the driver control signal. When the pin is low, the driver is deactivated during no transmission. During transmission the pin should be high to enable the driver.
7	RF_OUT	This is the output pin for the PCS RF signal. The pin is connected to the output of the PCS driver amplifier. Impedance matching is required.
8	NC	No connection.
9	VCC_BIAS	Supply voltage for biasing circuits of various blocks.
10	POT	This pin is connected to an external resistor. The value of the resistor varies the bias current of the PCS driver, which affects gain and ACPR.
11	VCC_FIRST_DRV	Supply voltage for the first amplifier in the PCS driver block.
12	NC	No connection.
13	DRV_IN	The PCS driver input pin connected to the RF input of the PCS band driver. The input signal should pass through a SAW filter before being connected to the driver. Impedance matching is required.
14	NC	No connection.
15	NC	No connection.
16	NC	No connection.
17	NC	No connection.
18	VCC_ESD	Supply voltage for ESD diodes.
19	MIX_OUT	This pin is connected to the RF output of the PCS upconverter. This pin needs impedance matching. The RF output signal should be routed through an image rejection filter before being connected to the driver input.
20	NC	No connection.
21	VCC_DIFF_DRV	Supply voltage for a differential amplifier in the upconverter block.
22	IDLE/	This is the upconverter enable signal. When the input is low, the chip is disabled. When the input is high, the chip is enabled.
23	NC	No connection.
24	VCC_DIFF_BIAS	Supply voltage
25	NC	No connection.
26	NC	No connection.
27	LO_IN	This is the input pin for the local oscillator for the PCS band. It is internally matched.
28	NC	No connection.
29	VCC_MIX	Supply voltage for the mixer in the upconverter block and for the LO buffer.
30	NC	No connection.
31	IF-	This is the balanced input to the upconverter. The DC bias is set internally.
32	IF+	Same as pin 31, except a complementary input.

Table 3. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage (VCC)	–0.3	5.0	V
Input voltage range	–0.3	VCC	V
Power dissipation	--	600	mW
Ambient operating temperature	–30	+80	°C
Storage temperature	–40	+125	°C

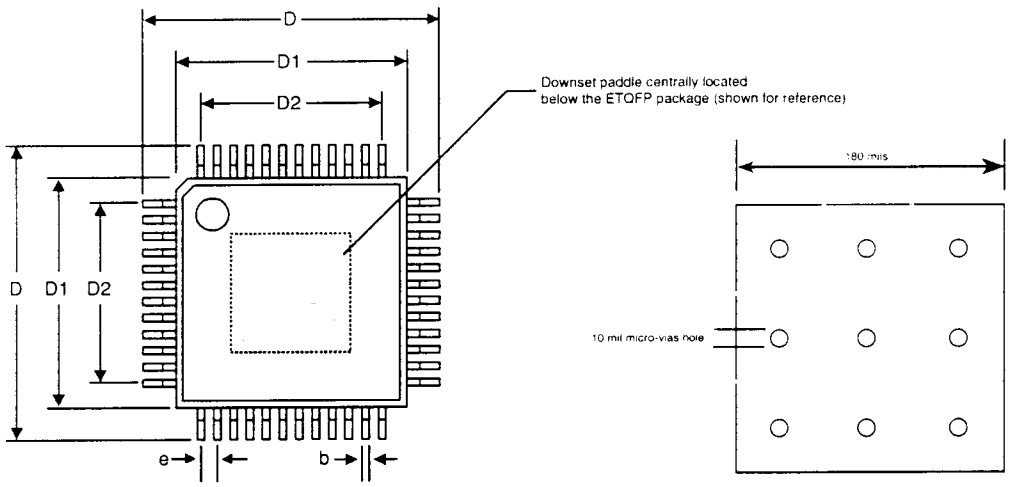
Table 4. Recommended Operating Conditions

Parameter	Min	Typical	Max	Units
Supply voltage	3.0	3.3	3.6	V
Logic level high	VCC – 0.5			V
Logic level low			0.5	V
Supply current in 1900 MHz CDMA @ 8 dBm		*** TBD ***		mA
Supply current in 1900 MHz CDMA (driver on = off)		*** TBD ***		mA
Supply current in sleep mode (chip enable = off, driver on = off)			10	µA

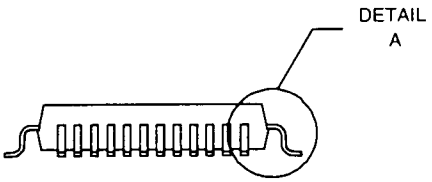
Table 5. RF25H Tx ASIC Electrical Specifications

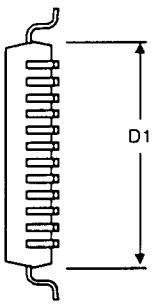
(TA = 25° C, VCC = 3.3 V, PLO = –10 dBm, input externally matched)

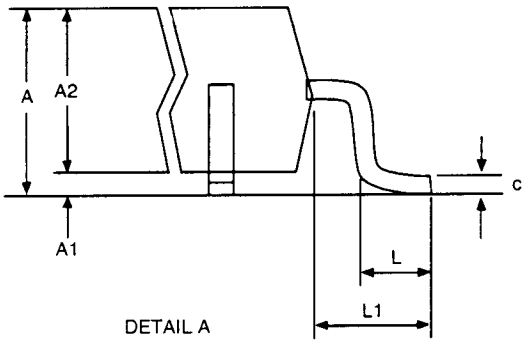
Parameter	Symbol	Test Condition	Min	Typical	Max	Units
PCS Variable-Gain Upconverter						
LO frequency range			1600		1800	MHz
LO input return loss (reference to 50 Ω)				–10		dB
Terminating resistor across IF inputs			485	510	535	Ω
Output frequency			1700		1910	MHz
Maximum conversion gain			17	18		dB
Minimum conversion gain				–6		dB
Output power at maximum gain				–3		dBm
ACPR in 30 KHz at 1.25 MHz offset @ –6 dBm output				–56	–54	dBc
ACPR in 1 MHz at 2.75 MHz offset @ –6 dBm output				–56	–54	dBc
Noise figure at maximum gain				9	10	dB
Noise figure @ 13 dB gain				13		dB
LO to RF leakage @ maximum gain, LO = –15 dBm				–35		dBm
PCS PA Driver						
Input return loss (reference to 50 Ω)				–15		dB
Output frequency			1700		1910	MHz
Gain (@ POT1800 = 100 Ω)			16	18		dB
Output power level with 1800 MHz mixer @ maximum gain			8	9.5		dBm
ACPR in 30 KHz band at 1.25 MHz offset @ 9 dBm output				–52	–51	dBc
ACPR in 1 MHz band at 2.75 MHz offset @ 9 dBm output				–52	–51	dBc
Noise figure				6	7	dB



Dimensional sketch of the ground pattern for the downset paddle







Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2	1.35	1.45	0.0528	0.0571
D	8.85	9.15	0.3484	0.3602
D1	6.95	7.05	0.2736	0.2776
D2		5.5 REF		0.2165 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.500 REF		0.0197 REF
b		0.220 REF		0.0087 REF
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.10 MAX		0.0039 MAX
Ref: 48-PIN ETQFP (GP00-D283) **				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

** The package has a downset paddle to provide good RF ground contact and needs to be soldered to the ground plane on the PCB.

NOTE: Package conforms to Jedec Standard MO-136

C085

Figure 4. RF25H Tx ASIC Package Dimensions – 48-Pin TQFP package With Downset Paddle

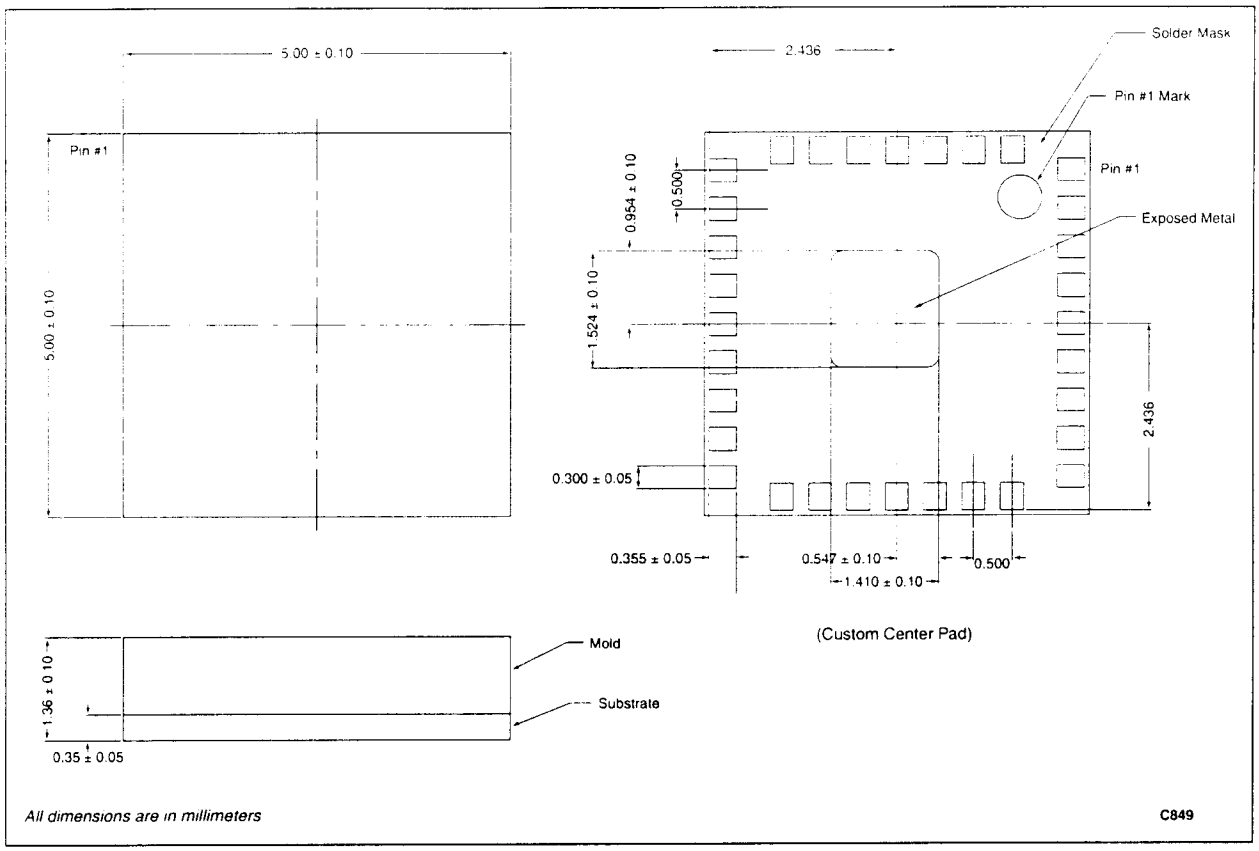


Figure 5. RF25H Tx ASIC Package Dimensions – 32-Pin LGA 5x5 Package

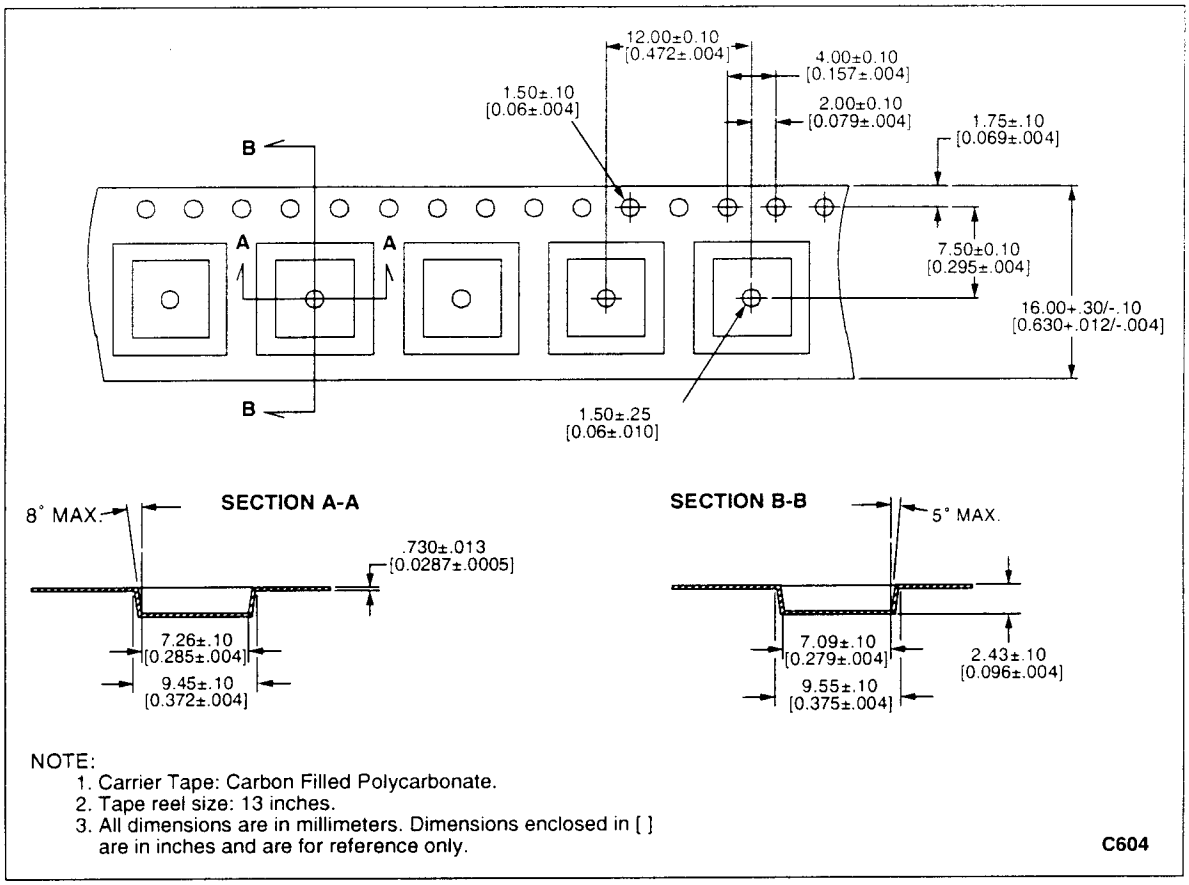


Figure 6. 48-Pin TQFP Tape and Reel Dimensions

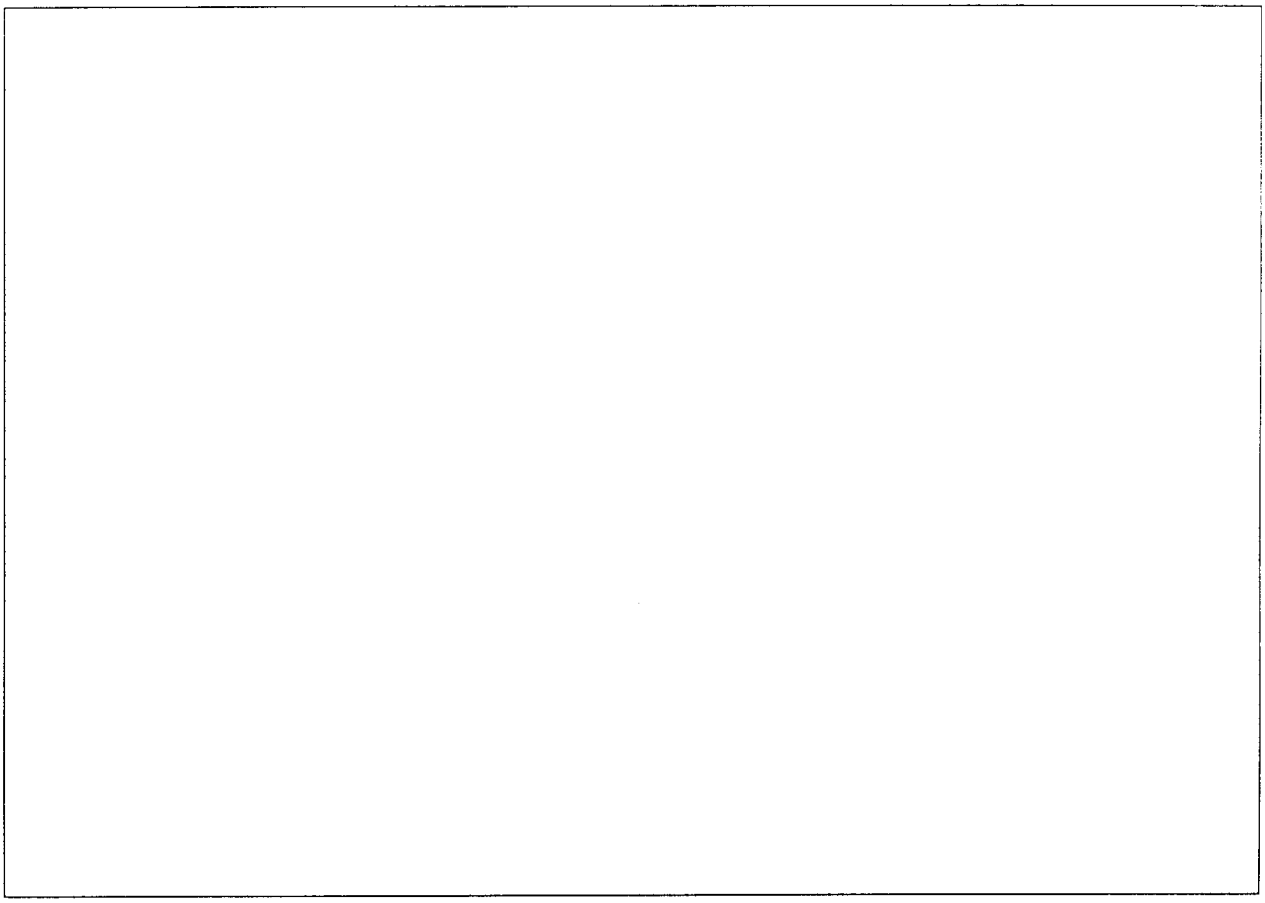


Figure 7. 32-Pin LGA 5x5 Tape and Reel Dimensions

Ordering Information

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