NCS8353

Stereo 20W/Ch Class D Audio Power Amplifier with Programmable Power Limit and Selectable Gain

The NCS8353 is a stereo Class D audio power amplifier capable of delivering a continuous power of up to 20 W/ch into an 8 Ω bridge tied load (BTL). It can be powered from the existing 24 V rail in Flat Panel Television (FPTV) systems. The high efficiency of the NCS8353, 86%, reduces the requirement of an external heat sink when driving high power.

The digital power limit feature can program the output power limit at 10 W, 12 W, 15 W, or 20 W/ch, allowing the NCS8353 to be a single system solution in FPTV audio applications.

The NCS8353 includes a digital power limit feature. The digital power limiter quickly reduces the internal gain of the amplifier when high amplitude signals would cause excessive clipping on the output.

The NCS8353 minimizes pop and click artifacts in the audio system by reducing voltage and current transients during power supply cycling, entering or recovering from shutdown, and mute. The shutdown feature reduces the quiescent current draw of the amplifier to 100 μA typical. The mute feature ensures that audio is not present at the output during audio source switching.

The gain of the NCS8353 is programmed via two gain pins, G0 and G1, allowing four selectable ranges: 20 dB, 26 dB, 32 dB, and 36 dB.

Auto recovery short circuit and over temperature protection circuitry are incorporated to ensure device functionality after short circuit and high temperature events occur.

Features

- Powered from 8 V to 26 V to include FPTV Backlight Supply (24 V ±5%)
- Digital Power Limiter Controlled by Two External bits: 10 W, 12 W, 15 W, or 20 W per Channel
  - Allows for Maximum System Flexibility
  - Reduces Distortion with Excessive Inputs
- Pop and Click Suppression
- Selectable Gain: 20 dB, 26 dB, 32 dB, 36 dB
- High Efficiency Eliminates the Need for External Heat Sink
- Low Supply Current: I_Q = 100 μA Typical During Shutdown at 12 V
- Mute Function
- Auto−recovery Short−Circuit Protection
- Over Temperature Protection
- Fully Differential Architecture
- This is a Pb−Free Device

Typical Applications

- Flat Panel Television (FPTV)
- Powered Speakers

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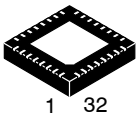
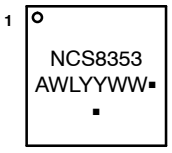


QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAMS



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCS8353MNTXG	QFN32 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

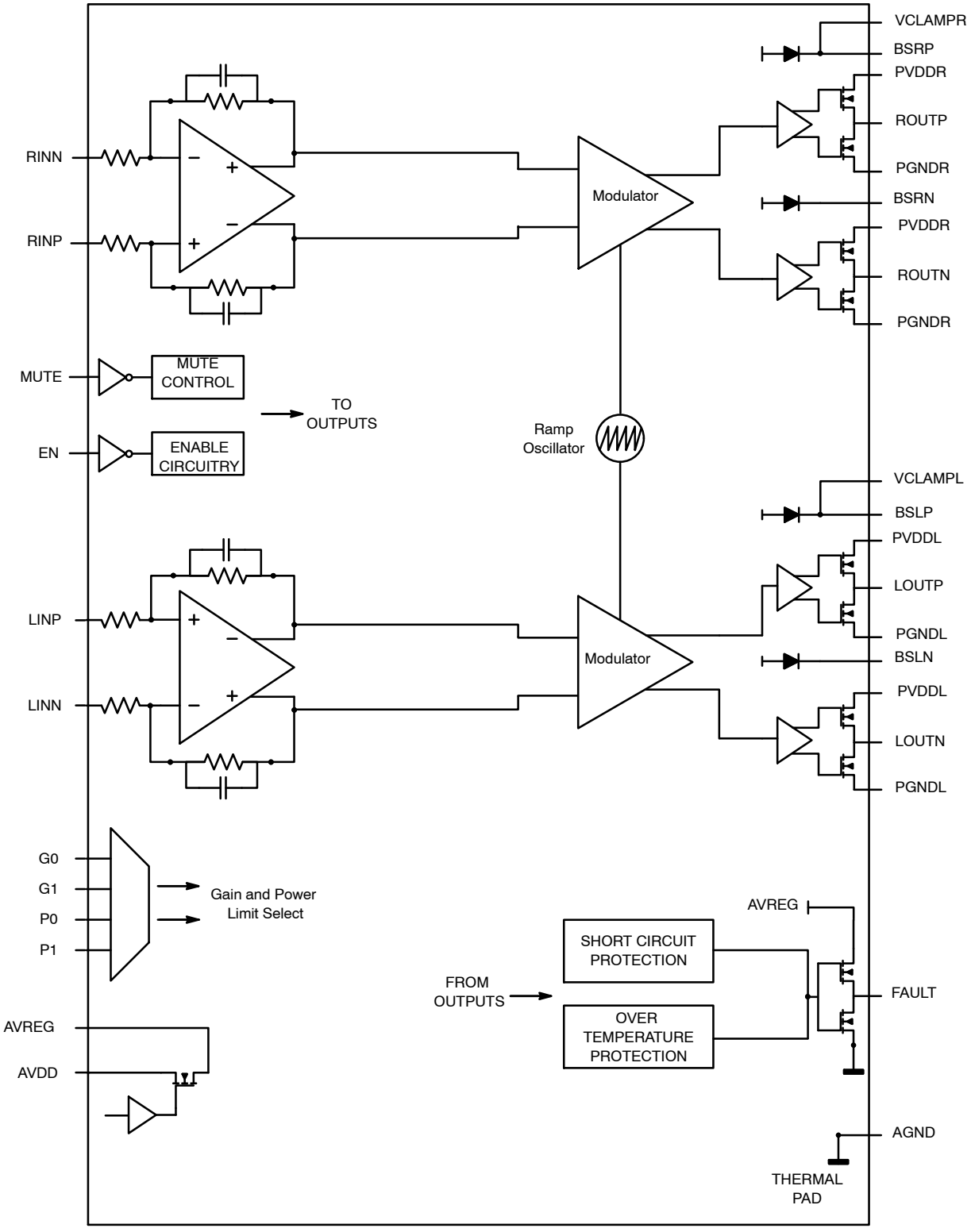


Figure 1. NCS8353 Basic Connections

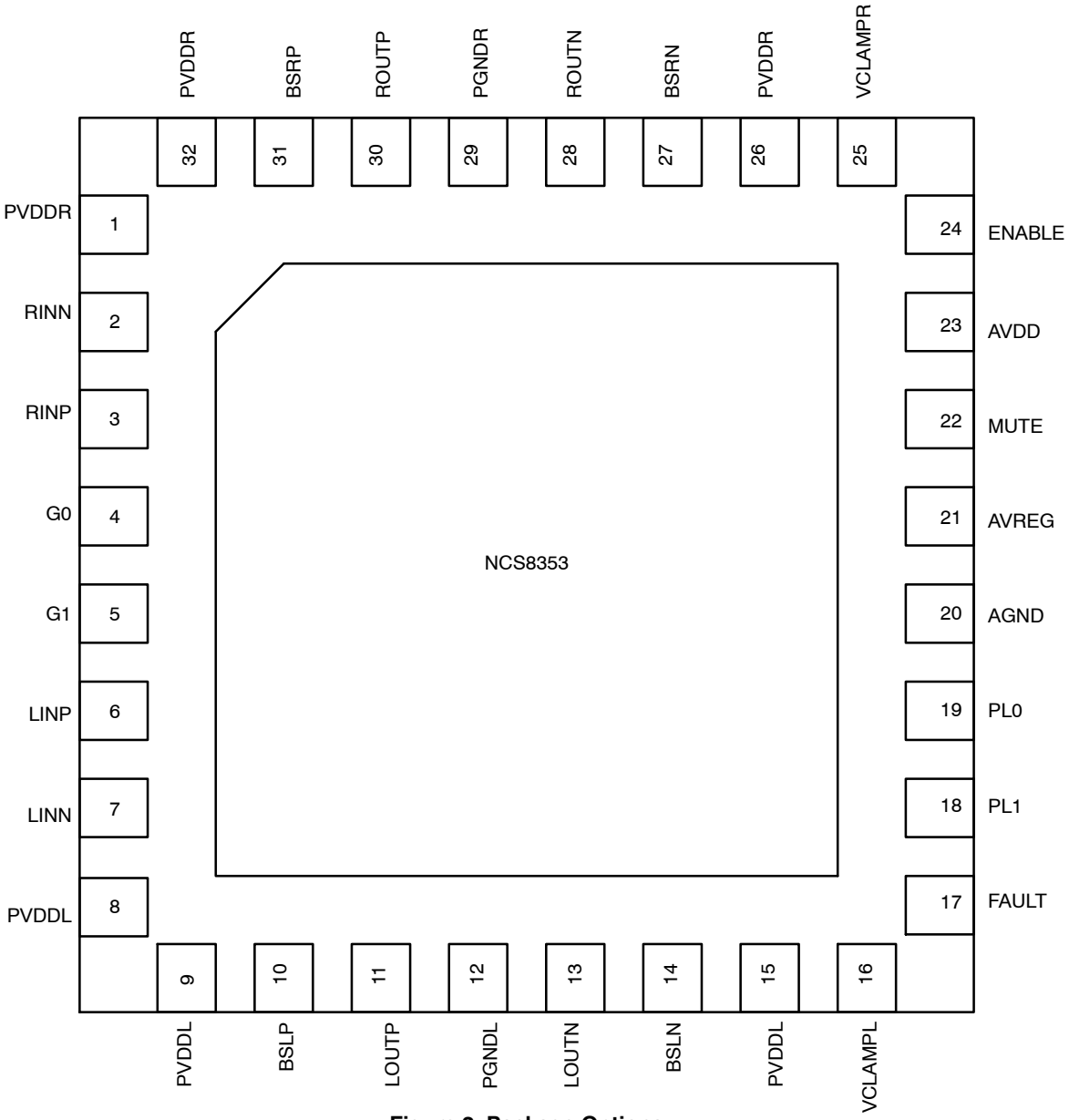


Figure 2. Package Options

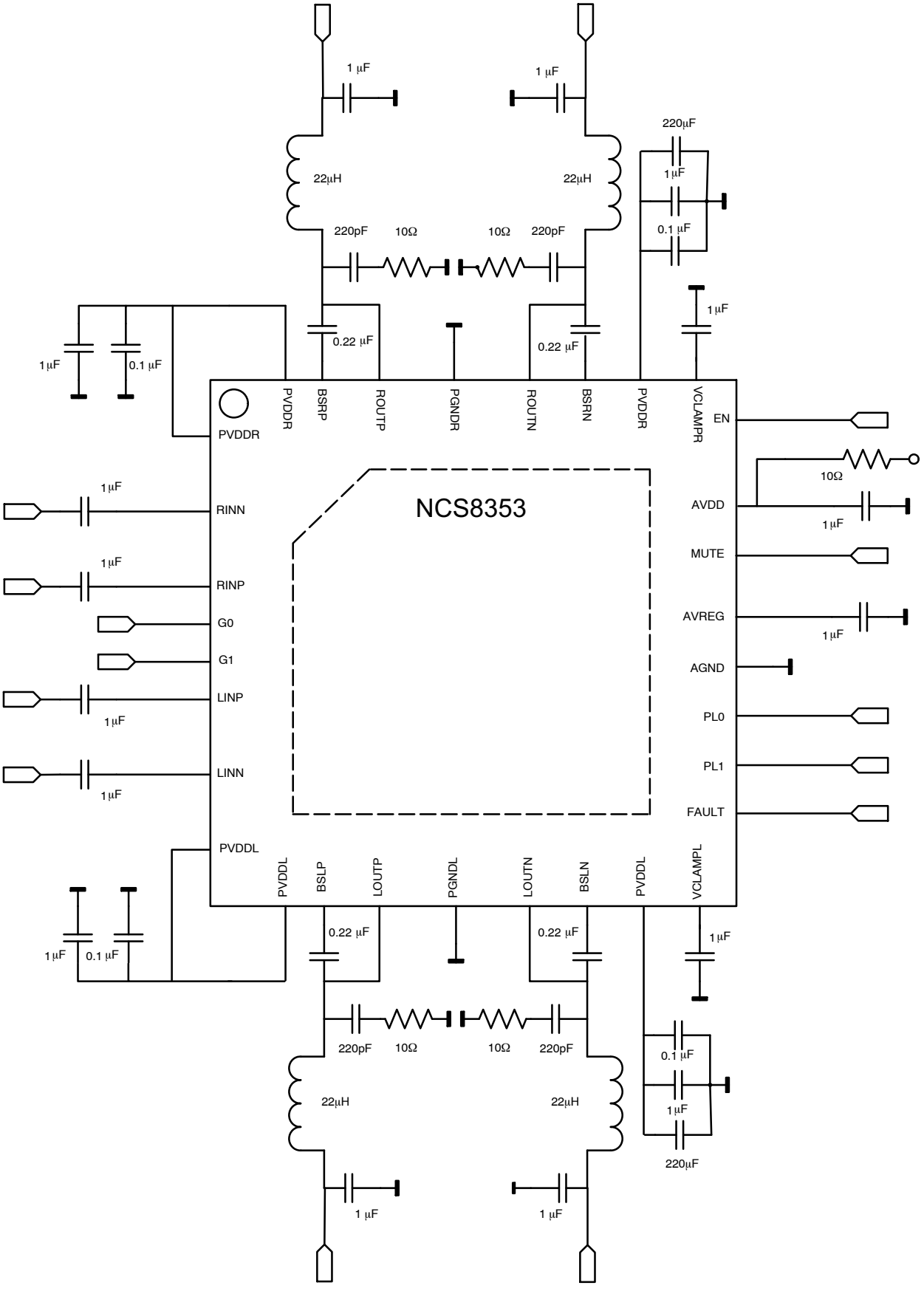


Figure 3. Typical Application Connection for 8 Ω Speaker

PIN FUNCTION AND DESCRIPTION

Pin#	Name	Input/output	Description
1	PVDDR	Power	Power supply for right channel.
2	RINN	Input	Right Input − Negative.
3	RINP	Input	Right Input − Positive.
4	G0	Input	LSB Gain Setting.
5	G1	Input	MSB Gain Setting.
6	LINP	Input	Left Input Positive.
7	LINN	Input	Left Input Negative.
8	PVDDL	Power	Power supply for left channel.
9	PVDDL	Power	Power supply for left channel.
10	BSLP	−	Bootstrap for positive left speaker output.
11	LOUTP	Output	Positive Left Speaker Output.
12	PGNDL	Ground	Power ground for left channel.
13	LOUTN	Output	Negative Left Speaker Output.
14	BSLN	−	Bootstrap for negative left speaker output.
15	PVDDL	Power	Power supply for left channel.
16	VCLAMPL	−	Internal voltage supply for left channel bootstrap capacitor.
17	FAULT	Output	TTL compatible output. Asserts HIGH during thermal shutdown or short circuit conditions.
18	PL1	Input	MSB − Power Limit.
19	PL0	Input	LSB − Power Limit.
20	AGND	Ground	Analog ground reference.
21	AVREG	Output	Regulator output voltage.
22	MUTE	Input	TTL compatible input. Mutes the device when a logic HIGH is present.
23	AVDD	Power	Analog high voltage supply.
24	ENABLE	Input	TTL compatible input. Enable for right and left channels when logic HIGH is present.
25	VCLAMPR	−	Internal voltage supply for right channel bootstrap capacitor.
26	PVDDR	Power	Power supply for right channel.
27	BSRN	−	Bootstrap for right negative output.
28	ROUTN	Output	Negative right speaker output.
29	PGNDR	Ground	Power ground for right channel.
30	ROUTP	Output	Positive right speaker output.
31	BSRP	−	Bootstrap for right positive output.
32	PVDDR	Power	Power supply for right channel.

MAXIMUM RATINGS TABLE

Parameter	Symbol	Rating	Unit
Power Supply Voltage (PVDDR, PVDDL)	P_{VDD}	30	V
Analog Supply Voltage (AVDD)	A_{VDD}	30	V
Input voltage (ENABLE, G0, G1, RINN, RINP, LINN, LINP)	V_{in}	−0.3 V to AV_{reg}	V
Input voltage Mute function (MUTE)	V_{in}	−0.3 V to 3.6 V	V
Output Current (ROUTP, ROUTN, LOUTP LOUTN)	I_O	4.7	A
Maximum Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	160	°C
Junction−to−Air Thermal Resistance QFN−32 (Note 1)	$R_{\theta JA}$	31.4	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Board size: 5” x 4”, 4−layer, 2 oz copper.

RECOMMENDED OPERATING CONDITIONS, T_A = 25°C unless otherwise noted

Specification Name	Conditions	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range		P_{VDD}	8		26	V
Analog Supply Voltage range		A_{VDD}	8		26	V
High−level input voltage	G0, G1, PL0, PL1, ENABLE, MUTE	V_{IH}	2	3.3	3.6	V
Low−level input voltage	G0, G1, PL0, PL1, ENABLE, MUTE	V_{IL}			0.8	V
High Level Output Voltage	Fault, I_{OH} = +1 mA	V_{OH}	A_{VREG} − 0.4			V
Low Level Output Voltage	Fault, I_{OL} = −1 mA	V_{OL}			A_{GND} + 0.4	V
Internal Oscillator Frequency		f_{OSC}		315		kHz

DC ELECTRICAL CHARACTERISTICS, AVDD = PVDDR = PVDDL = 12 V, R_L = 8 Ω, T_A = 25°C unless otherwise noted

Specification Name	Conditions	Symbol	Min	Typ	Max	Unit
Differential Output Offset Voltage	Inputs AC GND, C_{IN} = 1 μF, A_V = 20 dB, Measured differentially	V_{OSDIFF}		15	50	mV
5.0 V Internal Regulator	No load, C_{reg} = 1 μF	A_{VREG}	4.5	5	5.5	V
Voltage input common mode range	Inputs AC coupled, C_{IN} = 1 μF, V_{bias} = 2.15 V	V_{ICR}	A_{GND} + 0.35		A_{VREG} – 1.35	V
Quiescent Current	No load, No filter	I_Q		28	42	mA
Shutdown Quiescent Current	No load, No filter, ENABLE ≤ 0.8 V	I_{QSHDN}		100	200	μA
On Resistance Drain to Source	Io = 500 mA	R_{DSon}		360		mΩ
Gain	G0 = G1 ≤ 0.8 V	A_V	19	20	21	dB
	G0 ≤ 0.8 V, G1 ≥ 2 V		25	26	27	
	G0 ≥ 2 V, G1 ≤ 0.8 V		31	32	33	
	G0 = G1 ≥ 2 V		35	36	37	
Gain Matching	R_{OUTN} / R_{OUTP}, L_{OUTN} / L_{OUTP}			0.5		dB
Turn on time	ENABLE ≥ 2 V	t_{ON}		450		ms
Turn off time	ENABLE ≤ 0.8 V	t_{OFF}		150		ms

DC ELECTRICAL CHARACTERISTICS, AVDD = PVDDR = PVDDL = 24 V, R_L = 8 Ω, T_A = 25°C unless otherwise noted

Specification Name	Conditions	Symbol	Min	Typ	Max	Unit
Differential Output Offset Voltage	Inputs AC GND, C_{IN} = 1 μF, A_V = 20 dB, Measured differentially	V_{OSDIFF}		15	50	mV
5.0V Internal Regulator	No load, C_{reg} = 1 μF	A_{VREG}	4.5	5	5.5	V
Voltage input common mode range	Inputs AC coupled, C_{IN} = 1 μF, V_{bias} = 2.15 V	V_{ICR}	A_{GND} + 0.35		A_{VREG} – 1.35	V
Quiescent Current	P_{VDD} = 24 V, No load, No filter	I_Q		33	45	mA
Shutdown Quiescent Current	P_{VDD} = 24 V, No load, No filter, ENABLE ≤ 0.8 V	I_{QSHDN}		100	200	μA
On Resistance Drain to Source	I_O = 500 mA	$r_{DS(on)}$		360		mΩ
Gain	G0 = G1≤ 0.8 V	A_V	19	20	21	dB
	G0 ≤ 0.8 V, G1 ≥ 2 V		25	26	27	
	G0 ≥ 2 V, G1 ≤ 0.8 V		31	32	33	
	G0 = G1 ≥ 2 V		35	36	37	
Gain Matching	R_{OUTN} / R_{OUTP}, L_{OUTN} / L_{OUTP}			0.5		dB
Turn on time	ENABLE ≥ 2 V	t_{ON}		450		ms
Turn off time	ENABLE ≤ 0.8 V	t_{OFF}		150		ms

AC ELECTRICAL CHARACTERISTICS, AVDD = PVDDR = PVDDL = 12 V, R_L = 8 Ω, T_A = 25°C unless otherwise noted

Specification Name	Conditions	Symbol	Min	Typ	Max	Unit
AC Power Supply Rejection Ratio	No supply bypass, 200 mVpp ripple, f_{in} = 1 kHz, A_V = 36 dB	$PSRR_{AC}$		−69		dB
Common Mode Rejection Ratio IEC	Inputs shorted together, V_{IN} = 32 mVpp, f_{in} = 1 kHz, Av = 36 dB	$CMRR_{IEC}$		−55		dB
Output Power	A_V = 36 dB, THD+N = 1%	Pout		7.5		W
Total Harmonic Distortion + Noise	A_V = 36 dB, P_{OUT} = 1 W, f_{in} = 1 kHz	THD+N		0.05		%
Efficiency	THD+N = 0.03%, P_{OUT} = 5 W	n		85		%
Voltage noise (RTI)	Inputs AC GND thru 100 nF, A_V = 20 dB, A−weighting	V_{en}		100		μVrms
Crosstalk	Po = 1 W, f_{in} = 1 kHz, AV = 36 dB	X_{TALK}		−85		dB
Signal to Noise Ratio	V_{IN} = 100 mVpp, Av = 20 dB	SNR		90		dB
Thermal trip point	Thermal Shutdown	TSD		160		°C
Thermal hysteresis		THS		30		°C

AC ELECTRICAL CHARACTERISTICS, AVDD = PVDDR = PVDDL = 24 V, R_L = 8 Ω, T_A = 25 °C unless otherwise noted

Specification Name	Conditions	Symbol	Min	Typ	Max	Unit
AC Power Supply Rejection Ratio	No supply bypass, 200 mVpp ripple, f_{in} = 1 kHz, A_V = 36 dB	$PSRR_{AC}$		−69		dB
Common Mode Rejection Ratio (IEC)	V_{IN} = 32 mVpp, f_{in} = 1 kHz, Av = 36 dB	$CMRR_{IEC}$		−55		dB
Output Power	A_V = 36 dB, THD+N = 1%	Pout		20		W
Total Harmonic Distortion + Noise	A_V = 20 dB, P_{OUT} = 10 W (Max value from 20 Hz to 20 kHz)	THD+N		0.03		%
Efficiency	THD+N = 1%, P_{OUT} = 20 W			83		%
Voltage noise (RTI)	Inputs AC GND thru 100 nF, A_V = 32 dB, A−Weighting	V_{en}		100		μVrms
Crosstalk	Po = 1 W, f_{in} = 1 kHz, Av = 36 dB	X_{TALK}		−85		dB
Signal to Noise Ratio	V_{IN} =100 mVpp, f_{in} = 1 kHz, Av = 36 dB	SNR		90		dB
Thermal trip point	Thermal Shutdown	TSD		160		°C
Thermal hysteresis		THS		30		°C

TYPICAL CHARACTERISTICS

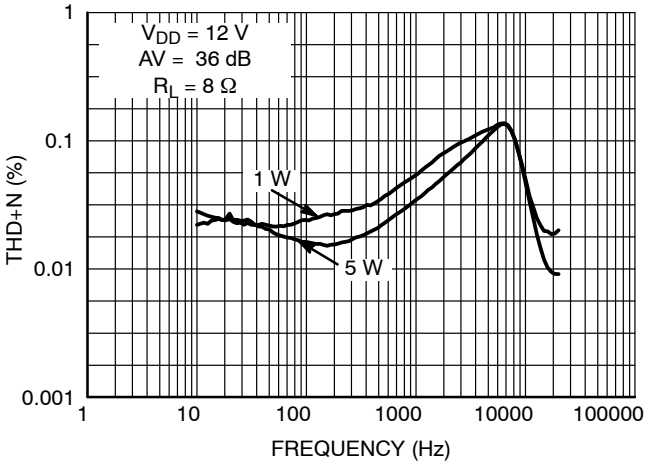


Figure 4. THD+N vs. Frequency (BTL)

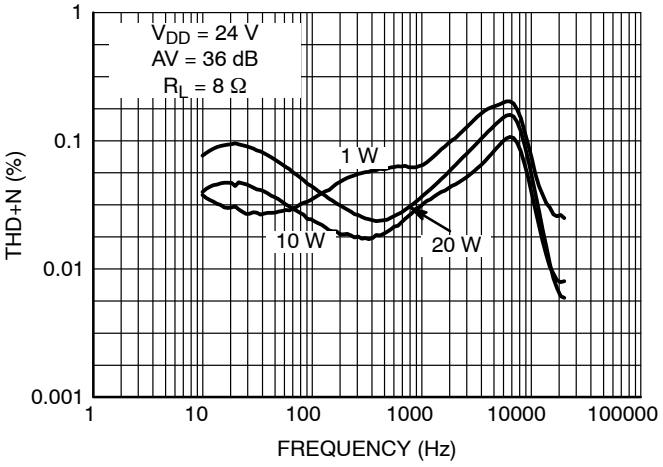


Figure 5. THD+N vs. Frequency (BTL)

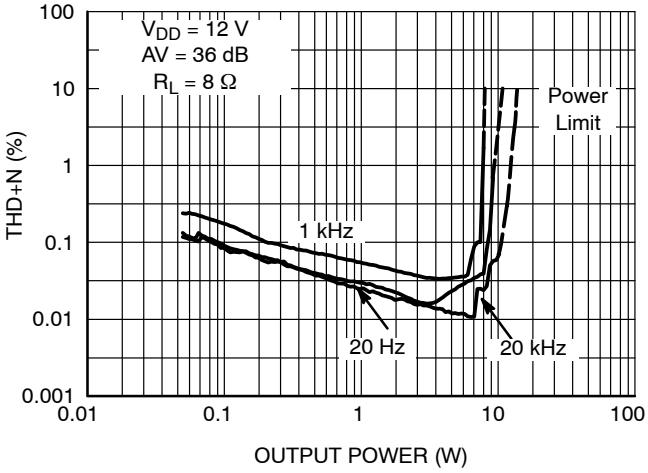


Figure 6. THD+N vs. P_{OUT}

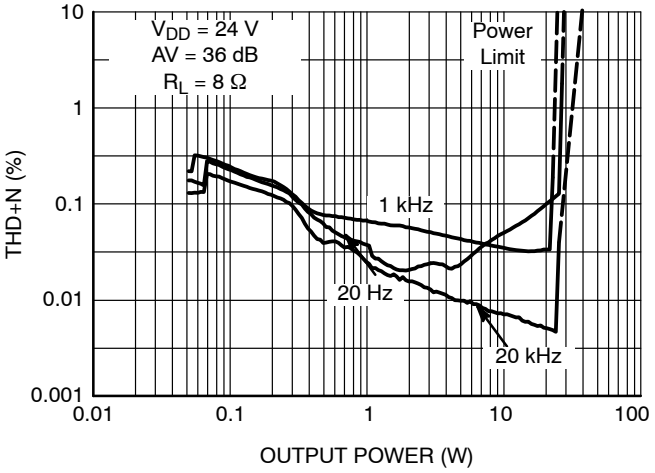


Figure 7. THD+N vs. P_{OUT}

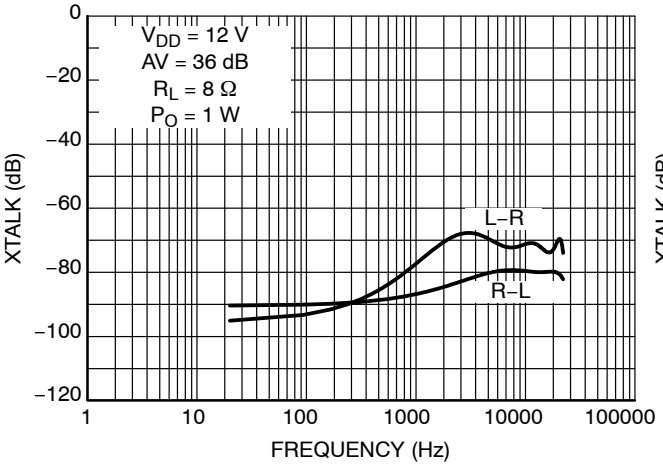


Figure 8. Crosstalk L to R and R to L (20 Hz to 20 kHz)

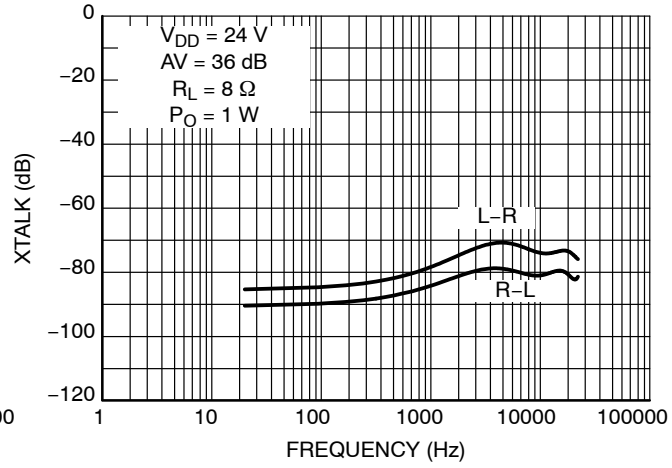


Figure 9. Crosstalk L to R and R to L (20 Hz to 20 kHz)

TYPICAL CHARACTERISTICS

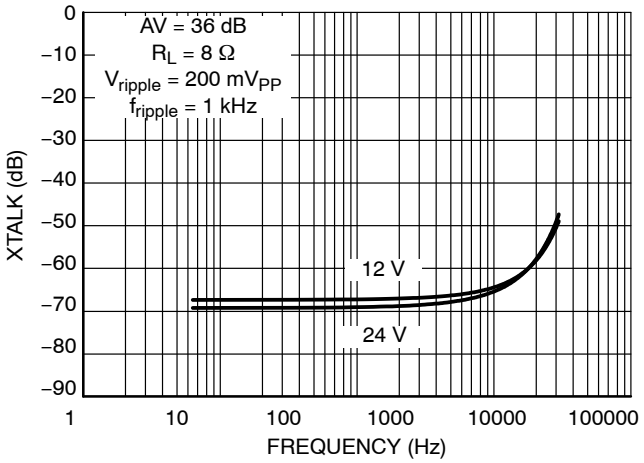


Figure 10. Crosstalk vs. Frequency

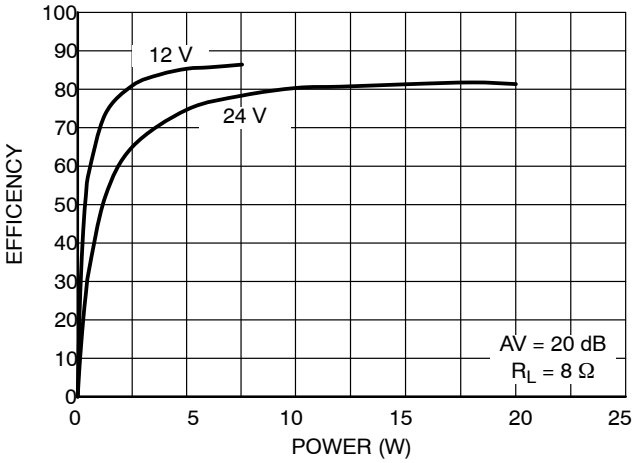


Figure 11. Efficiency vs. P_{out}

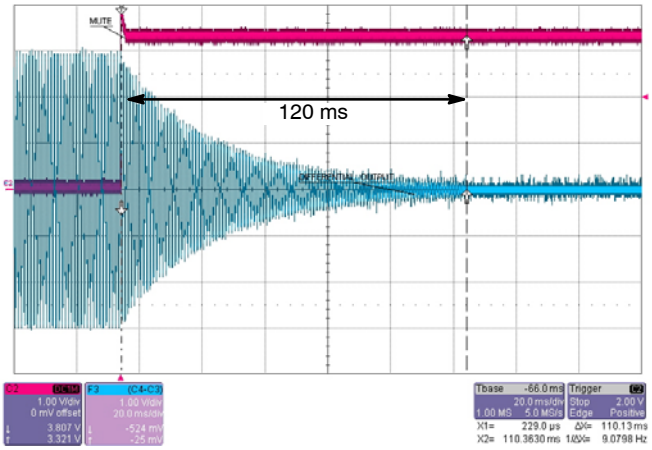


Figure 12. Turn−off Time − Mute Asserted

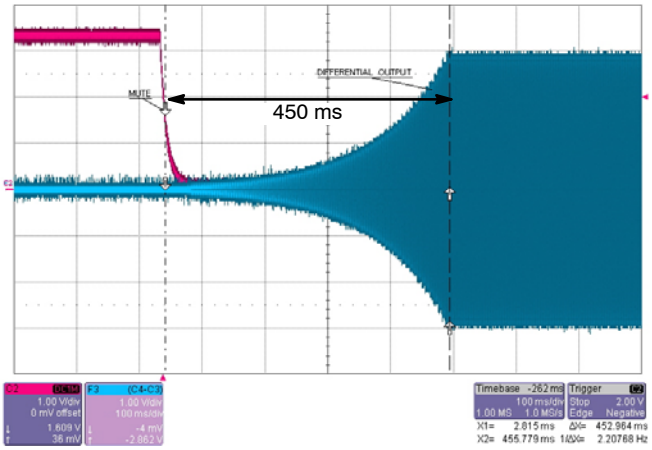


Figure 13. Turn−on Time − Mute De−asserted

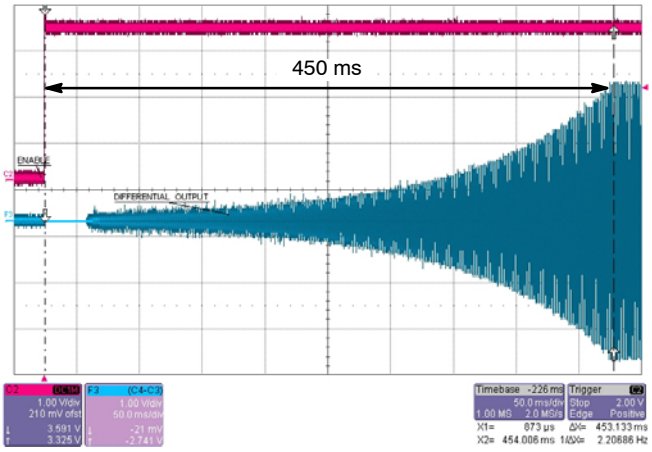


Figure 14. Turn−on Time − Enable Asserted

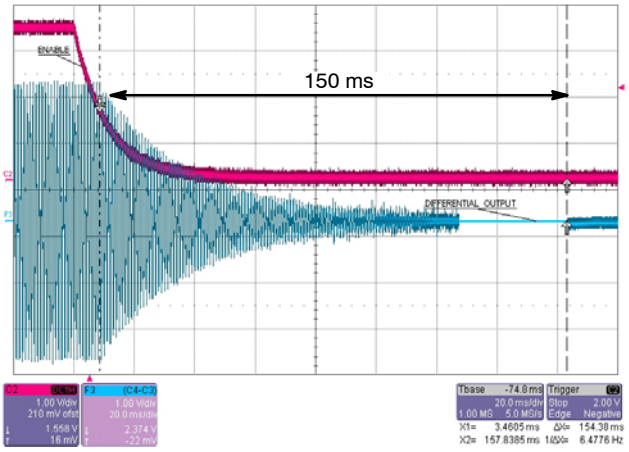


Figure 15. Turn−off Time − Enable de−asserted

APPLICATIONS INFORMATION

Digital Power Limiter

The NCS8353 utilizes a Digital Power Limiter (DPL) feature that limits the output power to 10 W, 12 W, 15 W, or 20 W per channel. This is achieved by the two external power limit pins, PL0 and PL1, which are TTL level compatible.

If a change in power limit is desired, the NCS8353 must first be disabled followed by setting a new power limit. Finally, when the NCS8353 is re−enabled, the new power limit will be active.

Table 1 illustrates the power limit per channel of the NCS8353 depending on the logic level of the power limit pins and is based on an 8 Ω speaker load.

Table 1.

PL1	PL0	Power Limit
0	0	10 W
0	1	12 W
1	0	15 W
1	1	20 W

Figure 16 shows a typical output waveform and a desired output power for an application. If the output waveform produces a higher output power than required; e.g., due to high input amplitudes, the DPL feature of the NCS8353 activates.

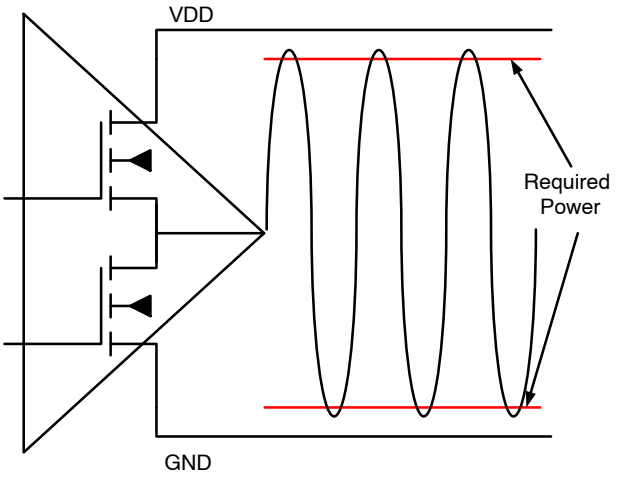


Figure 16. Before DPL Operation

The DPL reduces the internal gain of the NCS8353 thus reduces the output voltage to ensure the programmed power limit is not exceeded. Figure 17 illustrates the output voltage waveform after the DPL is activated.

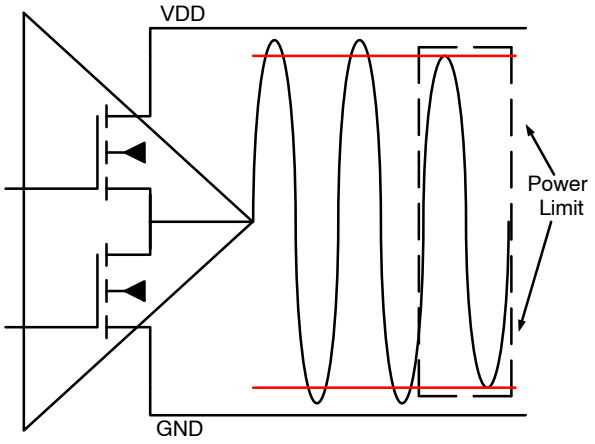


Figure 17. DPL Activated

The DPL monitors the input referred voltage level and is dependent on the programmed gain of the NCS8353. Table 2, page 12, is a quick reference for the system designer to verify when the DPL will activate assuming an 8 Ω load. If the input voltage exceeds the input reference levels illustrated in Table 2, the DPL will activate.

Figure 18 highlights the output power vs. input voltage for programmed power limits.

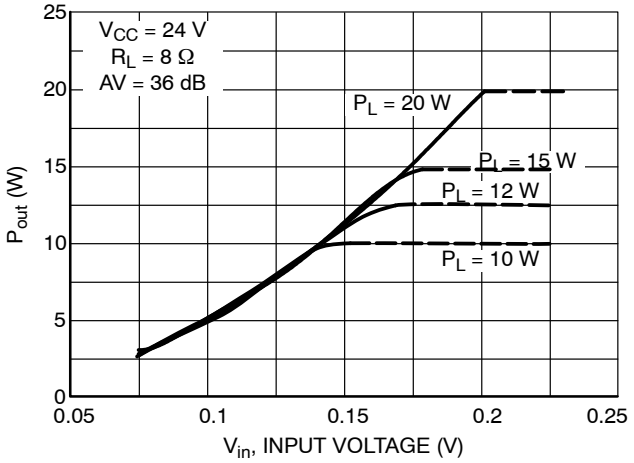


Figure 18. Power Limiter vs. V_{in}

Table 2. ALL POWER LIMITS AND VOLTAGES REFERENCED TO 8 Ω LOAD

P_{limit} / A_V	20 W	15 W	12 W	10 W
20 dB	1.789 Vin(p)	1.549 Vin(p)	1.386 Vin(p)	1.265 Vin(p)
26 dB	894 mVin(p)	775 mVin(p)	693 mVin(p)	632 mVin(p)
32 dB	447 mVin(p)	387 mVin(p)	346 mVin(p)	316 mVin(p)
36 dB	284 mVin(p)	246 mVin(p)	220 mVin(p)	201 mVin(p)

Programmable Gain Control

The NCS8353's 2-bit gain control can be programmed either by digital control or by bootstrapping the gain control pins, G0, G1, to logic HIGH or LOW and are TTL compatible inputs for soft programming needs. Reference the electrical characteristics table for minimum and maximum levels. The logic table shown in Table 3 highlights the amplifier gain settings in dB based on gain setting.

Table 3.

G1	G0	AMPLIFIER GAIN (dB) (Typ)
0	0	20
0	1	26
1	0	32
1	1	36

Similar to the DPL, if a change in gain is desired the NCS8353 must be disabled. The gain may then be programmed to the new desired level and then re-enabled for the new gain setting to latch.

Fault Detection

The NCS8353 incorporates fault detection circuitry. If a short circuit occurs the FAULT pin asserts logic HIGH providing the system designer an error flag for monitoring.

The FAULT flag also asserts HIGH when the NCS8353 enters thermal shutdown. When the NCS8353 cools to 130°C or once the short circuit condition is removed the FAULT flag returns LOW.

Short−Circuit Protection

A short can occur to V_{DD}, V_{SS}, or across the load. The short circuit protection circuitry will disable the output stage from delivering current to the load when a short is present. With the short circuit protection circuitry active the internal power dissipation will be minimized.

The NCS8353's short circuit protection is analogous to a power supply's hiccup mode current limiting operation. When a short is detected the NCS8353 will disable the output stage and will attempt to re-enable the output stage after 180 ms. If the short has been removed then the output stage re-enables and operates normally; however, if the short is still present the cycle begins again. Internal heat dissipation is kept to a minimum as current will only flow during the reset time of the protection circuitry. The hiccup mode is continuous until the short is removed.

Over Temperature Protection

The thermal protection circuitry of the NCS8353 monitors the maximum junction temperature of the die. When the temperature increases to 150°C, the specified maximum junction temperature, the internal gain of the device is reduced until the junction temperature is approximately 130°C. If the gain reduction is unable to limit the temperature rise of the junction then the thermal protection circuitry will completely disable the output stage once the junction temperature rises above 160°C. The NCS8353 will re-enable the output stage when the junction temperature falls to 130°C. This provides 30° of thermal hysteresis.

Enable

The NCS8353 incorporates a single ENABLE control for right and left audio channels. When ENABLE is asserted logic LOW, the internal circuitry completely disables each channel to reduce quiescent current draw from the power supply. Typical shutdown current for the NCS8353 will be 100 μA typical per channel and start−up time from shutdown is typically ≤450 ms. See the electrical specification table for conditions.

The ENABLE function also serves to latch new values for gain and the DPL. When new levels are desired the NCS8353 must be disabled, the new values must be programmed, and then re-enabled for the new values to latch. See Tables 1 and 3 for power limit and gain values.

Mute Function

The MUTE function will ensure any audio signal present at the input is inaudible at the speaker load. The right and left channels are not in shutdown during this time. During the MUTE state, the outputs will continue to switch at 50% duty cycle; however, a modulated audio signal will not be present. The MUTE function is activated with a logic HIGH signal and deactivated with a logic LOW signal.

Pop and Click Suppression

Pop and click is often a function of charge difference from input coupling and bypass capacitors, momentary differential offset voltages across the speaker, or state changes of the input source (codec) that cause an abrupt change in current to flow through the loudspeaker. In all

cases these pop and click phenomena occur during the following power sequences:

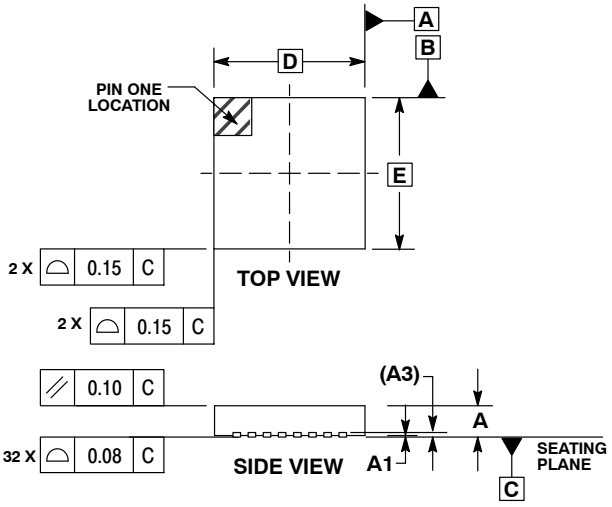
- Power supply power-up or power down (codec or amp).
- Entering or releasing from shutdown/mute (codec or amp).
- State changes in the audio codec; e.g., switching between audio sources.

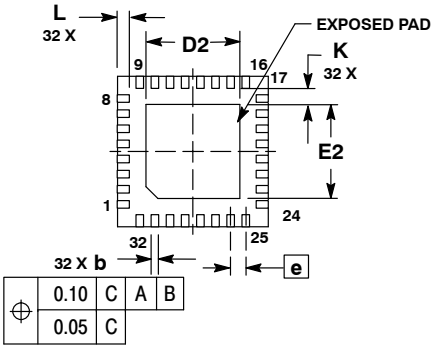
Due to the voltage changes in the audio signal chain a momentary current will flow through the loudspeaker. When current flows through the voice coil of a loudspeaker it causes the diaphragm to move thus causing a popping and clicking sound.

The NCS8353 includes pop and click suppression circuitry that creates a slow ramp to bias the amplifier during the previously mentioned power sequences. In order to eliminate “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When logic high is applied to the shutdown pin, the internal biasing voltage rises quickly and once the output DC level is around the common mode voltage, the gain is established slowly. This method to turn on the device is optimized in terms of rejection of “pop and click” noises. The device has the same behavior when it is turned-off by a logic low on the shutdown pin. No power is delivered to the load 150 ms after a falling edge on the shutdown pin. Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

PACKAGE DIMENSIONS

QFN32, 5x5x1, 0.5P
CASE 488AM−01
ISSUE O



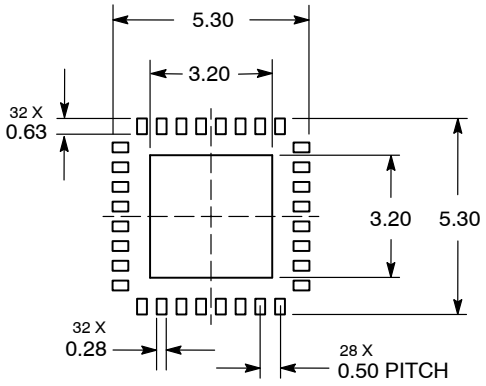


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	---	---
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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