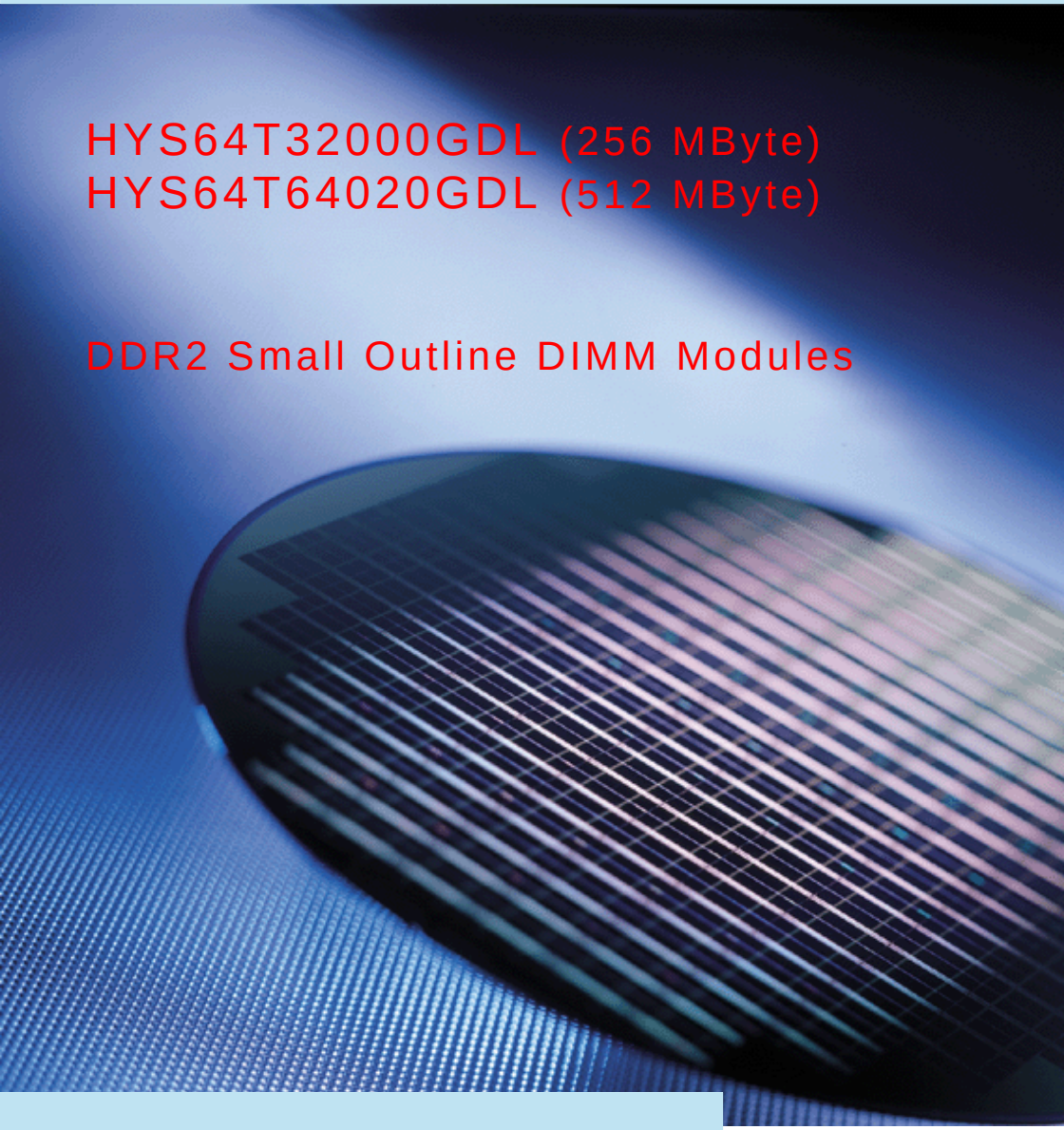
HYS64T32000GDL (256 MByte)
HYS64T64020GDL (512 MByte)

DDR2 Small Outline DIMM Modules



Memory Products

Never stop thinking.

200-pin Small Outline DDR2 SDRAM Modules (SO-DIMMs)

256 MByte & 512 MByte Modules
PC2-3200S /-4300S /-5300S

- 200-pin Non-ECC Unbuffered 8-Byte Dual-In-Line DDR2 SDRAM Module for Notebooks and other application where small form factors are required.
- One rank 32M x 64 and two ranks 64M × 64 organization
- JEDEC standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (±0.1 V) power supply
- Built with 512Mb DDR2 SDRAMs in 84-ball FBGA chipsize packages
- Programmable $\overline{\text{CAS}}$ Latencies (3, 4 & 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- OCD (Off-Chip Driver Impedance Adjustment) and ODT (On-Die Termination)
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 67.60 mm x 30.00 mm (MO-224)
- Based on JEDEC standard reference card layouts Raw Card “A” & “C”

- Performance:

Speed Grade Indicator	-5	-3.7	-3	Unit
Component Speed Grade	DDR2-400	DDR2-533	DDR2-667	
Module Speed Grade	PC2-3200	PC2-4300	PC2-5300	
Max. Clock Frequency @ CL = 3	200	200	200	MHz
Max. Clock Frequency @ CL = 4 & 5	200	266	333	MHz

1.0 Introduction

The HYS64T32000GDL and HYS64T64020GDL are low profile Small-Outline DIMM modules (SO-DIMMs) with 30,0 mm height based on DDR2 technology. DIMMs are available as one rank 32M x 64 (256MB) and two ranks 64M x 64 (512MB) organisation and density, intended for mounting into 200 pin connector sockets.

The memory array is designed with 512Mb Double Data Rate (DDR2) Synchronous DRAMs for Non-ECC applications. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

1.1 Ordering Information

Type & Partnumber	Compliance Code	Description	ECC/ Non-ECC	SDRAM Technology
PC2-3200:				
HYS64T32000GDL-5-A	PC2-3200S-33310-C	one rank 256 MB SO-DIMM	Non-ECC	512 MBit (x16)
HYS64T64020GDL-5-A	PC2-3200S-33310-A	two ranks 512 MB SO-DIMM	Non-ECC	512 MBit (x16)
PC2-4300:				
HYS64T32000GDL-3.7-A	PC2-4300S-44410-C	one rank 256 MB SO-DIMM	Non-ECC	512 MBit (x16)
HYS64T64020GDL-3.7-A	PC2-4300S-44410-A	two ranks 512 MB SO-DIMM	Non-ECC	512 MBit (x16)
PC2-5300:				
HYS64T32000GDL-3-A	PC2-5300S-44410-C	one rank 256 MB SO-DIMM	Non-ECC	512 MBit (x16)
HYS64T64020GDL-3-A	PC2-5300S-44410-A	two ranks 512 MB SO-DIMM	Non-ECC	512 MBit (x16)

Notes:

1. All part numbers end with a place code, designating the silicon die revision. Example: HYS 64T64020GDL-5-A, indicating Rev.A die are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see section 8 of this datasheet.
2. The Compliance Code is printed on the module label and describes the speed grade, f.e. “PC2-4300S-44410-C”, where 4300S means Small Outline DIMM modules with 4.26 GB/sec Module Bandwidth and “44410” means $\overline{\text{CAS}}$ latency = 4, trcd latency = 4 and trp latency = 4 using the latest JEDEC SPD Revision 1.0 and produced on the Raw Card “C”.

1.2 Address Format

Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M × 64	1	Non-ECC	4	13/2/10	8k	64 ms	7.8 µs
512 MB	2 x 32M × 64	2	Non-ECC	8	13/2/10	8k	64 ms	7.8 µs

1.3 Components on Modules

Density	DRAM components reference datasheet	DRAM Density	DRAM Organisation
256 MB	HYB18T512160AC	512 Mbit	32Mb x 16
512 MB	HYB18T512160AC	512 Mbit	32Mb x 16
For a detailed description of all functionalities of the DRAM components on these modules see the referenced component datasheet			

1.4 Pin Definition and Function

Pin Name	Description	Pin Name	Description
A[12:0]	Row Address Inputs	DQ[63:0]	Data Input/Output
A[9:0]	Column Address Inputs	DQS[7:0]	Data strobes
A10/AP	Column Address Input for Auto-Precharge	$\overline{\text{DQS}}$[7:0]	Data strobes complement
BA[1:0]	SDRAM Bank Selects	DM[7:0]	Data Masks
CK[1:0]	Clock input (positive line of differential pair)	SCL	Serial bus clock
$\overline{\text{CK}}$[1:0]	Clock input (negative line of differential pair)	SDA	Serial bus data line
$\overline{\text{RAS}}$	Row Address Strobe	SA[1:0]	slave address select
$\overline{\text{CAS}}$	Column Address Strobe	V_{DD}	Power (+ 1.8 V)
$\overline{\text{WE}}$	Read/Write Input	V_{REF}	I/O reference supply
$\overline{\text{CS}}$[1:0]	Chip Selects	V_{SS}	Ground
CKE[1:0]	Clock Enable	V_{DDSPD}	EEPROM power supply
ODT[1:0]	Active termination control lines [1)]	NC	no connect

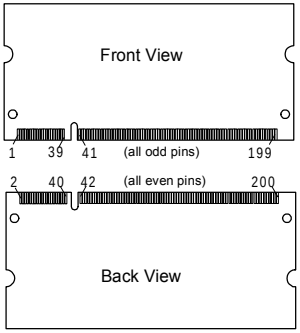
1) Active termination only applies to DQ, DQS, $\overline{\text{DQS}}$ and DM signals
2) $\overline{\text{CS1}}$, ODT1 and CKE1 are used on dual rank modules only

1.5 Pin Configuration

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREF	2	VSS	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	VSS	4	DQ4	53	VSS	54	VSS	103	VDD	104	VDD	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	VSS	156	VSS
7	DQ1	8	VSS	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	VSS	10	DM0	59	VSS	60	VSS	109	$\overline{WE}$	110	$\overline{CS0}$	159	DQ49	160	DQ53
11	$\overline{DQS0}$	12	VSS	61	DQ24	62	DQ28	111	VDD	112	VDD	161	VSS	162	VSS
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC	164	CK1
15	VSS	16	DQ7	65	VSS	66	VSS	115	$\overline{CS1}$	116	(A13)	165	VSS	166	$\overline{CK1}$
17	DQ2	18	VSS	67	DM3	68	$\overline{DQS3}$	117	VDD	118	VDD	167	$\overline{DQS6}$	168	VSS
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	VSS	22	DQ13	71	VSS	72	VSS	121	VSS	122	VSS	171	VSS	172	VSS
23	DQ8	24	VSS	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	VSS	28	VSS	77	VSS	78	VSS	127	VSS	128	VSS	177	VSS	178	VSS
29	$\overline{DQS1}$	30	CK0	79	CKE0	80	CKE1	129	$\overline{DQS4}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK0}$	81	VDD	82	VDD	131	DQS4	132	VSS	181	DQ57	182	DQ61
33	VSS	34	VSS	83	NC	84	(A15)	133	VSS	134	DQ38	183	VSS	184	VSS
35	DQ10	36	DQ14	85	(BA2)	86	(A14)	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS7}$
37	DQ11	38	DQ15	87	VDD	88	VDD	137	DQ35	138	VSS	187	VSS	188	DQS7
39	VSS	40	VSS	89	A12	90	A11	139	VSS	140	DQ44	189	DQ58	190	VSS
41	VSS	42	VSS	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	VSS	193	VSS	194	DQ63
45	DQ17	46	DQ21	95	VDD	96	VDD	145	VSS	146	$\overline{DQS5}$	195	SDA	196	VSS
47	VSS	48	VSS	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS2}$	50	NC	99	A3	100	A2	149	VSS	150	VSS	199	VDDSPD	200	SA1

Pins 84, 85, 86 and 116 are not connected on this modules and are reserved for future modules

1.6 Pin Locations



200 pin SO-DIMM (MO-224)

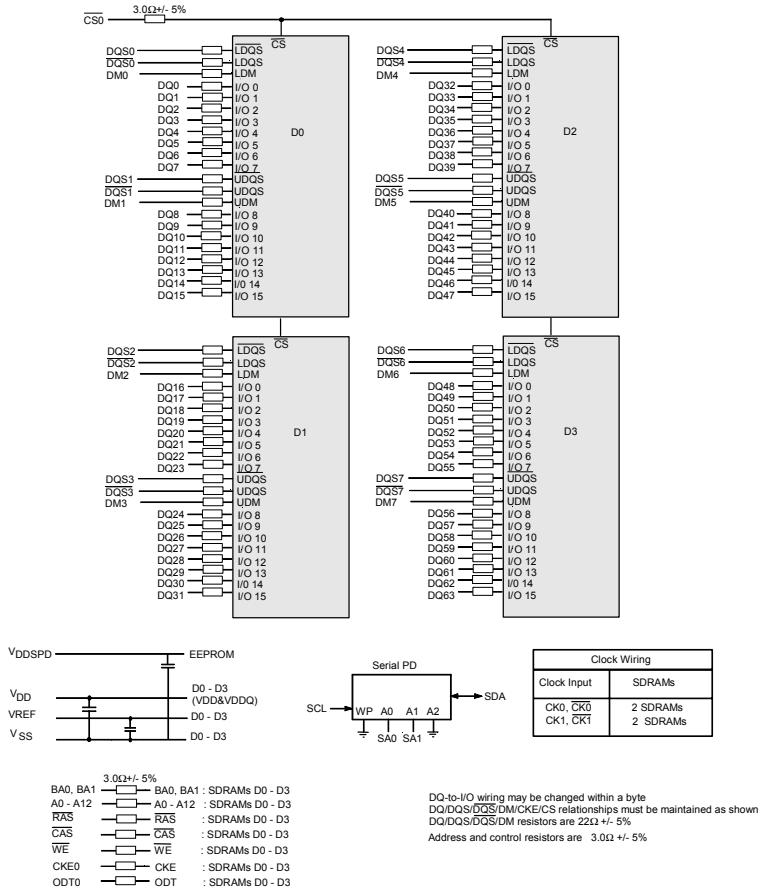
1.7 Unbuffered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK[1:0], $\overline{CK}$[1:0]	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$.
CKE[1:0]	Input	Active High	Activates the SDRAM clock signals when high and deactivates when lo. By deactivating the clocks, CKE low initiates the Power Down Mode or the Self Refresh Mode
$\overline{CS}$[1:0]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
ODT[1:0]	Input	Active High	When high, termination resistance is enabled for all DQ, DQS and DM pins, assuming this function is enabled in the Extended mode Register Set (EMRS).
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive edge of the clock, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
DM[7:0]	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is samples on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA[1:0]	Input	-	Selects which internal SDRAM memory bank is activated
A[12:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10(=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ[63:0]	I/O	-	Data Input /Output pins.
DQS[7:0], $\overline{DQS}$[7:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA[2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
VREF	Supply	-	Reference voltage for the SSTL-18 inputs.
V_{DD}SPD	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.

2.0 Block Diagrams

2.1 One Rank 32M x64 DDR2 SDRAM SO - DIMM Module (x16 components)

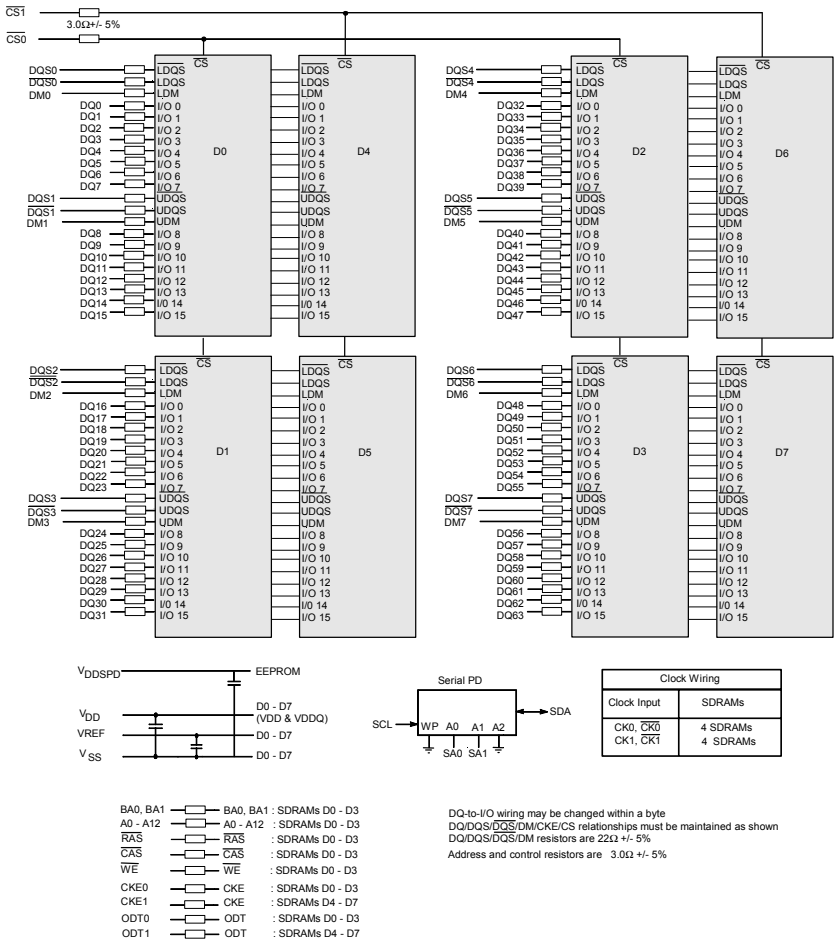
HYS64T32000GDL on Raw Card C



Block Diagram

2.2 Two Ranks 64M x 64 DDR2 SDRAM SO - DIMM Modules (x16 components)

HYS64T64020GDL on Raw Card A



3.0 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3	
Storage temperature range	T_{STG}	-55	+100	°C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.1 Operating Temperature Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DIMM Module Operating Temperature Range (ambient)	TOPR	0	+65	°C	
DRAM Component Case Temperature Range	TCASE	0	+95	°C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREFI = 3.9 µs.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

3.2 Supply Voltage Levels and DC Operating Conditions (SSTL_1.8)

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	–	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	–	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	–	V_{REF} – 0.125	V	
Input Leakage Current	I_{IL}	– 5		5	µA	3)
Output Leakage Current	I_{OL}	– 5		5	µA	3)

1 Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2 Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\,(DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
3 For any pin under test input of 0 V ≤V_{IN} ≤V_{DDQ} + 0.3 V. Values are shown per DDR2-SDRAM component

4.0 I_{DD} Specifications and Conditions

4.1 256MByte SO-DIMM Module HYS64T32000GDL (1 rank, 4 components x16)

256 MByte HYS64T32000GDL		PC2-3200 "-5"		PC2-4300 "-3.7"		PC2-5300 "-3"			
Symbol	Parameter / Condition	typ.	max.	typ.	max.	typ.	max.	Unit	Note
I_{DD0}	Operating Current	201	241	216	259	237	284	mA	1
I_{DD1}	Operating Current	239	287	260	312	286	343	mA	1
I_{DD2P}	Precharge PD Standby Current	7,1	9,9	9,4	13,1	11,8	16,5	mA	1
I_{DD2N}	Precharge Standby Current	65	78	87	104	109	131	mA	1
I_{DD2Q}	Precharge Quiet Standby Current	49	68	65	90	81	113	mA	1
$I_{DD3P(0)}$	Active PD Standby Current	26	37	35	49	43	61	mA	1
$I_{DD3P(1)}$	LP Active PD Standby Current	tbd.	tbd.	tbd.	tbd.	tbd.	tbd.	mA	1
I_{DD3N}	Active Standby Current	97	117	127	153	158	189	mA	1
I_{DD4R}	Operating Current Burst Read	253	304	312	374	372	447	mA	1
I_{DD4W}	Operating Current Burst Write	269	323	331	397	395	474	mA	1
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	385	462	404	485	419	503	mA	1
I_{DD5D}	Auto-Refresh Current (tREFI)	tbd.	tbd.	tbd.	tbd.	tbd.	tbd.	mA	1
I_{DD6}	Low-Power Self-Refresh Current	5	8	5	8	5	8	mA	1
I_{DD7}	Operating Current	569	671	616	726	679	801	mA	1

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.

4.2 512 MByte SO-DIMM Module HYS64T64020GDL (2 ranks, 8 components x16)

512 MByte HYS64T64020GDL		PC2-3200 "-5"		PC2-4300 "-3.7"		PC2-5300 "-3"			
Symbol	Parameter / Condition	typ.	max.	typ.	max.	typ.	max.	Unit	Note
I_{DD0}	Operating Current	208	251	226	273	249	301	mA	1, 2
I_{DD1}	Operating Current	246	297	269	325	298	360	mA	1, 2
I_{DD2P}	Precharge PD Standby Current	14,1	19,8	18,8	26,3	23,5	32,9	mA	1, 3
I_{DD2N}	Precharge Standby Current	131	157	174	207	218	261	mA	1, 3
I_{DD2Q}	Precharge Quiet Standby Current	97	136	129	181	162	227	mA	1, 3
$I_{DD3P(0)}$	Active PD Standby Current	52	73	69	97	87	122	mA	1, 3
$I_{DD3P(1)}$	LP Active PD Standby Current	tbd.	tbd.	tbd.	tbd.	tbd.	tbd.	mA	1,3
I_{DD3N}	Active Standby Current	195	234	254	305	315	387	mA	1, 3
I_{DD4R}	Operating Current Burst Read	261	314	321	388	384	463	mA	1, 2
I_{DD4W}	Operating Current Burst Write	276	333	341	411	407	491	mA	1, 2
I_{DD5B}	Auto-Refresh Current (tRFCmin.)	392	472	413	498	431	520	mA	1, 2
I_{DD5D}	Auto-Refresh Current (tREFI)	tbd.	tbd.	tbd.	tbd.	tbd.	tbd.	mA	1, 3
I_{DD6}	Low-Power Self-Refresh Current	10	16	10	16	10	16	mA	1, 3
I_{DD7}	Operating Current	576	681	625	740	691	818	mA	1, 2

Notes: 1) Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled.
2) The other rank is in IDD2P Precharge Power-Down Standby Current mode
3) Both ranks are in the same IDD current mode

4.3 I_{DD} Measurement Conditions

(VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

Symbol	Parameter/Condition
I_{DD0}	**Operating Current - One bank Active - Precharge** tCK = tCKmin., tRC = tRCmin., tRAS = tRASmin., CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.
I_{DD1}	**Operating Current - One bank Active - Read - Precharge** IOUT = 0 mA, BL = 4, tCK = tCKmin., tRC = tRCmin., tRAS = tRASmin.,tRCD = tRCDmin.,AL = 0, CL = CLmin.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.
I_{DD2P}	**Precharge Power-Down Current:** All banks idle; CKE is LOW; tCK = tCKmin.; Other control and address inputs are STABLE, Data bus inputs are FLOATING.
I_{DD2N}	**Precharge Standby Current**: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD2Q}	**Precharge Quiet Standby Current**: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address inputs are STABLE, Data bus inputs are FLOATING.
$I_{DD3P(0)}$	**Active Power-Down Current**: All banks open; tCK = tCKmin., CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to "0" (Fast Power-down Exit);
$I_{DD3P(1)}$	**Active Power-Down Current**: All banks open; tCK = tCKmin., CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to "1" (Slow Power-down Exit);
I_{DD3N}	**Active Standby Current**: All banks open; tCK = tCKmin.; tRAS = tRASmax; tRP = tRPmin.,CKE is HIGH; $\overline{CS}$ is high between valid commands. Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD4R}	**Operating Current - Burst Read:** All banks open; Continuous burst reads; BL = 4;AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; IOUT = 0mA.
I_{DD4W}	**Operating Current - Burst Write:** All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin.; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;
I_{DD5B}	**Burst Auto-Refresh Current**: tCK = tCKmin., Refresh command every tRFC = tRFCmin. interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD5D}	**Distributed Auto-Refresh Current**: tCK = tCKmin., Refresh command every tRFC = tREFI interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.
I_{DD6}	**Self-Refresh Current**: CKE ≤0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. IDD6 current values are guaranteed up to TCASE of 85ºC max.
I_{DD7}	**All Bank Interleave Read Current:** 1. All banks are being interleaved at minimum tRC without violating tRRD using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. Iout = 0mA. 2. Timing pattern: - ***DDR2 -400***: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D - ***DDR2 -533***: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D - ***DDR2 -667***: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D 3. Legend: A = Activate, RA = Read with Auto-Precharge, D=DESELECT

Notes:

1. IDD specifications are tested after the device is properly initialized and IDD parameter are specified with ODT disabled.
2. Definitions for IDD:
   LOW is defined as VIN <= VIL(ac)max; HIGH is defined as VIN >= VIH(ac)min.
   STABLE is defined as inputs are stable at a HIGH or LOW level.
   FLOATING is defined as inputs are VREF = VDDQ / 2.
   SWITCHING is defined as:
   inputs are changing between HIGH and LOW every other clock (once per two cycles) for address and control signals, and inputs changing between HIGH and LOW every other clock (once per cycle) for DQ signals not including mask or strobes.
3. IDD1, IDD4R, and IDD7 current measurements are defined with the outputs disabled (Iout = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
3. For two rank modules: For all active current measurements the other rank is in Precharge Power-Down Mode IDD2P

4.3 I_{DD} Measurement Conditions (cont'd)

For testing the IDD parameters, the following timing parameters are used:

Parameter		Symbol	-5 PC2-3200	-3.7 PC2-4300	-3 PC2-5300	Unit
			3-3-3	4-4-4	4-4-4	
CAS Latency		CLmin	3	4	4	tCK
Clock Cycle Time		tCKmin	5	3.75	3	ns
Active to Read or Write delay		tRCDmin	15	15	12	ns
Active to Active / Auto-Refresh command period		tRCmin	60	60	57	ns
Active bank A to Active bank B command delay	x16	tRRDmin	10	10	10	ns
Active to Precharge Command		tRASmin	45	45	45	ns
		tRASmax	70000	70000	70000	ns
Precharge Command Period		tRPmin	15	15	12	ns
Auto-Refresh to Active / Auto-Refresh command period		tRFCmin	105	105	105	ns
Average periodic Refresh interval		tREFI	7.8	7.8	7.8	µs

4.4 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "week" or "strong" termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving "0" or "1", as long a ODT is enabled during a given period of time.

ODT current per terminated pin:

		EMRS(1) State	min.	typ.	max.	Unit
Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING	IODTO	A6 = 0, A2 = 1	5	6	7.5	mA/DQ
		A6 = 1, A2 = 0	2.5	3	3.75	mA/DQ
Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	IODTT	A6 = 0, A2 = 1	10	12	15	mA/DQ
		A6 = 1, A2 = 0	5	6	7.5	mA/DQ
note: For power consumption calculations the ODT duty cycle has to be taken into account						

5.0 Electrical Characteristics & AC Timings

5.1 AC Timing Parameter by Speed Grade (Component level data, for reference only)

Symbol	Parameter		-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 -667		Unit
			Min	Max	Min	Max	Min	Max	
t_{AC}	DQ output access time from CK / $\overline{CK}$		–600	+600	-500	+500	-450	+450	ps
t_{DQSCK}	DQS output access time from CK / $\overline{CK}$		–500	+500	-450	+450	-400	+400	ps
t_{CH}	CK, $\overline{CK}$ high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	CK, $\overline{CK}$ low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
t_{HP}	Clock Half Period		min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		
t_{CK}	Clock cycle time	CL = 3	5000	8000	5000	8000	5000	8000	ps
		CL = 4 & 5	5000	8000	3750	8000	3000	8000	ps
t_{IS}	Address and control input setup time		600	-	600	-	tbd.	-	ps
t_{IH}	Address and control input hold time		600	-	600	-	tbd.	-	ps
t_{DH}	DQ and DM input hold time		400	-	350	-	tbd.	-	ps
t_{DS}	DQ and DM input setup time		400	-	350	-	tbd.	-	ps
t_{IPW}	Control and Addr. input pulse width (each input)		0.6	-	0.6	-	0.6	-	t_{CK}
t_{DIPW}	DQ and DM input pulse width (each input)		0.35	-	0.35	-	0.35	-	t_{CK}
t_{HZ}	Data-out high-impedance time from CK / $\overline{CK}$		-	tACmax	-	tACmax	-	tACmax	ps
t_{LZ}	Data-out low-impedance time from CK		tACmin	tACmax	tACmin	tACmax	tACmin	tACmax	ps
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)		-	350	-	300	-	tbd.	ps
t_{QHS}	Data hold skew factor		-	450	-	400	-	tbd.	ps
t_{QH}	Data Output hold time from DQS		t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	t_{HP}-t_{QHS}	-	
t_{DQSS}	Write command to 1st DQS latching transition		WL -0.25	WL +0.25	WL -0.25	WL +0.25	WL -0.25	WL +0.25	t_{CK}
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35	-	0.35	-	0.35	-	t_{CK}
t_{DSS}	DQS falling edge to CLK setup time (write cycle)		0.2	-	0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CLK (write cycle)		0.2	-	0.2	-	0.2	-	t_{CK}
t_{MRD}	Mode register set command cycle time		2	-	2	-	2	-	t_{CK}
t_{WPRES}	Write preamble setup time		0	-	0	-	0	-	ps
t_{WPRE}	Write preamble		0.25	-	0.25	-	0.35	-	t_{CK}
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}
t_{RAS}	Active to Precharge command		45	-	45	-	45	-	ns
t_{RC}	Active to Active/Auto-refresh command period		60	-	60	-	57	-	ns
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		105	-	105	-	105	-	ns

Symbol	Parameter		-5 DDR2 -400		-3.7 DDR2 -533		-3 DDR2 -667		Unit
			Min	Max	Min	Max	Min	Max	
t_{RCD}	Active to Read or Write delay (with and without Auto-Precharge) delay		15	-	15	-	12	-	ns
t_{RP}	Precharge command period		15	-	15	-	12	-	ns
t_{RRD}	Active bank A to Active bank B command	x16 (2k page size)	10	-	10	-	10	-	ns
t_{CCD}	$\overline{CAS}$ A to $\overline{CAS}$ B Command Period		2	-	2	-	2	-	t_{CK}
t_{WR}	Write recovery time		15	-	15	-	12	-	ns
t_{DAL}	Auto precharge write recovery + precharge time		WR+tRP	-	WR+tRP	-	WR+tRP	-	t_{CK}
t_{WTR}	Internal write to read command delay		10	-	7.5	-	7.5	-	ns
t_{RTP}	Internal read to precharge command delay		7.5	-	7.5	-	7.5	-	ns
t_{XARD}	Exit power down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	t_{CK}
t_{XARDS}	Exit active power-down mode to read command (slew exit, lower power)		6 - AL	-	6 - AL	-	6 - AL	-	t_{CK}
t_{XP}	Exit precharge power-down to any valid command (other than NOP or Deselect)		2	-	2	-	2	-	t_{CK}
t_{XSRD}	Exit Self-Refresh to read command		200	-	200	-	200	-	t_{CK}
t_{XSNR}	Exit Self-Refresh to non-read command		tRFC + 10	-	tRFC + 10	-	tRFC + 10	-	ns
t_{CKE}	CKE minimum high and low pulse width		3	-	3	-	3	-	t_{CK}
t_{OIT}	OCD drive mode output delay		0	12	0	12	0	12	ns
t_{DELAY}	Minimum time clocks remain ON after CKE asynchronously drops low		tIS+tCK +tIH	-	tIS+tCK +tIH	-	tIS+tCK +tIH	-	ns
t_{REFI}	Average Periodic Refresh Interval	0°C - 85°C	-	7.8	-	7.8	-	7.8	µs
		85°C - 95°C	-	3.9	-	3.9	-	3.9	

1. For details and notes see the relevant INFINEON component datasheet
2. Timing definition and values for tis, tih, tds and tdh may change due to actual JEDEC work. This may also effect the SPD code for these parameters

5.2 ODT AC Electrical Characteristics and Operating Conditions (all speed bins

Symbol	Parameter / Condition		min.	max.	Units
t_{AOND}	ODT turn-on delay		2	2	t_{CK}
t_{AON}	ODT turn-on	DDR2-400/533	tAC(min)	tAC(max) + 1 ns	ns
		DDR2-667	tAC(min)	tAC(max) + 0.7 ns	
t_{AONPD}	ODT turn-on (Power-Down Modes)		tAC(min) + 2ns	2 t_{CK} + tAC(max) + 1ns	ns
t_{AOFD}	ODT turn-off delay		2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off		tAC(min)	tAC(max) + 0.6ns	ns
t_{AOFPD}	ODT turn-off delay (Power-Down Modes)		tAC(min) + 2ns	2.5 t_{CK} + tAC(max) + 1ns	ns
t_{ANPD}	ODT to Power Down Mode Entry Latency		3	-	t_{CK}
t_{AXPD}	ODT Power Down Exit Latency		8	-	t_{CK}

6.0 Serial Presence Detect Codes for SO-DIMM DIMM Modules

Byte#	Description	Speed Grade	SPD Entry Value	Hex Value	
				HYS64T32000GDL	HYS64T64020GDL
0	Number of SPD Bytes	all	128	80	
1	Total Bytes in Serial PD	all	256	08	
2	Memory Type	all	DDR2-SDRAM	08	
3	Number of Row Addresses	all	13	0D	
4	Number of Column Addresses	all	10	0A	
5	Number of DIMM Banks, Package and Height	all	1 / 2	60	61
6	Module Data Width	all	x64	40	
7	Reserved	all	Undefined	00	
8	Module Interface Levels	all	SSTL_1.8	05	
9	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 5	-5	5 ns	50	
		-3.7	3.7 ns	3D	
		-3	3 ns	30	
10	SDRAM Access Time from Clock at CL = 5	-5	0.6 ns	60	
		-3.7	0.5 ns	50	
		-3	tbd	tbd	
11	DIMM Configuration Type	all	non-ECC	00	
12	Refresh Rate/Type	all	7.8 µs / SR	82	
13	SDRAM Width, Primary	all	x16	10	
14	Error Checking SDRAM Data Width	all	non-ECC	00	
15	Reserved	all	-	00	
16	Burst Length Supported	all	4 & 8	0C	
17	Number of SDRAM Banks	all	4	04	
18	Supported $\overline{CAS}$ Latencies	all	5, 4, 3	38	
19	Reserved	all	Undefined	00	
20	DIMM Type Information	all	SO-DIMM	04	
21	SDRAM Module Attributes	all	normal DIMM	00	
22	SDRAM Device Attributes: General	all	incl. weak driver	01	
23	Min. Clock Cycle Time at $\overline{CAS}$ Latency = 4	-5	5 ns	50	
		-3.7	3.7 ns	3D	
		-3	3 ns	30	
24	SDRAM Access Time from Clock for CL = 4	-5	0.6 ns	60	
		-3.7	0.5 ns	50	
		-3	tbd	tbd	
25	Minimum Clock Cycle Time at CL = 3	all	5 ns	50	
26	Access Time from Clock at CL = 3	all	0.6 ns	60	
27	Minimum Row Precharge Time (tRP)	-5 & -3.7	15 ns	3C	
		-3	12 ns	30	
28	Minimum Row Act. to Row Act. Delay (tRRD)	all	10 ns	28	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (tRCD)	-5 & -3.7	15 ns	3C	
		-3	12 ns	30	
30	Minimum $\overline{RAS}$ Pulse Width (tRAS)	all	45 ns	2D	
31	Module Density (per rank)		256 MB	40	

Byte#	Description	Speed Grade	SPD Entry Value	Hex Value	
				HYS64T32000GDL	HYS64T64020GDL
32	Address and Command Setup Time (tIS)	-5 & -3.7	0.6 ns	60	
		-3	tbd	tbd	
33	Address and Command Hold Time (tIH)	-5 & -3.7	0.6 ns	60	
		-3	tbd	tbd	
34	Data Input Setup Time (tDS)	-5	0.40 ns	40	
		-3.7	0.35 ns	35	
		-3	tbd	tbd	
35	Data Input Hold Time (tDH)	-5	0.40 ns	40	
		-3.7	0.35 ns	35	
		-3	tbd	tbd	
36	Write Recovery Time (tWR)	-5 & -3.7	15 ns	3C	
		-3	12 ns	30	
37	Internal Write to Read Command delay (tWTR)	-5	10 ns	28	
		-3.7 & -3	7.5 ns	1E	
38	Internal Read to Precharge delay (tRTP)	all	7.5 ns	1E	
39	Reserved		Undefined	00	
40	Extension of Byte 41 tRC and Byte 42 tRFC	all		00	
41	Minimum Core Cycle Time (tRC)	-5 & -3.7	60 ns	3C	
		-3	57 ns	39	
42	Min. Auto Refresh Command Cycle Time (tRFC)	all	105 ns	69	
43	Maximum Clock Cycle Time tck	all	8 ns	80	
44	Max. DQS-DQ Skew (tDQSQmax.)	-5	0.35 ns	23	
		-3.7	0.30 ns	1E	
		-3	tbd	tbd.	
45	Read Data Hold Skew Factor (tQHS)	-5	0.45 ns	2D	
		-3.7	0.40 ns	28	
		-3	tbd	tbd	
46-61	Superset Information		-	00	
62	SPD Revision		Revision 1.0	10	
63	Checksum for Bytes 0 - 62	-5		tbd	tbd
		-3.7		tbd	tbd
		-3		tbd	tbd
64-71	Manufacturers JEDEC ID Code		–	C1000000	
72	Module Assembly Location				
73-90	Module Part Number				
91-92	Module Revision Code				
93-94	Module Manufacturing Date				
95-98	Module Serial Number				
99-127	Manufacturer's Specific Data				
128-255	Open for Customer use				

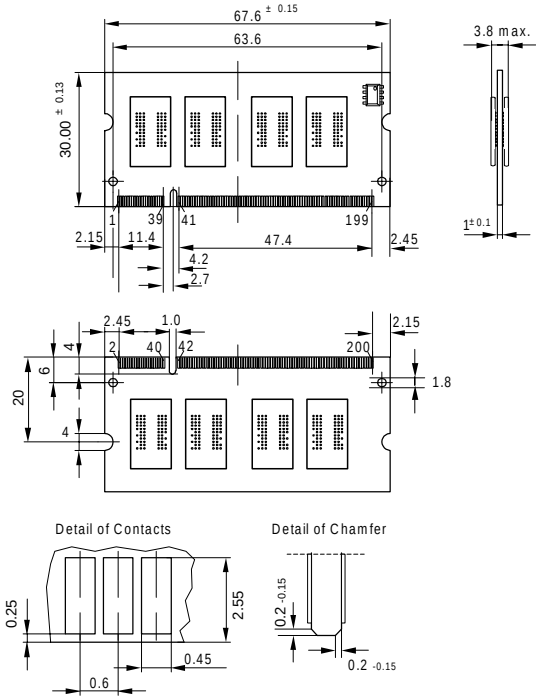
7.0 Package Outlines

7.1 Raw Card A

Module Package

DDR2 Small Outline DIMM Modules (SO-DIMM) Raw Card A

two physical ranks, 8 components x16



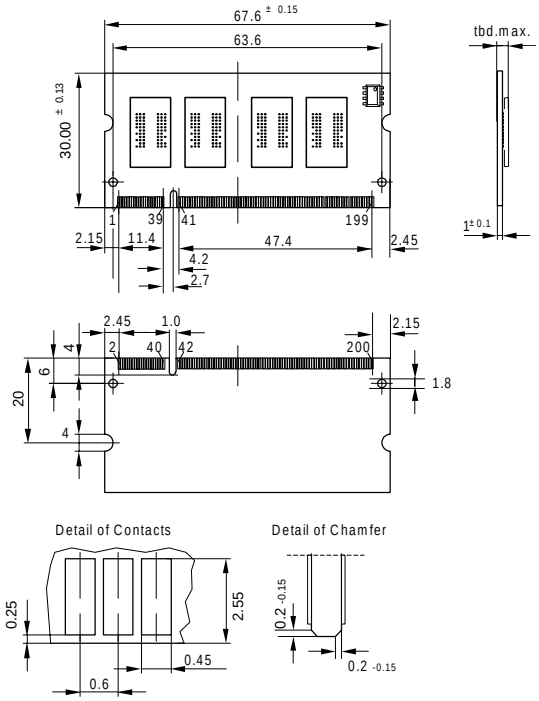
note: all outline dimensions and tolerances are in accordance with the JEDEC standard (MO-224)

7.2 Raw Card B

Module Package

DDR2 Small Outline DIMM Modules (SO-DIMMs) Raw Card C

one physical rank, 4 components x16



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

8.0 Nomenclature (Modules & Components)

8.1 DDR2 DIMM Modules

	1	2	3	4	5	6	7	8	9	10	11
Example:	HYS	64	T	64	0	2	0	G	DL	-5	-A

1	INFINEON Prefix	HYS for IFX DIMM Modules	7	Product Variations	0 = standard
2	Module Data Width	64 = Non-ECC Modules 72 = ECC Modules	8	Package	G = standard module H = “green” module
3	DRAM Technology	T = DDR2	9	Module Type	R = Registered DIMMs U = Unbuffered DIMMs DL = Small Outline DIMMs ML = MicroDIMM
4	Memory Density per I/O	64 = 64 Mb 128 = 128 Mb 256 = 256 Mb	10	Speed Grade	-5 = PC2-3200 (DDR2-400) -3.7 = PC2-4300 (DDR2-533) -3 = PC2-5300 (DDR2-667)
5	Raw Card Revision	0 = first revision	11	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
6	Number of Memory Ranks	0 = One Rank 2 = Two Ranks	Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes.		

8.2 DDR2 Memory Components

	1	2	3	4	5	6	7	8	9
Example:	HYB	18	T	512	16	0	A	C	-5

1	INFINEON Component Prefix	HYB for DRAM Components	6	Product Variations	0 = standard
2	Power Supply Voltage	18 = 1.8 V Power Supply	7	Die Revision	A = 1st Generation B = 2nd Generation C = 3rd Generation
3	DRAM Technology	T = DDR2	8	Package Type	C = BGA package F = BGA package (lead and halogen free)
4	Memory Density	256 = 256 Mb 512 = 512 Mb 1G = 1024Mb	9	Speed Grade	-5 =...DDR2-400 -3.7 =.DDR2-533 -3 =...DDR2-667
5	Memory Organisation	40 = x4, 4 data in/outputs 80 = x8, 8 data in/outputs 16 = x16, 16 data in/outputs			