



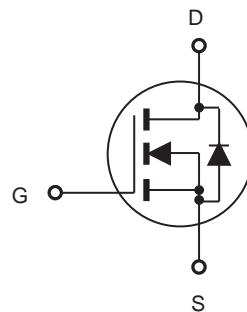
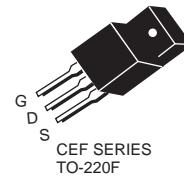
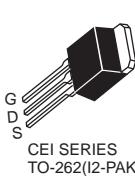
# CEP10N4/CEB10N4 CEI10N4/CEF10N4

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP10N4	450V	0.7Ω	10A	10V
CEB10N4	450V	0.7Ω	10A	10V
CEI10N4	450V	0.7Ω	10A	10V
CEF10N4	450V	0.7Ω	10A <sup>e</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handing capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.



### ABSOLUTE MAXIMUM RATINGS T<sub>C</sub> = 25°C unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	450		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous	I <sub>D</sub>	10	10 <sup>e</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>f</sup>	40	40 <sup>e</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	125 1.0	45 0.36	W W/°C
Single Pulsed Avalanche Energy <sup>d</sup>	E <sub>AS</sub>	450	450	mJ
Single Pulsed Avalanche Current <sup>d</sup>	I <sub>AS</sub>	10	10	A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.0	2.8	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	450			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 450\text{V}, V_{\text{GS}} = 0\text{V}$		25	100	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 30\text{V}, V_{\text{DS}} = 0\text{V}$		100	500	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}$		-100	-500	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	2		4	V
Static Drain-Source On-Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10\text{V}, I_D = 6\text{A}$		0.6	0.7	$\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = 50\text{V}, I_D = 6\text{A}$	3	6		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		1400		pF
Output Capacitance	$C_{\text{oss}}$			330		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			120		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{\text{d(on)}}$	$V_{\text{DD}} = 200\text{V}, I_D = 10\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 9.1\Omega$		14	75	ns
Turn-On Rise Time	$t_r$			27	125	ns
Turn-Off Delay Time	$t_{\text{d(off)}}$			50	100	ns
Turn-Off Fall Time	$t_f$			24	60	ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = 320\text{V}, I_D = 10\text{A}, V_{\text{GS}} = 10\text{V}$		48	65	nC
Gate-Source Charge	$Q_{\text{gs}}$			4		nC
Gate-Drain Charge	$Q_{\text{gd}}$			15		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$ <sup>g</sup>				10	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = 10\text{A}$			2.0	V

Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature .
- b.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$  .
- c.Guaranteed by design, not subject to production testing.
- d. $L = 9.16\text{mH}, I_{AS} = 10\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$  .
- e.Limited only by maximum temperature allowed .
- f.Pulse width limited by safe operating area .
- g.Full package  $I_{S(\text{max})} = 5.6\text{A}$  .

**CEP**

# CEP10N4/CEB10N4 CEI10N4/CEF10N4

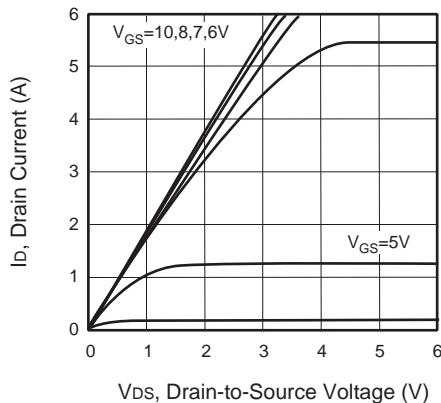


Figure 1. Output Characteristics

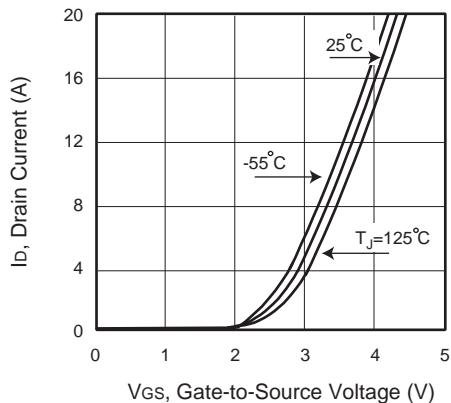


Figure 2. Transfer Characteristics

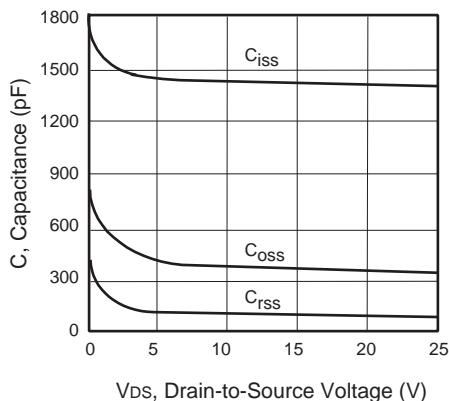


Figure 3. Capacitance

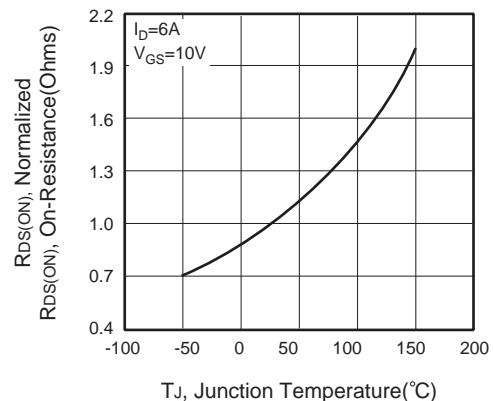


Figure 4. On-Resistance Variation with Temperature

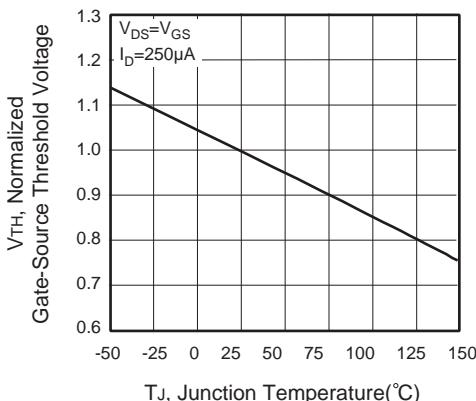


Figure 5. Gate Threshold Variation with Temperature

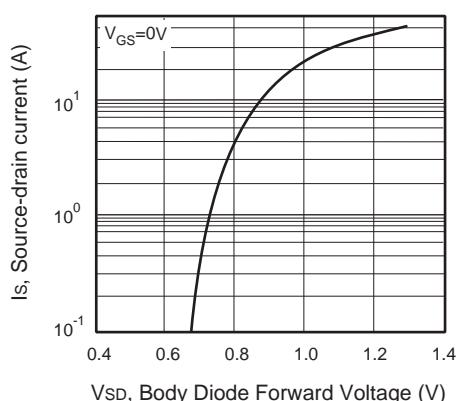


Figure 6. Body Diode Forward Voltage Variation with Source Current

CEP  
CEB  
CEI  
CEF

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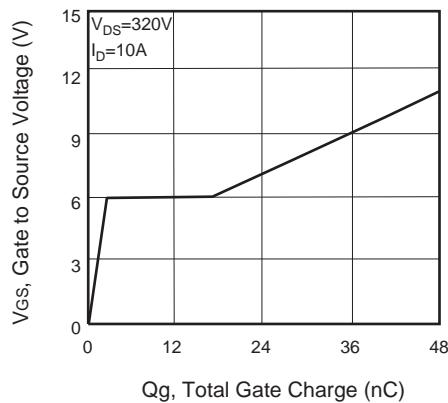


Figure 7. Gate Charge

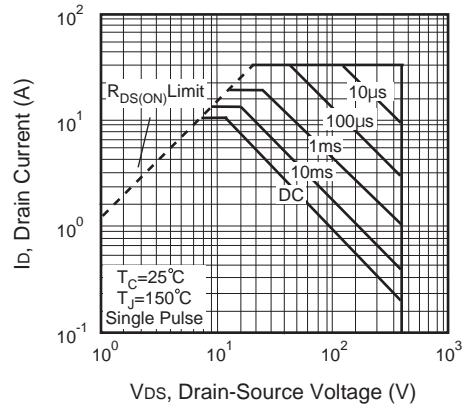


Figure 8. Maximum Safe Operating Area

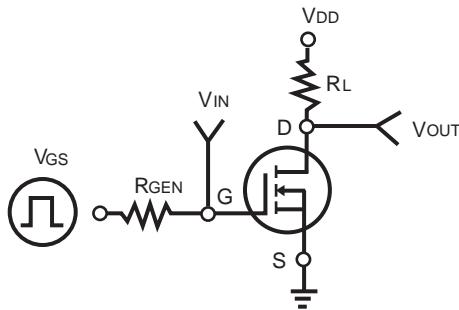


Figure 9. Switching Test Circuit

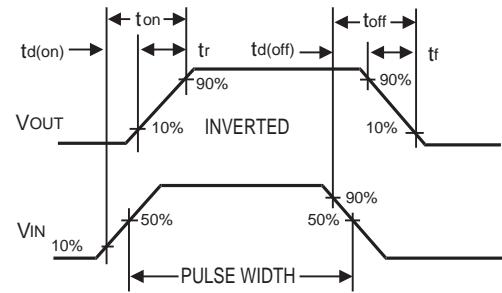


Figure 10. Switching Waveforms

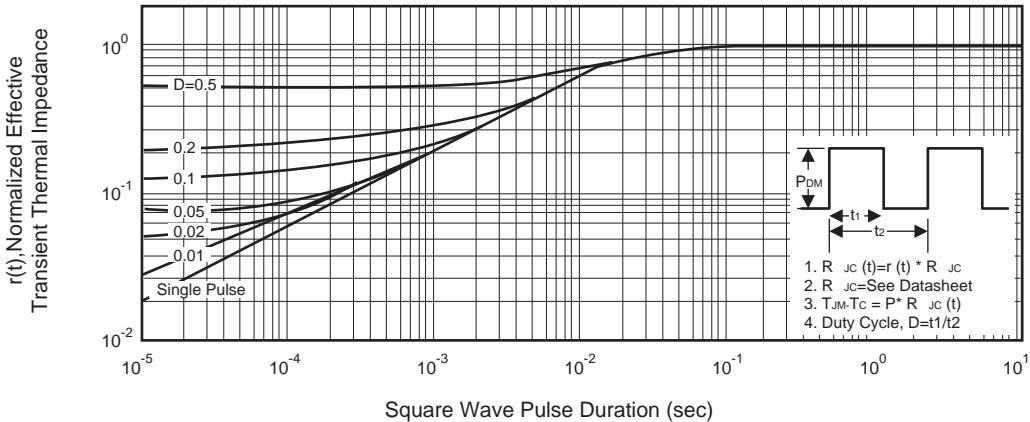


Figure 11. Normalized Thermal Transient Impedance Curve