

May 1993

DESCRIPTION

The SSI 73M650 Serial Packet Controller (SPC) is a multifunction synchronous/asynchronous communications IC that simplifies synchronous communications interface to a standard PC peripheral bus. The SPC consists of the control and FIFO registers of a 16550A UART combined with one channel of an 8530 SCC. It operates in two basic configurations.

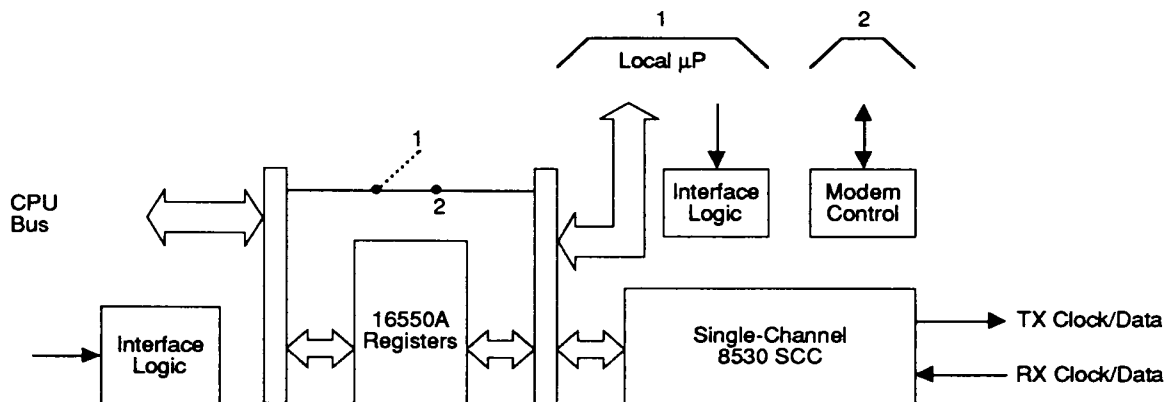
The Dual-Processor configuration has two parallel interface ports, one for connection to a CPU and the other to a local protocol controller. The local controller can then use the SCC block for synchronous or asynchronous protocols.

The Single-Processor configuration can be used in either a Mailbox or Non-mailbox mode. The Mailbox mode uses the same internal configuration as Dual-Processor, but all registers are accessible through only one hardware port. This allows the CPU to replace the function of the local controller while the SPC maintains the standard asynchronous interface. In the Non-mailbox mode, the SPC is simply a 16550A and one channel of an 8530 in the same package. The user may select either the 16550A block or the 8530 block.

FEATURES

- Register compatibility with 16550A UART
- Functional superset of a single channel 8530 SCC
- DMA signals available in 44-pin package
- NRZ, NRZI, FM and Manchester encode and decode
- 32-bit CRC for V.42 compatibility
- 3 or 16 byte Rx and Tx FIFOs for SCC reduces interrupt overhead
- External devices can be mapped into PC I/O space
- Static design with Oscillator Disable for low power standby operation
- Clock pre-divide to allow input of higher frequency processor clocks
- 16-byte UART receive FIFO always active to reduce CPU overhead
- Space-saving 28-pin version (73M1650)
- Bus timing compatible with PCMCIA Release 2

BLOCK DIAGRAM



- 1) Dual Processor Only
2) Single Processor Only

SSI 73M650/1650

Serial Packet Controller

FUNCTIONAL DESCRIPTION

The SSI 73M650 Serial Packet Controller (SPC) simplifies high speed packetized serial communications in the PS/2 or PC bus environment.

FUNCTIONAL BLOCKS

The SPC is configured as two main blocks: the 16550A Main Processor UART Register block which facilitates interface to software packages written for 16450/16550A UARTs, and a Serial Communication Controller block (SCC) which is an enhanced version of one channel of an 8530.

16550A UART Register Block

The UART Register block is hardware- and register-compatible to a 16550A UART and will run most existing software packages. Additional bits to control power down and other features are available through a special hardware mode called Single-Chip-Select (SINGLECS).

A distinct feature of the 73M650 is the accessibility of all these registers to a second processor through Channel-B in the Dual-Processor configuration. The local processor can then modify these registers and the data FIFOs to perform compression and/or error correction (such as V.42bis) at a very high speed. This is not currently possible using standard products.

The scratchpad register, acting as a Mailbox, allows communication between the CPU and a local processor or microcontroller.

SCC Block

The SCC block implements the operation of one-channel (channel A) of an 8530 SCC. Some improvements in the 73M650 over the 8530 may require modifications to be made to the software currently available for the 8530.

The SCC block performs asynchronous data transfer and packetized synchronous protocols such as Monosync, Bisync, HDLC and SDLC. Included in this block are a baud rate generator, a Digital Phase Locked Loop (DPLL) for clock recovery, and a three-byte FIFO in the SCC transmit and receive path. The SCC block has NRZ, NRZI, FM and Manchester data encoding and supports a 32-bit CRC, useful in the V.42bis error correction standard.

The SPC can operate at up to 6 Mbit/s data rate. The crystal rate may be as high as 20 MHz with an internal programmable prescaler.

REGISTER SETS

The SSI 73M650 SPC contains three register sets:

Main Processor UART Registers

This register set is virtually identical to a 16550A register set. In a special hardware mode called Single-Chip-Select (SINGLECS), additional bits are introduced into these registers.

Channel A Registers

This register set is similar to 8530 Channel A registers and controls the asynchronous and synchronous serial port.

Channel B Registers

This register set allows for access by a second processor or software package to the main processor 16550A data. An additional register contains a clock prescaler and oscillator shut down.

PRODUCT CONFIGURATIONS

The SPC is used in either single- or dual-processor environments with different applications as follows:

1. When a local processor is available for high speed packetized applications, the Dual-Processor configuration is selected by tying the SP pin to GND. In this configuration the local processor and the CPU use separate hardware pins to access the SPC. The 16550A and SCC blocks are accessed independently.
2. When no local processor is needed, the SPC is used in the Single-Processor configuration and the SP pin is connected to +5V.

For maximum functionality, the SPC can operate in a unique register access arrangement called Single-Chip-Select (SINGLECS). This is the only operating mode for the 28-pin version (73M1650), and can be selected in 40- and 44-pin versions by tying the $\overline{CS2}$ and $\overline{MCS}$ pins together.

Dual-Processor Configuration

When the SP pin is connected to GND, the SPC is put into the Dual-Processor configuration. In this configuration, the main CPU and local processor use separate address, data and control pins to access the SPC. The 16550A registers are controlled by the CPU. Some of these registers are accessible to a local processor via Channel B through separate pins. The local processor uses Channel A for serial data transfer.

Upon any change in the 16550A register contents and FIFOs status, an interrupt can be generated to notify the local processor that the CPU has accessed the SPC.

Note that in Dual-Processor configuration the Modem Control and Status signals ($\overline{RTS}$, $\overline{CTS}$, etc.) are available to the main CPU via the 16550A registers.

Single-Processor Configuration

When the SP pin is connected to +5V, the SPC operates in the Single-Processor configuration. The CPU has access to all of the registers in the SPC using one data bus (D0-D7), one read strobe ($\overline{RD}$) and one write strobe ($\overline{WR}$). The address and chip select pins may be connected in the following ways:

1. When maximum firmware compatibility to 16550A/8530 operation is desired, the main CPU accesses different registers as follows:
 - a. $\overline{CS2}$, A0-A2 to access main port 16550A registers.
 - b. $\overline{MCS}$, A/ $\overline{B}$, D/ $\overline{C}$ to access Channel A and Channel B.
2. When maximum functionality is desired, the $\overline{CS2}$ and $\overline{MCS}$ pins are tied together to take the SPC into (the Single-Chip-Select (SINGLECS) mode. In this mode, which is the only operating mode for the 28-pin version (73M1650), new bits are added to the 16550A registers to allow for the following features:
 - a. Transmit FIFO trigger level control.
 - b. DMA TXRDY and RXRDY status bits.
 - c. Programmable access to the three register sets using bits 7, 6 of 16550A IER (REGSEL1, REGSEL0 bits).
 - d. Access to an external device by setting both REGSEL1 and REGSEL0 bits. In this unique application of the 73M650, proper signals to access a multiplexed address/data bus component (ALE, $\overline{MRD}$, $\overline{MWR}$) are generated allowing access to the external device in two cycles. This application greatly simplifies the required hardware for interface of PC bus to a local device.

Mailbox Mode

When the PE bit (bit 7 of Channel B, CCR) is set, the CPU can independently access the 16550A and SCC blocks. The SPC has the same internal set-up as the Dual-Processor configuration, however the hardware access to different registers is through only one data bus. The SCC block is now accessible to the CPU.

This allows the user to develop software drivers for the CPU to access and modify the data transmitted or received by a standard software package. This feature is useful in multi-tasking environments.

An interrupt can be sent to the CPU to invoke the operation of the auxiliary software package whenever data is transferred by the main processor. The auxiliary software package can then read the data FIFOs, modify the data by compression or error correction and transmit the new data using the SCC block.

Non-mailbox Mode

When the PE bit (bit 7 of Channel B, CCR) is cleared, the main CPU can access either the 16550A or SCC block. The SPC effectively behaves as either a 16550A or a single-channel 8530 in the same package, always operating as the block (16550A or 8530) that was last accessed.

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Serial Packet Controller

FEATURES COMPARISON BETWEEN SERIAL PACKET CONTROLLER (SSI 73M650) AND SERIAL COMMUNICATIONS CONTROLLER (SCC)

SCC

CAPABILITIES

- Two independent full-duplex channels
- PCLK clock required for operation
- Synchronous/Isosynchronous data rates:
 - Up to 1/4 PCLK (i.e., 2.5 Mbit/s) maximum data rate with 10 MHz PCLK using an external phase lock loop for clock recovery
 - Up to 625 kBit/s with a 10 MHz clock rate. Up to 500 kBit/s with a 8 MHz clock rate (FM encoding using a digital phase lock loop)
 - Up to 372.5 kBit/s with a 10 MHz clock rate. Up to 250 kBit/s with a 8 MHz clock rate (NRZI encoding using a digital phase locked loop)
- Asynchronous capabilities:
 - 5, 6, 7, or 8 bits per character
 - 1, 1.5, or 2 stop bits
 - Odd, even, or no parity
 - Multiples of 1, 16, 32, 64 of clock
 - Break generation and detection
 - Parity, overrun and frame error detection
- Byte oriented synchronous capabilities:
 - Internal or external character synchronization
 - 1 or 2 synchronization capabilities
 - Automatic cyclic redundancy check generation and detection

SSI 73M650

CAPABILITIES

- One full-duplex channel
- Two emulation modes 73M550, 8530
- Single- or Dual-Processor supported
- Fully static operation, no clocks required
- Clock turn-off through register set for very low power standby operation
- Synchronous/Isynchronous data rates:
 - Up to 1 time CLK (i.e., 6 Mbit/s) maximum data rate using an external phase lock loop for clock recovery
 - Up to 1250 kBit/s with a 20 MHz clock rate. (FM encoding using a digital phase lock loop)
 - Up to 625 kBit/s with a 20 MHz clock rate. (NRZI encoding using a digital phase locked loop)
- Asynchronous capabilities:
 - 5, 6, 7, or 8 bits per character
 - 1, 1.5, or 2 stop bits
 - Odd, even, or no parity
 - Multiples of 1, 16, 32, 64 of clock
 - Break generation and detection
 - Parity, overrun and frame error detection
- Byte oriented synchronous capabilities:
 - Internal or external character synchronization
 - 1 or 2 synchronization capabilities
 - Automatic cyclic redundancy check generation and detection

SCC

- **SDLC/HDLC capabilities:**
 - Abort sequence generation and checking
 - Automatic zero insertion and deletion
 - Automatic flag insertion between messages
 - Address field recognition
 - I-field residue handing, no direct valid bit count recognition
 - Automatic 16-bit cyclic redundancy generation in idle flag mode only
 - Automatic CRC detection
 - SDLC loop mode with EOP recognition/loop entry and exit
- **Data Buffering:**
 - Receiver contains a 3 byte FIFO plus receiver shift register
 - Transmitter contains a 1 byte FIFO plus transmit shift register
- **Data Encoding:**
 - NRZ, NRZI, or FM encoding/decoding
 - Manchester decoding only

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- **SDLC/HDLC capabilities:**
 - Abort sequence generation and checking
 - Automatic zero insertion and deletion
 - Automatic flag insertion between messages
 - Address field recognition
 - I-field residue handing, indicates directly a valid bit count
 - Automatic 16 SDLC, 32 V.42bis bit cyclic redundancy generation/detection
 - SDLC loop mode with EOP recognition/loop entry and exit
- **Data Buffering:**
 - Single Processor –**
 - Receiver contains a 16 byte FIFO plus receiver shift register
 - Transmitter contains a 16 byte FIFO plus transmit shift register
 - Dual Processor –**
 - Receiver contains a 3 byte FIFO plus receiver shift register
 - Transmitter contains a 3 byte FIFO plus transmit shift register
- **Data Encoding:**
 - NRZ, NRZI, or FM encoding/decoding
 - Automatic manchester decoding and encoding for fiber optics
- **Automatic Controls:**
 - Automatic transmitter control
 - Fully automatic SDLC transmission in mark idle
 - Automatic transmitter control for common transmitter bus configuration in single processor

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Serial Packet Controller

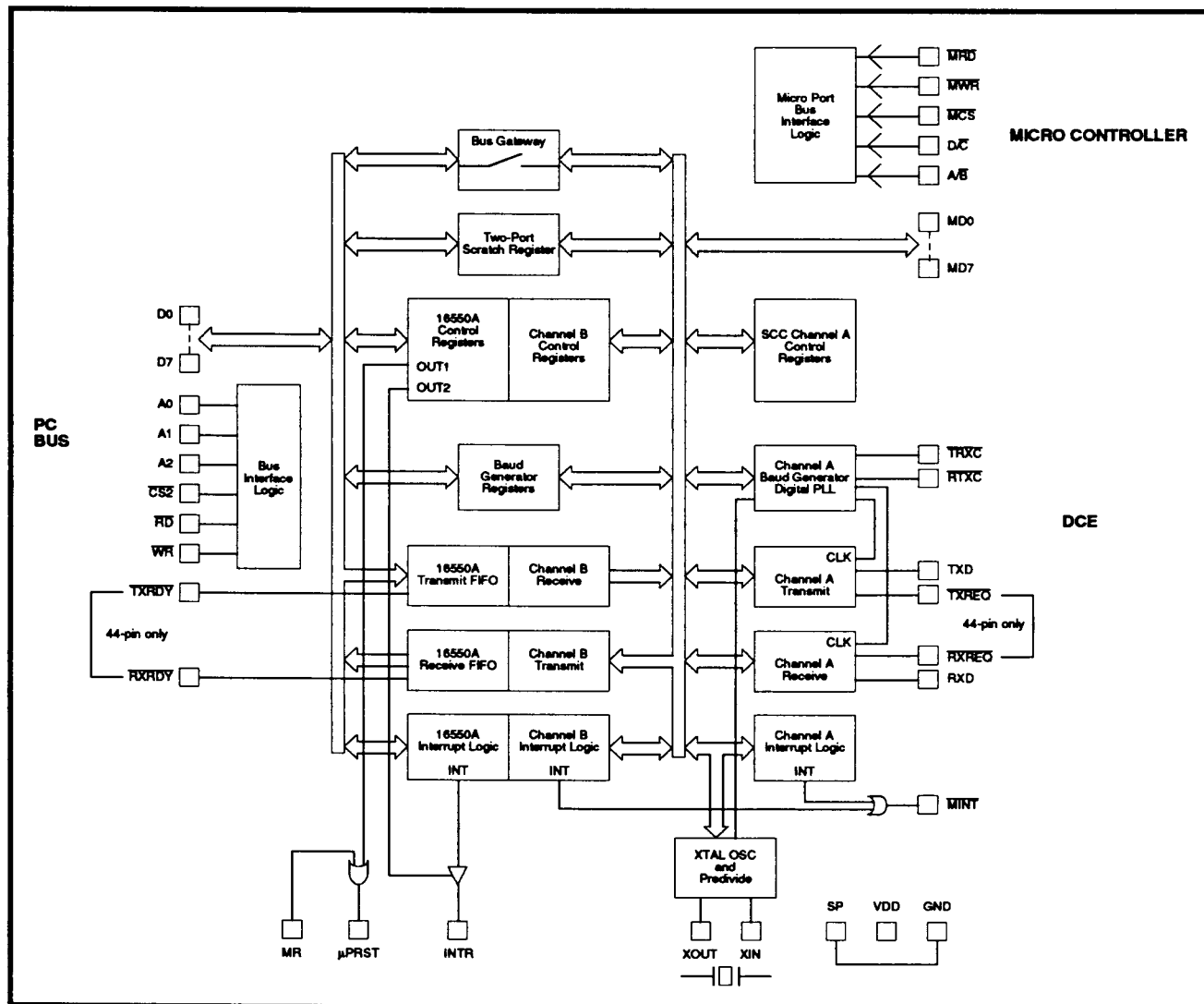


FIGURE 1: Dual-Processor Block Diagram
(Not Available on 28-Pin version)

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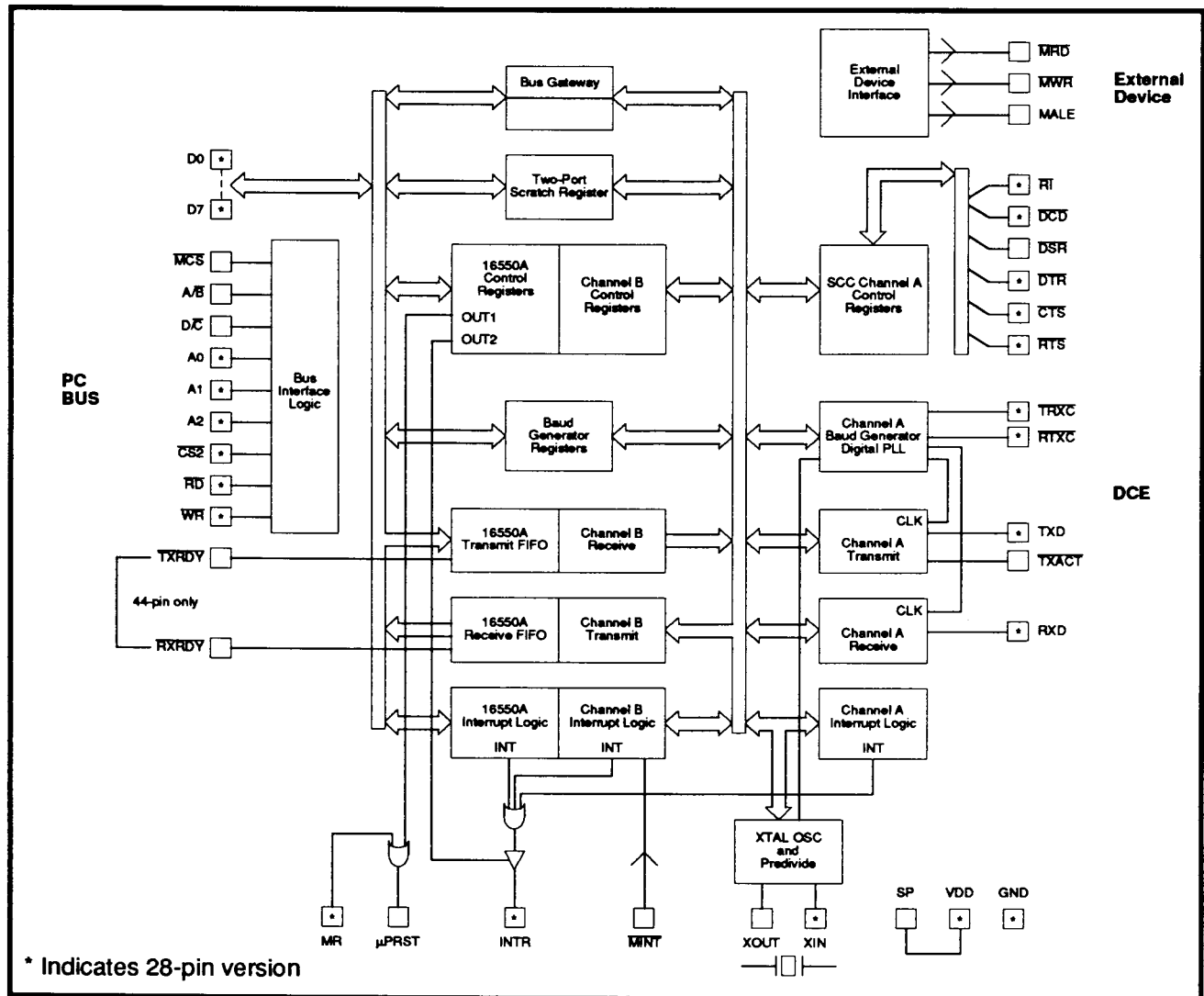


FIGURE 2: Single-Processor Mailbox Mode Block Diagram

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Serial Packet Controller

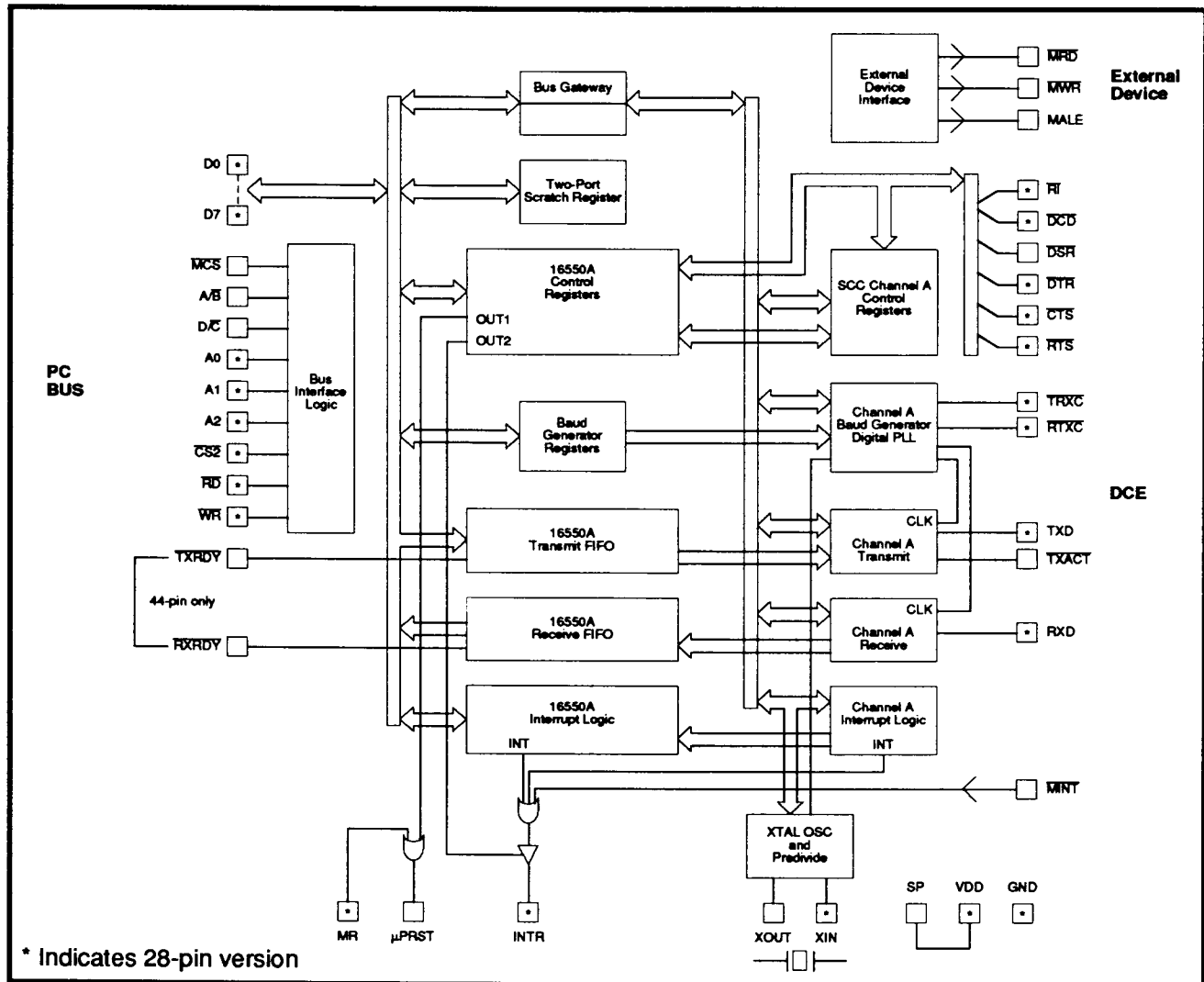


FIGURE 3: Single-Processor Non-Mailbox Mode Block Diagram

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Serial Packet Controller

PIN DESCRIPTION

Pins marked by * are available in 28-pin version (73M1650).

NAME	TYPE	DESCRIPTION
VDD *	I	+5V Supply, $\pm 10\%$. Bypass with a .1 μ F capacitor.
GND *	I	System Digital Ground.
SP	I	Single-Processor Mode Select. When high, selects Single-Processor mode. When low, selects Dual-Processor mode.
XIN *	I	Crystal/Clock Input. When a crystal is used for the time base, it is connected between this pin and XOUT. When an external clock is used, this pin requires a TTL logic level signal at maximum frequency of 20 MHz. By programming the 4-bit prescaler (bits 0, 1, 2, 3 of Channel B CCR), the external clock frequency can be adjusted to supply the required internal clock.
XOUT	I/O	Crystal output. When a crystal is used for the time base, it is connected between this pin and XIN.
MR *	I	Master Reset. When high, internal registers are initialized. This signal should be brought low for the normal operation of the SPC. A high on MR generates a high on the μ PRST pin.
μ PRST	O	Local Microprocessor Reset. This signal follows the state of MR signal and is used to reset a local microprocessor. Programming the μ PRST bit (bit 2 of 16550A MCR) to a high will also generate an active high signal on this pin.
TXD *	O	Serial Transmit Data. The serial data is updated on the rising edge of the internal transmit clock. The source of transmit clock is either an inverted version of the TRXC/RTXC pins signal or the output of Baud Rate Generator or the DPLL.
TRXC *	I/O	Synchronized Clock. The function of this pin is controlled by the TRXCO/I bit (bit 2 of Channel A WR11). If the TRXCO/I bit is set, this pin is an output clock whose rising edge can be used to sample TXD signal. When the source of the transmit clock is selected to be this pin by programming bits 4, 3 of Port-A WR11 to 01, the serial transmit data (TXD) pin is updated on the falling edge of this signal. If the TRXCO/I bit is cleared, this pin functions as an input transmit clock.
RXD *	I	Serial Receive Data. Serial data is sampled on the falling edge of the internal receive clock. The source of the receive clock is either an inverted version of the TRXC/RTXC pins signal or the output of Baud Rate Generator or the DPLL.

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Serial Packet Controller

PIN DESCRIPTION (Continued)

Pins marked by * are available in 28-pin version (73M1650).

NAME	TYPE	DESCRIPTION
$\overline{\text{RTXC}}$ *	I	Synchronized Receive Clock. When an external receive clock source is selected by clearing bits 4, 3 of Channel A WR11, the data on the RXD pin is sampled on the rising edge of this signal. The received clock may also be supplied by the $\overline{\text{TRXC}}$ pin, Baud Rate Generator or the DPLL, in which case this pin has no function. In comparison with the 8530, this pin has no accommodation for an external crystal to supply the receive clock.
$\overline{\text{TXRDY}}$	O	DMA Transmit Request. Available on the 44-pin version only; shows the status of the 16550A transmit FIFO. In the non-FIFO or 16450 mode (bit 0 FCR cleared) or when no DMA is selected (bit 3 FCR cleared), $\overline{\text{TXRDY}}$ goes active low when there is no character in the transmit FIFO and returns high when the first character is loaded into the FIFO. In the FIFO mode (bit 0 FCR set) and when DMA is selected (bit 3 FCR set), $\overline{\text{TXRDY}}$ goes active low as the transmit FIFO trigger level is reached and goes inactive high when the FIFO is completely full. If the Silicon Systems enhancement mode is not selected (bit 5 IER cleared), $\overline{\text{TXRDY}}$ goes active when the FIFO is not full. This is equivalent to a FIFO trigger level of 15.
$\overline{\text{RXRDY}}$	O	DMA Receive Ready. Available on the 44-pin version only; shows the status of the 16550A receive FIFO. In the non-FIFO or 16450 mode (bit 0 FCR cleared) or when no DMA is selected (bit 3 FCR cleared), this signal goes active low when there is at least one character in the receive FIFO. It returns inactive high when there are no more characters in the receive FIFO. In the FIFO mode (bit 0 FCR set) and DMA operation (bit 3 FCR set), this signal goes active low as the receive FIFO trigger level is reached or timeout is occurred. $\overline{\text{RXRDY}}$ returns to the inactive high level when there are no characters in the receive FIFO.
$\overline{\text{TXREQ}}$	O	DMA Transmit Request. Available on the 44-pin version only; shows the status of the 8530 three-byte transmit FIFO. TXREQ goes active low when the transmit FIFO is empty. It goes high when the FIFO is not empty.
$\overline{\text{RXREQ}}$	O	DMA Receive Request. Available on the 44-pin version only; shows the status of the 8530 three-byte receive FIFO. RXREQ goes active low when data is available in the receive FIFO. It goes inactive high when the receive FIFO is completely empty.

Main processor 16550A port:

Function and timing of these pins are similar to 16550A.

NAME	TYPE	DESCRIPTION
D0-D7 *	I/O	Data Bus. This bus provides bi-directional communication between the SPC and the main CPU. In Dual-Processor mode, the 16550A registers are accessed by this bus. In the Single-Processor mode; 16550A registers, Channel A and Channel B registers are accessed by this bus.

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PIN DESCRIPTION (Continued)

Main processor 16550A port: (Continued)

Function and timing of these pins are similar to 16550A.

Pins marked by * are available in 28-pin version (73M1650).

NAME	TYPE	DESCRIPTION
A0-A2 *	I	Register Select Address. These signals determine the address of the 16550A register to be accessed. Eight registers are selected when DLAB bit (bit 7 of 16550A LCR) is low or upon reset. Two additional registers are accessed when DLAB is set high.
$\overline{CS2}$ *	I	Chip Select, Main port. When low while $\overline{RD}$ or $\overline{WR}$ are low, allows reading or writing of the registers. In the Dual-Processor mode only the 16550A registers are accessed using this pin. In the Single-Processor mode, 16550A port as well as Channel A and Channel B registers are accessed using this pin.
$\overline{RD}$ *	I	Read Strobe. When low while $\overline{CS2}$ is low, the contents of the register addressed by A0-A2 or $A/\overline{B}$, $D/\overline{C}$ may be read to the D0-D7 data bus.
$\overline{WR}$ *	I	Write Strobe. When low while $\overline{CS2}$ is low, the contents of the D0-D7 data bus are written to the register selected by A0-A2 or $A/\overline{B}$, $D/\overline{C}$ on the rising edge of this signal. No change is made to the register which is marked to be READ-ONLY.
INTR *	I	Interrupt, High-impedance. This pin goes high whenever attention is requested from the main CPU. Clearing the E1 bit (bit 3 of 16550A MCR), places this pin in a high impedance state, allowing multiple ICs to share one CPU interrupt signal.

Channel A and Channel B In Dual-Processor Configuration:

Pins marked by # have a different function in the Single-Processor configuration.

NAME	TYPE	DESCRIPTION
MD0-7 #	I/O	Data Bus, Local Processor: Allows access to Channel A and Channel B. This bus is controlled by the local processor.
$A/\overline{B}$	I	Port Select Address: Controlled by the local processor. When high selects Channel A (USART) to transmit and receive data serially. When low allows access of the local processor to the main port (16550A) registers through Channel B.
$D/\overline{C}$	I	Command or Data Select Address: When low, a command register within Channel A or Channel B is selected. Command registers are selected in two cycles: the register address is first written into the lower four bits of command register, and the desired data is subsequently written to the selected command register. When high, the serial transmit/receive data is transferred in one cycle.
$\overline{MCS}$ #	I	Chip Select, Local Processor: In combination with the MRD and MWR; allows access to Channel A and Channel B registers.

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PIN DESCRIPTION (Continued)

Channel A and Channel B in Dual-Processor Configuration: (Continued)

Pins marked by * are available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Single-Processor** configuration.

NAME	TYPE	DESCRIPTION
$\overline{\text{MRD}}$ #	I	Read Strobe, Local Processor. When low while $\overline{\text{MCS}}$ is low, the contents of the selected register in Channel A or Channel B is transferred to the data bus. The serial data register ($\text{D}/\overline{\text{C}}$ high) can be read in one cycle. When reading the command register ($\text{D}/\overline{\text{C}}$ low), the command register address is determined by bits 0, 1, 2, 3 of WR0 . To read a new command register a write cycle to WR0 to change the register address should be done prior to the read cycle.
$\overline{\text{MWR}}$ #	I	Write Strobe, Local Processor. When low while $\overline{\text{MCS}}$ is low, contents of the data bus is written into the selected register in Channel A or Channel B if the register is not marked READ-ONLY. Writing into the serial data register ($\text{D}/\overline{\text{C}}$ high) can be done in one cycle. When writing the command register ($\text{D}/\overline{\text{C}}$ low), The command register address is determined by bits 0, 1, 2, 3 of WR0 . To write to a new command register, a write cycle to change the register address should be done prior to the write cycle.
$\overline{\text{MINT}}$ #	O	Interrupt, Local Processor, Weak Pullup. When low, notify the local processor an unmasked interrupt event occurred, caused by either an access to the 73M550 register set by the main CPU or by an unmasked interrupt occurring in the SCC. A 10K pullup resistor should be utilized between this pin and the VCC pin to provide a fast rise time at the end of interrupt. This high impedance state allows multiple ICs to share one CPU interrupt signal.

Channel A and Channel B in Single-Processor Configuration:

Pins marked by * are available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Dual-Processor** configuration.

NAME	TYPE	DESCRIPTION
$\text{A}/\overline{\text{B}}$	I	Channel Select Address. When high, selects Channel A (USART) to transmit and receive data serially. When low, allows access to the Main Processor (16550A) registers through Channel B. This signal is only used when the $\overline{\text{MCS}}$ is low.
$\text{D}/\overline{\text{C}}$	I	Command or Data Address Select. When low, a command register within Channel A or Channel B is selected. Individual registers are selected in two cycles: The address of the register is first written into the lower four bits of the command register then desired data is subsequently read from or written into the command register. When high, the serial transmit/receive data is transferred in one cycle. This signal is only used when the $\overline{\text{MCS}}$ is low.

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PIN DESCRIPTION (Continued)

Channel A and Channel B In Single-Processor Configuration: (Continued)

Pins marked by * are available in 28-pin version (73M1650).

Pins marked by # have a different function in the Dual-Processor configuration.

NAME	TYPE	DESCRIPTION
$\overline{MCS}$ #	I	Chip select, Channel A and Channel B. Access to the SPC registers is controlled by this signal and $\overline{CS2}$. When these signals are not tied together and individually controlled, the last block selected (16550A or Channel A/ B) controls the operation of the serial port. When this signal is tied to $\overline{CS2}$, The SPC is put into the Single-Chip-Select (SINGLECS) mode and access to the registers is controlled by two bits in the 16550A IER register (REGSEL1, REGSEL0). Setting REGSEL1 bit enables access to an external device in two cycles. In the SINGLECS mode, new bits are introduced in the Main Processor 16550A registers, allowing additional features.
MALE #	O	External Device ALE. When in the Single-Chip-Select (SINGLECS) mode and RSEL1 bit is set, this signal is used by the external device to latch the address of its registers. MALE is an inverted version of the WRB signal in the first cycle of an external device access. Data is transferred to the external device in the subsequent cycle using the $\overline{MWR}$ or $\overline{MRD}$ signal. When not in the SINGLECS mode, this pin remains high.
$\overline{MWR}$ #	O	External Device Write Strobe. When in the Single-Chip-Select (SINGLECS) mode and RSEL1 bit is set, this signal follows the $\overline{WR}$ signal issued by the main processor in the second cycle of an external device access. Data present on the main processor data bus (D0-D7) can be written into the external device. When not in SINGLECS mode, this pin remains high.
$\overline{MRD}$ #	O	External Device Read Strobe. When in the Single-Chip-Select (SINGLECS) mode and RSEL1 bit is set, this signal follows the $\overline{RD}$ signal issued by the main processor in the second cycle of an external device access. Data can be read from the external device to the main processor data bus (D0-D7). When not in the SINGLECS mode, this pin remains high.
MINT #	I	External Device Interrupt. When in the Single-Chip-Select (SINGLECS) mode, a low level on this pin generates an interrupt to the main processor on the INTR pin if enabled by the software. When not in the SINGLECS mode, this pin is ignored.
RTS *#	O	Request To Send. This signal shows that a DCE (modem) is ready to send the data. It is controlled by the RTS bit (bit 1 of 16550A MCR or bit 1, Port-A WR8). Setting the RTS bit results in a low level on this pin. Clearing the RTS bit would result in this pin going high immediately when the Auto Enable feature is not active. When the Auto Enable feature is active (bit 5, WR3 set), this pin goes high only after RTS bit is cleared and transmitter register is empty.

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Serial Packet Controller

PIN DESCRIPTION (Continued)

Channel A and Channel B in Single-Processor Configuration: (Continued)

Pins marked by * are available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Dual-Processor** configuration.

NAME	TYPE	DESCRIPTION
$\overline{\text{CTS}}$ *#	I	Clear To Send. This signal is used in DCE (modem) handshaking to show that the DCE has established the communication and data may be transferred to DCE. This input is Schmitt triggered and inverted and its status is reflected in the CTS bit (bit 4 of 16550A MSR and bit 5, Channel A RR0). If the Auto Enable feature is active (bit 5, WR3 set), data is automatically transmitted when this pin is low. If the Auto Enable is not selected this pin can be used as a general purpose input. The DCTS bit (bit 0 of 16550A MSR) is set when a change in the $\overline{\text{CTS}}$ logic level is detected, and it can generate an interrupt.
$\overline{\text{DTR}}$ *#	O	Data Terminal Ready. This signal is used in DCE (modem) handshaking to signify that the SPC is ready to communicate. This pin is a complement of DTR bit (bit 0 of 16550A MCR and bit 7, Channel A WR5). This pin can be used as a general purpose output pin.
$\overline{\text{DSR}}$ #	I	Data Set Ready. This signal is used in the DCE (modem) handshaking to indicate that the DCE is ready to communicate. This input is Schmitt triggered and inverted and its status is reflected in the DSR bit (bit 5 of 16550A MSR or bit 5, of Channel A RR10). This pin can be used as a general purpose input pin. Bit DDSR (bit 1 of 16550A MSR) is set when a change in $\overline{\text{DSR}}$ logic level is detected, and it can generate an interrupt.
$\overline{\text{DCD}}$	I	Data Carrier Detect. A DCE (modem) status input indicates that the DCE has detected the carrier signal on the medium (telephone line). This input is Schmitt triggered and inverted and its status is reflected in the DCD bit (bit 7 of 16550A MSR and bit 3, Channel A RR0). If the Auto Enable feature is active (bit 5, Channel A WR3 set), a low level on $\overline{\text{DCD}}$ automatically activates the receiver circuitry. When the Auto Enable is not selected this pin can be used as a general purpose input pin. Bit DDCD (bit 3 of 16550A MSR) is set when a change in $\overline{\text{DCD}}$ level is detected, and it can generate an interrupt.
$\overline{\text{RI}}$ *#	I	Ring Indicator. A DCE (modem) status input indicating the presence of ringing voltage on the telephone line. This input is Schmitt triggered and inverted and its status is reflected in the RI bit (bit 6 of 16550A MSR and bit 0, Channel A RR10). This input can be used as a general purpose input pin. The TERI bit (bit 2 of 16550A MSR) is set when a high-to-low transition is detected on this pin, and it can generate an interrupt to the main processor.
$\overline{\text{TXACT}}$ #	O	Transmitter Active. When low, this pin indicates the transmitter is currently transmitting active data. This pin is asserted just before the transmitter becomes active and is negated when the transmitter becomes active and is negated when the transmitter idles. This pin may be utilized to externally gate the transmit pin onto a transmit buss shared by multiple ICs.

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Serial Packet Controller

		DATA BIT NUMBER								
REGISTER		ADDRESS A2-A0	D7	D6	D5	D4	D3	D2	D1	D0
Receiver Buffer Register (Read only)	RBR	0 DLAB = 0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Transmit Holding Register (Write only)	THR	0 DLAB = 0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Interrupt Enable Register	IER	1 DLAB = 0	REGSEL1 (SINGLECS)	REGSEL0 (SINGLECS)	SSI Enable (SINGLECS)	0	Enable Modem Status	Enable Receiver Status	Enable THRE	Enable RDA
Interrupt ID Register (Read only)	IIR	2	FIFOs Enabled	FIFOs Enabled	RxRDY (SSI Enable)	TxRDY (SSI Enable)	Interrupt ID 2	Interrupt ID 1	Interrupt ID 0	Interrupt Pending
FIFO Control Register (Write only)	FCR	2	RCVR Trigger 1	RCVR Trigger 0	XMIT Trigger 1 (SSI Enable)	XMIT Trigger 0 (SSI Enable)	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
Line Control Register	LCR	3	Divisor Latch Access (DLAB)	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop	Word Length Select 1	Word Length Select 0
Modem Control Register	MCR	4 REGSEL=0	0	0	0	Loop	Enable Interrupt	μPRST	RTS	DTR
Line Status Register	LSR	5 REGSEL=0	Error in Receive FIFO	Transmit Empty	Transmit Holding Empty	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	Data Ready (DR)
Modem Status Register	MSR	6 REGSEL=0	DCD	RI	DSR	CTS	Delta DCD (DDCD)	Trailing Edge RI (TERI)	Delta DSR (DOSR)	Delta CTS (DCTS)
Scratch Register	SCR	7 REGSEL=0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (LS)	DLL	0 DLAB = 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS)	DLM	1 DLAB = 1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

TABLE 1: Main Port 16550A UART Registers

SSI 73M650/1650

Serial Packet Controller

			DATA BIT NUMBER							
REGISTER		ADDRESS UCR (3:0)	D7	D6	D5	D4	D3	D2	D1	D0
UART Command Register (Write only)	UCR	D/C=0 A/B=0 ONECS =1: D/C=0 A3=1 RGSEL0=1	0	0	0	0	Register Select 3	Register Select 2	Register Select 1	Register Select 0
Receiver Buffer Register (Read only)	RBR	8 — or — D/C=1 A/B=0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Transmit Holding Register (Write only)	THR	8 — or — D/C=1 A/B=0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Interrupt Enable Register	IER	1	0	0	0	Enable External INT (SP=1)	Enable MCR/SCR Status	Enable Divisor LCR Status	Enable THRE	Enable RDABOE
Interrupt ID Register (Read only)	IR	2	0	0	0	0	0	Interrupt ID 2	Interrupt ID 1	Interrupt ID 0
Line Control Register (Read only)	LCR	3	0	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop	Word Length Select 1	Word Length Select 0
Modem Control Register (Read only)	MCR	4	Delta MCR	0	0	Loop	0	0	RTS	DTR
Line Status Register	LSR	5	0	0	Transmit Holding Ready (Read only)	Channel B Tx Transmit Break	Channel B Tx Framing Error	Channel B Tx Parity Error	Channel B Rx Overrun Error (Read only)	Channel B Rx Data Ready (Read only)
Modem Status Register (Read/Write)	MSR	6	DCD	RI	DSR	CTS	0	0	0	0
Scratch Register	SCR	7	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (LS) (Read only)	DLL	9	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS) (Read only)	DLM	10	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Configure Control Register	CCR	11	16550 A Parallel Enable (SP=1)	0	0	OSC OFF	Divisor Prescale 3	Divisor Prescale 2	Divisor Prescale 1	Divisor Prescale 0

TABLE 2: Channel B Registers

SSI 73M650/1650 Serial Packet Controller

		DATA BIT NUMBER								
REGISTER		ADDRESS WR0 (3:0)	D7	D6	D5	D4	D3	D2	D1	D0
Command Register	WR0	0	CRC Reset 1	CRC Reset 1	Command Code 2	Command Code 1	Command Code 0	Register Select 2	Register Select 1	Register Select 0
Tx/Rx Interrupt Data Transfer	WR1	1 (WR only)	0	0	0	Receive Interrupt Mode 1	Receive Interrupt Mode 0	Parity Special	Tx Int Enable	External Interrupt Enable
Interrupt Vector Register	WR2	2 (RD/WR)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Receive Control	WR3	3 (WR only)	Rx Bits /Char 1	Rx Bits /Char 0	Auto Enable	Enter Hunt Mode	Rx CRC Enable	Address Search Mode (SDLC)	SYNC Char Load Inhibit	Receiver Enable
Tx/Rx Misc. Modes	WR4 RR4	4 (RD/WR)	Clock Rate 1	Clock Rate 0	SYNC Mode 1	SYNC Mode 0	Stop Bits 1	Stop Bits 0	Even Parity	Parity Enable
Transmit Control	WR5 RR5	5 (RD/WR)	DTR	Tx Bits /Char 1	Tx Bits /Char 0	Send Break	Transmit Enable	SDLC/ CRC-16	RTS	Tx CRC Enable
SYNC Char or SDLC Address	WR6 RR6	6 (RD/WR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC Char or SDLC Flag	WR7 RR7	7 (RD/WR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit Buffer Register	WR8	8 D/C=1 A/B=1 (WR only)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master Interrupt Control	WR9 RR9	9 (RD/WR)	Reset Command 1	Reset Command 0	0	Status High	Master Interrupt Enable (MIE)	0	0	Vector Includes Status
Tx/Rx Misc. Control	WR10	10 (WR only)	CRC Preset	Data Encoding 1	Data Encoding 0	Go Active on Poll	Mark Idle	Abort on Underrun	Loop	6 Bit Sync
Clock Mode Control	WR11 RR11	11 (RD/WR)	Manchester Encode Transmit	Receive Clock Source 1	Receive Clock Source 0	Transmit Clock Source 1	Transmit Clock Source 0	TRxC Pin Output	TRxC Output Source 1	TRxC Output Source 0
Lower Byte Baud Generator	WR12 RR12	12 (RD/WR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Upper Byte Baud Generator	WR13 RR13	13 (RD/WR)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Misc. Control	WR14 RR14	14 (RD/WR)	PLL Command 2	PLL Command 1	PLL Command 0	Local Loopback	Auto Echo	TX CRC-32	Baud Generator Source	Baud Generator Enable
External /Status Interrupt Control	WR15 RR15	15 (RD/WR)	Break/ Abort Interrupt Control	Tx Underrun /EOM Int. En.	CTS Interrupt Enable	Sync/ Hunt Interrupt Enable	DCD Interrupt Enable	DSR Interrupt Enable	Zero Count Interrupt Enable	RI Interrupt Enable

TABLE 3: SCC Channel A Write Registers

SSI 73M650/1650

Serial Packet Controller

			DATA BIT NUMBER							
REGISTER		ADDRESS WR0 (3:0)	D7	D6	D5	D4	D3	D2	D1	D0
Tx/Rx Buffer/ External Status	RR0	0	Break/ Abort Detect	Transmit Underrun /EOM	CTS	Hunt	DCD	Transmit Buffer Empty	Zero Count	Receive Char. Available
Special Receive Condition Status	RR1	1	End of Frame (SDLC)	CRC/ Framing Error	Receive Overrun Error	Parity/ CRC-32 Error	Bit Remainder 2	Bit Remainder 1	Bit Remainder 0	All Sent
Interrupt Vector Register	RR2	2	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Interrupt Pending Register	RR3	3	0	0	Channel A Receive Interrupt Pending	Channel A Transmit Interrupt Pending	Channel A Ext/Status Interrupt Pending	Channel B Interrupt ID 2	Channel B Interrupt ID 1	Channel B Interrupt ID 0
Receive Data Register	RR8	8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Misc. Status	RR10	10	One Clock Missing	Two Clocks Missing	DSR	Loop Sending	CRC16	CRC32	On Loop	RI

TABLE 4: SCC Channel A Read Registers

ADDRESS MAPPING: Single Processor Register Maps in Single-Chip-Select Mode

REGSEL1	REGSEL0	A2	A1	A0	A/ $\bar{B}$	D/ $\bar{C}$	Addressed Register
0	0	000 - 111			X	X	550 Registers as normal
0	1	0	00 - 11		X	X	550 Registers as normal
0	1	1	X	X	0	0	Channel B Control
0	1	1	X	X	0	1	Channel B Data
0	1	1	X	X	1	0	Channel A Control
0	1	1	X	X	1	1	Channel A Data
1	1	X	X	X	X	X	External Device

FIGURE 8: 40 and 44 Pin Versions

REGSEL1	REGSEL0	A2	A1	A0	A/ $\bar{B}$	D/ $\bar{C}$	Addressed Register
0	0	000 - 111			-	-	550 Registers as normal
0	1	0	00 - 11		-	-	550 Registers as normal
0	1	1	0	0	-	-	Channel A Data
0	1	1	0	1	-	-	Channel A Control
0	1	1	1	0	-	-	Channel B Data
0	1	1	1	1	-	-	Channel B Control

FIGURE 9: 28 Pin Version (73M1650)

SSI 73M650/1650 Serial Packet Controller

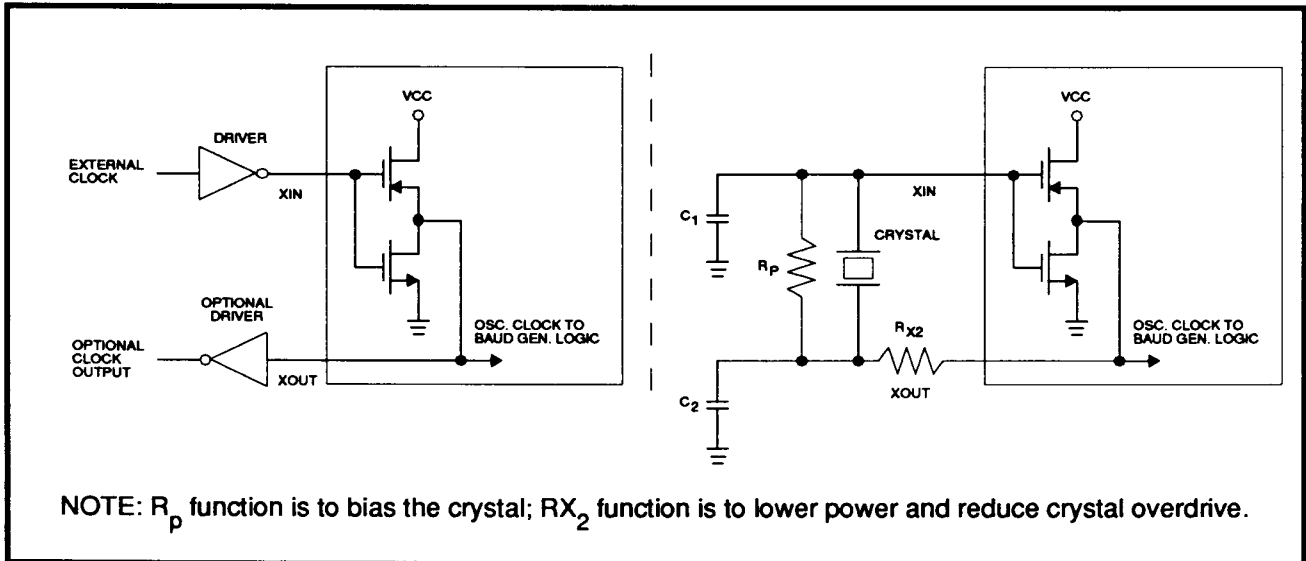


FIGURE 4: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 MHz	1 M Ω	1.5K	10-30 pF	40-60 pF
20 MHz	1 M Ω	0	10-30 pF	10-30 pF

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+7V
Storage Temperature		-65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		-0.3 to $V_{CC} + 0.3$

SSI 73M650/1650

Serial Packet Controller

DC CHARACTERISTICS

(TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
VILX Clock Input Low Voltage		-0.3		0.8	V
VIHX Clock Input High Voltage		2.0		VCC	V
VIL Input Low Voltage		-0.3		0.8	V
VIH Input High Voltage		2.0		VCC+0.3	V
VOL Output Low Voltage	IOL = -5 mA (except XOUT, MD0-MD7)			0.4	V
VOL Output Low Voltage, MD0-MD7	IOL = -3 mA			0.4	V
VOH Output High Voltage	IOH = 5 mA (except XOUT & MINT)	2.4			V
IOH Output High Current	MINT = 2.5V	20		250	μA
ICC1 Supply Current	See Note 1		2	10	mA
ICC2 Power Down Current	See Note 2			50	μA
IIL Input Leakage				±10	μA
IOZ High-Impedance Leakage				±20	μA

Note 1: Outputs unloaded, CMOS level inputs, Xtal = Data Rate = 10 MHz.

Note 2: Outputs unloaded, CMOS level input, Oscillator disabled or XIN = VCC.

AC CHARACTERISTICS

(TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

PARAMETER	MIN	NOM	MAX	UNITS
tCD TRXC (Transmit Clock) or RTXC (Receive Clock) to TXdata		75	150	ns
fOSC Baud Rate Crystal/External Clock	0		20	MHz
fBG Baud Rate Generator			15	MHz
fDPLL Input Frequency Digital Phase Lock Loop DPLL	0		20	MHz
fDATA Serial Data Rate	0		6	MBit/s
fDLOOP Serial Data Rate SDLC Loop Mode Bit/s	0		4	Mbit/s

SSI 73M650/1650

Serial Packet Controller

READ AND WRITE CYCLE – DUAL PROCESSOR (Refer to Figures 5 & 6)

PARAMETER	MIN	NOM	MAX	UNITS
tAR Address Setup before READ (CS2)	15	0		ns
tARM Address Setup before READ (MCS)	15	0		ns
tAW Address Setup before WRITE (CS2)	15	0		ns
tAWM Address Setup before WRITE (MCS)	15	0		ns
tRA Address Hold after READ with CS2	10	0		ns
tWA Address Hold after WRITE with CS2	10	0		ns
tRAS Address Hold after READ with MCS	20	10		ns
tWAS Address Hold after WRITE with MCS	20	10		ns
tRD READ Minimum Width Asserted with CS2	60	25		ns
tWR WRITE Minimum Width Asserted with CS2	60	25		ns
tRDM READ Minimum Width Asserted with MCS	80	25		ns
tWRM WRITE Minimum Width Asserted with MCS	80	25		ns
tRDV READ to Data Output Asserted with CS2		25	60	ns
tRDVM READ to Data Output Asserted with MCS		25	80	ns
tDS DATA Setup before end of WRITE	30	5		ns
tDH DATA Hold Time after WRITE	30	5		ns
tHZ DATA to High Impedance after READ		15	30	ns
tDVC Address to Data Available Dual Processor using CS2		60	100	ns
tDVM Address to Data Available Dual Processor using MCS		90	140	ns
tRC Channels A & B Register Bank, End of READ Cycle to a subsequent to New Command Cycle	200	100		ns
tWC Channels A & B Register Bank, End of WRITE Cycle Command to a subsequent New Command Cycle	200	100		ns
tRC End of READ Cycle to next Read Cycle, 550 UART registers	30	10		ns
tWC End of WRITE Cycle to next Write Cycle, 550 UART registers	30	10		ns

SSI 73M650/1650

Serial Packet Controller

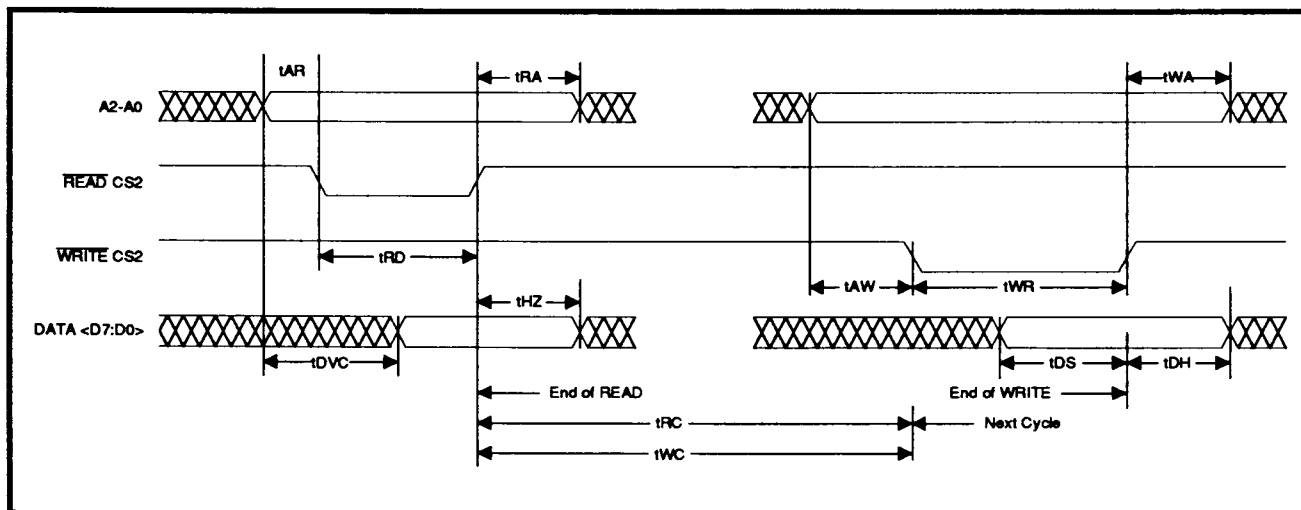


FIGURE 5: CPU/Host Processor Bus

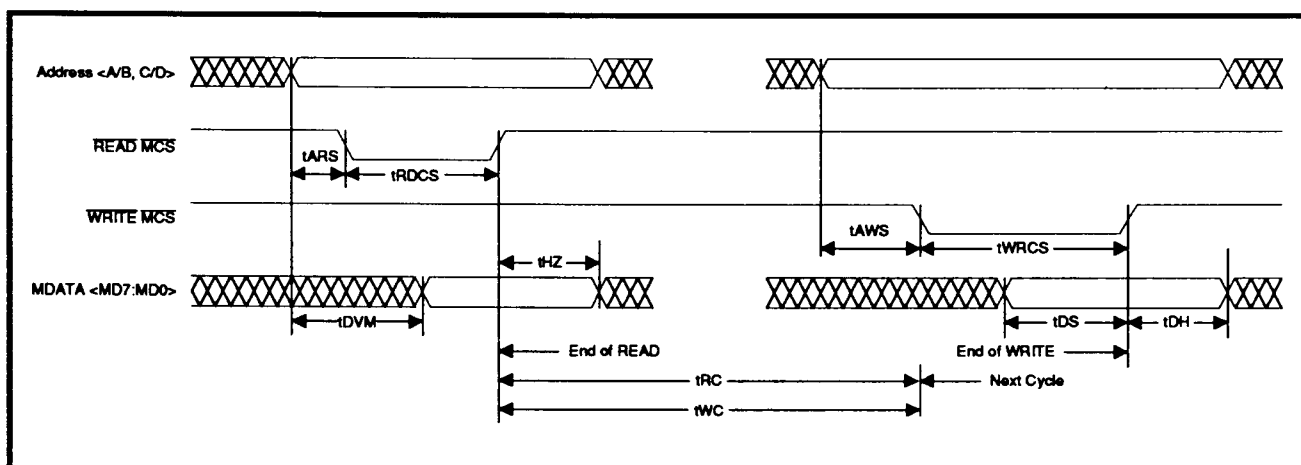


FIGURE 6: Local Controller Bus

NOTES: $\overline{\text{READ CS}}$ is active when ($\overline{\text{RD}}$ and $\overline{\text{CS2}}$) are asserted
 $\overline{\text{WRITE CS}}$ is active when ($\overline{\text{WR}}$ and $\overline{\text{CS}}$) are asserted
 $\overline{\text{READ MCS}}$ is active when ($\overline{\text{MRD}}$ and $\overline{\text{MCS}}$) are asserted
 $\overline{\text{WRITE MCS}}$ is active when ($\overline{\text{MWR}}$ and $\overline{\text{MCS}}$) is asserted

SSI 73M650/1650 Serial Packet Controller

AC CHARACTERISTICS

(TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

READ AND WRITE CYCLE – SINGLE PROCESSOR (Refer to Figure 7)

PARAMETER	MIN	NOM	MAX	UNITS
tAR Address Setup before READ (CS2)	15	0		ns
tARM Address Setup before READ (MCS)	15	0		ns
tARS Address Setup before READ SINGLECS	15	0		ns
tAW Address Setup before WRITE (CS2)	15	0		ns
tAWM Address Setup before WRITE (MCS)	15	0		ns
tAWS Address Setup before WRITE SINGLECS	15	0		ns
tRA Address Hold after READ	20	10		ns
tWA Address Hold after WRITE	20	10		ns
tRD READ Minimum Width Asserted with CS2	60	25		ns
tWR WRITE Minimum Width Asserted with CS2	60	25		ns
tRDM READ Minimum Width Asserted with MCS	80	25		ns
tWRM WRITE Minimum Width Asserted with MCS	80	25		ns
tRDCS READ Minimum Width Asserted with SINGLECS	80	30		ns
tWRCS WRITE Minimum Width Asserted with SINGLECS	80	30		ns
tRDV READ to Data Output Asserted with CS2		25	60	ns
tRDVM READ to Data Output Asserted with MCS		25	80	ns
tRDVCS READ to Data Output Asserted with SINGLECS		30	80	ns
tDS DATA Setup before end of WRITE	30	20		ns
tDH DATA Hold Time after WRITE	30	20		ns
tHZ DATA to High Impedance after READ	30	15		ns
tDVSCS Address to Data Available Single Processor (MCS and CS2) SINGLECS		80	140	ns
tDVCSS Address to Data Available Single Processor using CS2		80	140	ns
tDVSMCS Address to Data Available Single Processor using MCS		80	140	ns
tRC Channels A & B Register Bank, End of READ Cycle to a subsequent to New Command Cycle	200	100		ns
tWC Channels A & B Register Bank, End of WRITE Cycle Command to a subsequent New Command Cycle	200	100		ns
tRC End of READ Cycle to next Read Cycle, 550 UART registers	30	10		ns
tWC End of WRITE Cycle to next Write Cycle, 550 UART registers	30	10		ns
tWE WRITE to External Write Data delay		20	40	ns
tRE READ to External READ Data delay		20	40	ns

SSI 73M650/1650

Serial Packet Controller

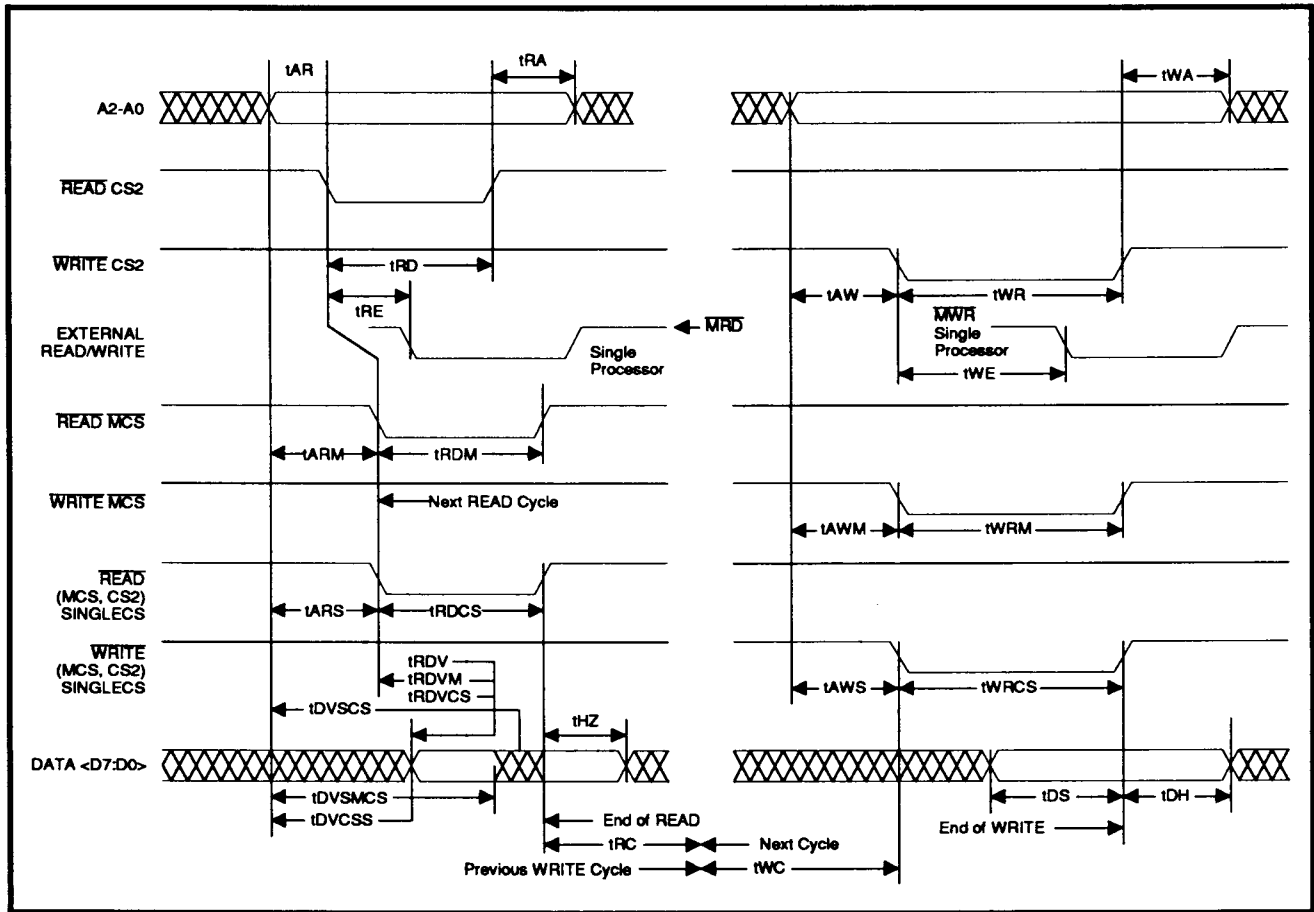


FIGURE 7: CPU/Host Processor Bus

- NOTES:
- $\overline{\text{READ}} \text{ CS}$ is active when ($\overline{\text{RD}}$ and $\overline{\text{CS2}}$) are asserted
 - $\overline{\text{WRITE}} \text{ CS}$ is active when ($\overline{\text{WR}}$ and $\overline{\text{CS}}$) are asserted
 - $\overline{\text{READ}} \text{ MCS}$ is active when ($\overline{\text{MRD}}$ and $\overline{\text{MCS}}$) are asserted
 - $\overline{\text{WRITE}} \text{ MCS}$ is active when ($\overline{\text{MWR}}$ and $\overline{\text{MCS}}$) is asserted
 - $\overline{\text{READ}} \text{ SINGLECS}$ is active when ($\overline{\text{RD}}$ and $\overline{\text{MCS}}$ and $\overline{\text{CS2}}$) are asserted
 - $\overline{\text{WRITE}} \text{ SINGLECS}$ is active when ($\overline{\text{WR}}$ and $\overline{\text{MCS}}$ and $\overline{\text{CS2}}$) are asserted

SSI 73M650/1650 Serial Packet Controller

MODEM CONTROL

PARAMETER	CONDITIONS	MIN	MAX	UNITS
tMDO Delay from WRITE MCR to Output	100 pF load		200	ns
tSIM Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF load		250	ns

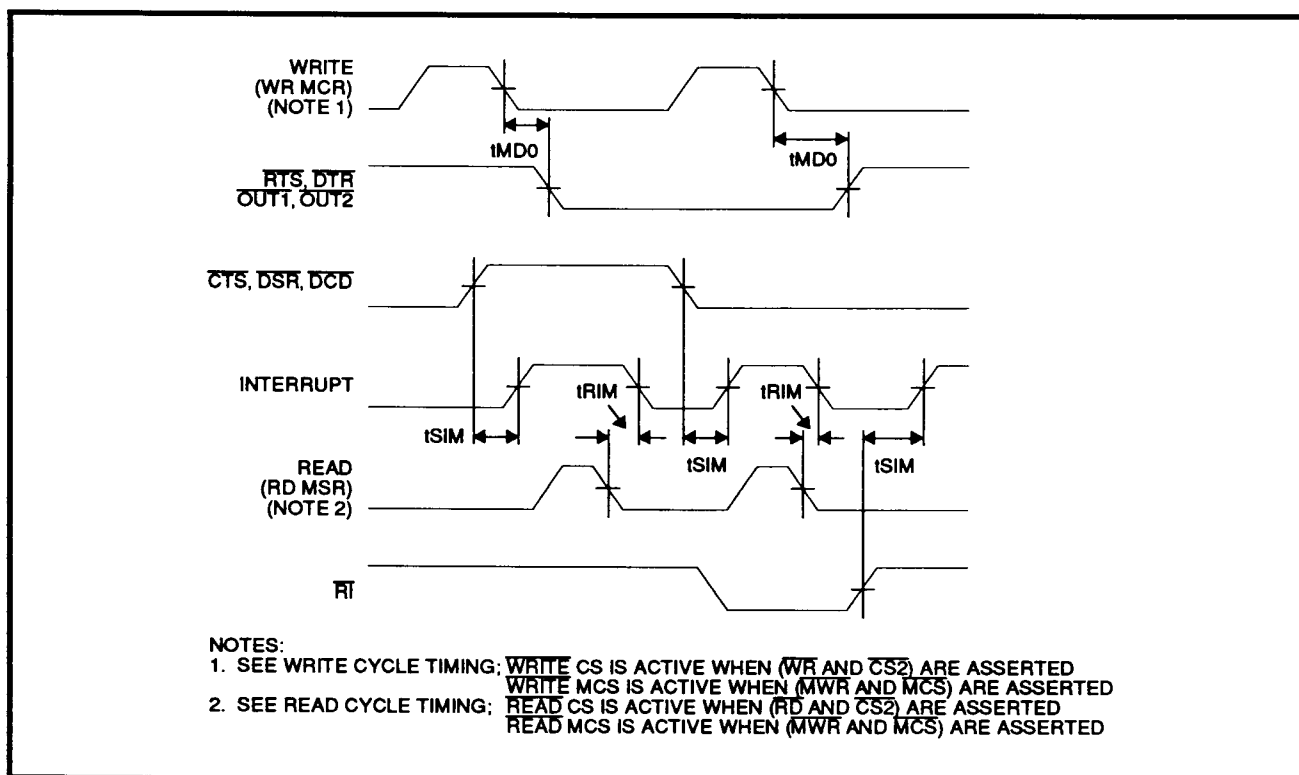


FIGURE 8: Modem Controls Timing

SSI 73M650/1650

Serial Packet Controller

SSI 73M650 TIMING COMPARED TO PCMCIA PC CARD STANDARD - RELEASE 2.0

ITEM	SYMBOL	IEEE	MIN	MAX	SSI 73M650			
					SSI	MIN	MAX	UNITS
Data Setup before IOWR	t _{su} (IOWR)	t _{DVIWL}	60		TDS	30		ns
Data Hold following IOWR	t _h (IOWR)	t _{IWHDX}	30		TDH	30		ns
IOWR Width Time	t _w IOWR	t _{IWLIWH}	165		TWR	80		ns
Address Setup before IOWR	t _{su} A (IOWR)	t _{AVIWL}	70		TAW	30		ns
Address Hold following IOWR	t _h A (IOWR)	t _{IWHAX}	20		TWA	20		ns
CE Setup before IOWR	t _{su} CE (IOWR)	t _{ELIWL}	5			Any		
CE Hold following IOWR	t _h CE (IOWR)	t _{IWHEH}	20			Any		
REG Setup before IOWR	t _{su} REG (IOWR)	t _{RGLIWL}	5					
REG Hold following IOWR	t _h REG (IOWR)	t _{IWHRGH}	0					
IOIS16 Delay Falling from Address	t _d IOIS16 (ADR) ₁	t _{AVISL}		35				
IOIS16 Delay Rising from Address	t _d IOIS16 (ADR) ₂	t _{AVISH}		35				
Wait Delay Falling from IOWR	t _d WAIT (IOWR)	t _{IWLWTL}		35				
Wait Width Time	t _w WAIT	t _{WLWTH}		12,000				
NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.								

TABLE 5: I/O Output (WRITE) Timing Specification for All 5V I/O Cards

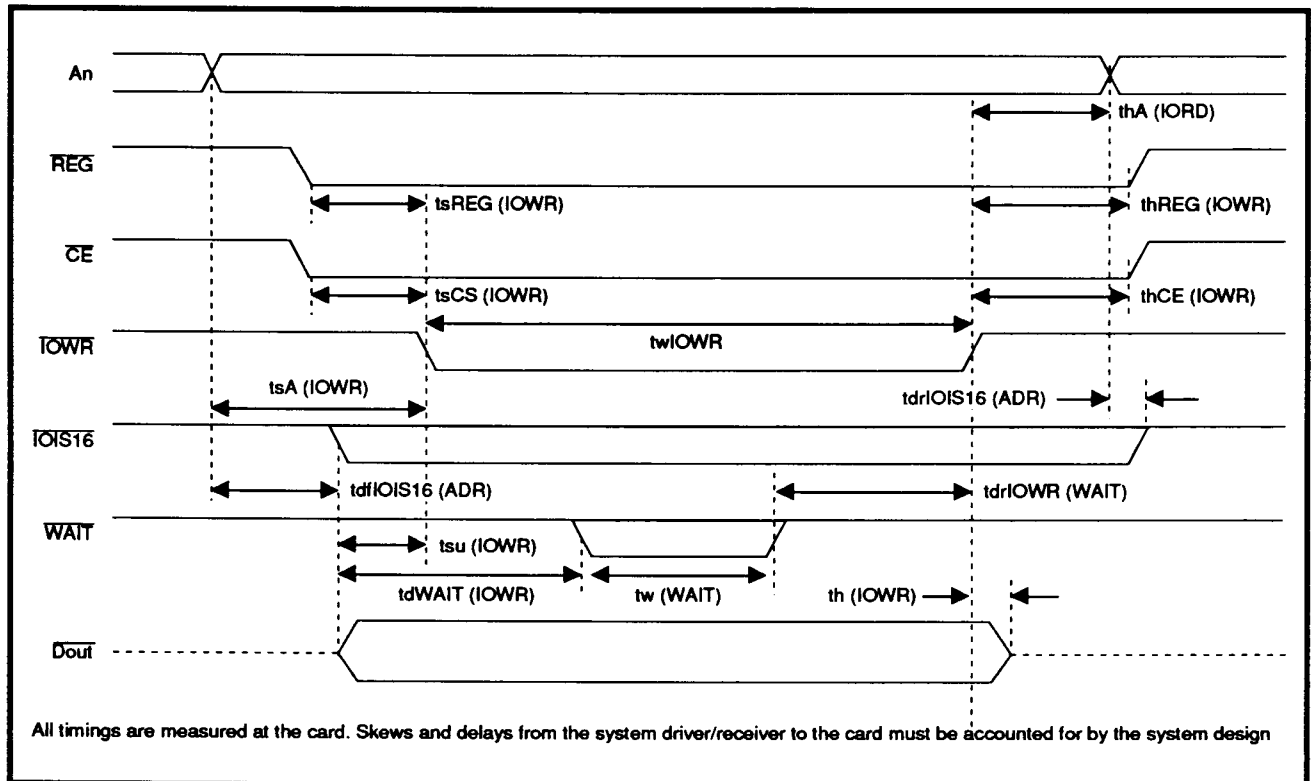


FIGURE 9: I/O Output Timing Specification (WRITE)

SSI 73M650/1650

Serial Packet Controller

SSI 73M650 TIMING COMPARED TO PCMCIA PC CARD STANDARD - RELEASE 2.0

ITEM	SYMBOL	IEEE	MIN	MAX	SSI 73M650			
					SSI	MIN	MAX	UNITS
Data Delay after IORD	t d (IORD)	tIGLQV		100	TRVD		80	ns
Data Hold following IORD	t h (IORD)	tIGHQX	0		THZ	0		ns
IORD Width Time	t w IORD	tIGLIGH	165		TRD	80		ns
Address Setup before IORD	t su A (IORD)	tAVIGL	70		TAR	30		ns
Address Hold following IORD	t h A (IORD)	tIGHAX	20		TRA	20		ns
CE Setup before IORD	t su CE (IORD)	tELIGL	5			Any		
CE Hold following IORD	t h CE (IORD)	tIGHEH	20			Any		
REG Setup before IORD	t su REG (IORD)	tRGLIGL	5					
REG Hold following IORD	t h REG (IORD)	tIGHRGH	0					
INPACK Delay Falling from IORD	t d INPACK (IORD)	tGLIAL	0	45				
INPACK Delay Rising from IORD	t d INPACK (IORD)	tIGHIAH		45				
IOIS16 Delay Falling from Address	t d IOIS16 (ADR) ₁	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 (ADR) ₂	tAVISH		35				
Wait Delay Falling from IORD	t d WAIT (IORD)	tIGLWTL		35				
Data Delay from Wait Rising	td(WAIT)	tWTHQV		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				
NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.								

TABLE 6: I/O Output (READ) Timing Specification for All 5V I/O Cards

SSI 73M650/1650 Serial Packet Controller

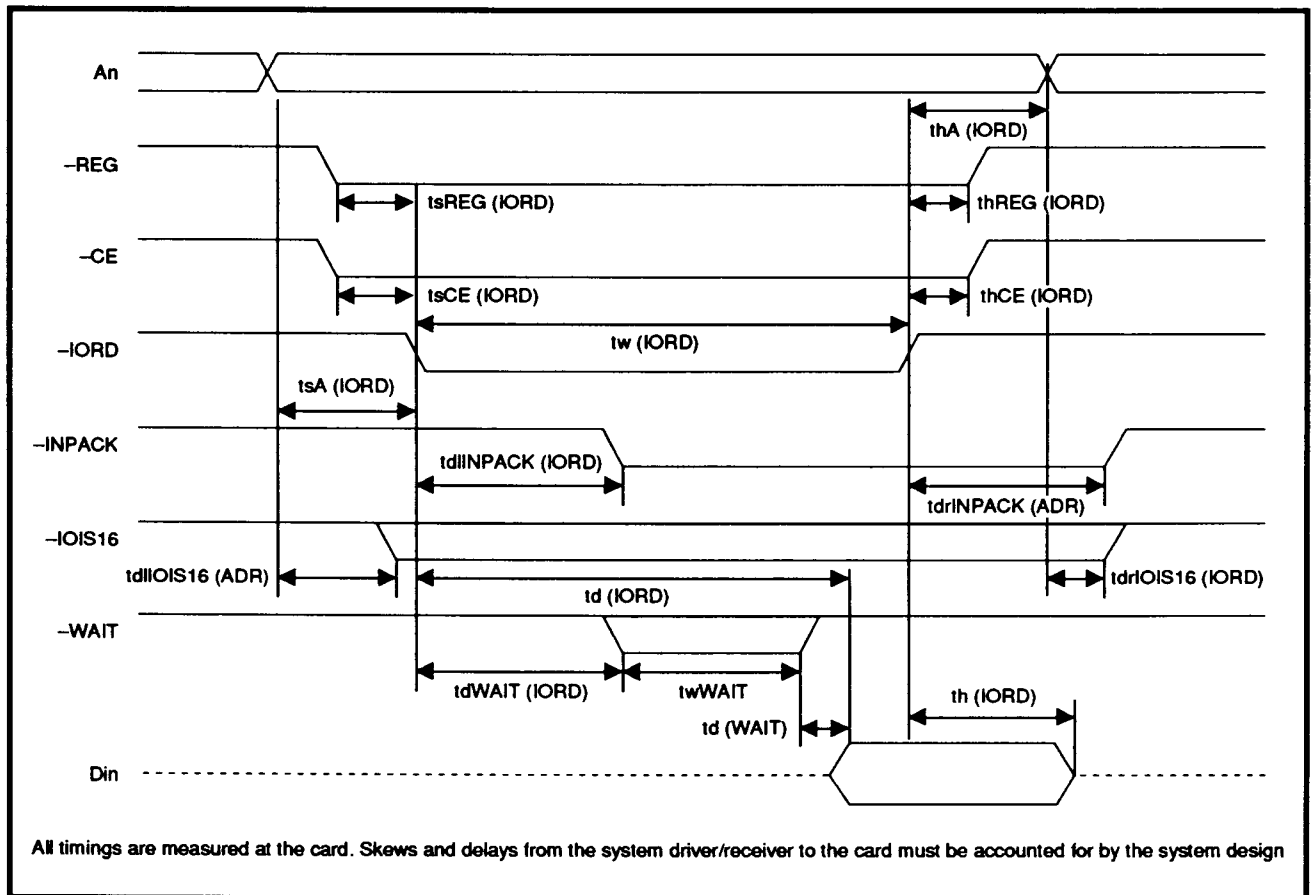


FIGURE 10: I/O Output Timing Specification (READ)

SSI 73M650/1650

Serial Packet Controller

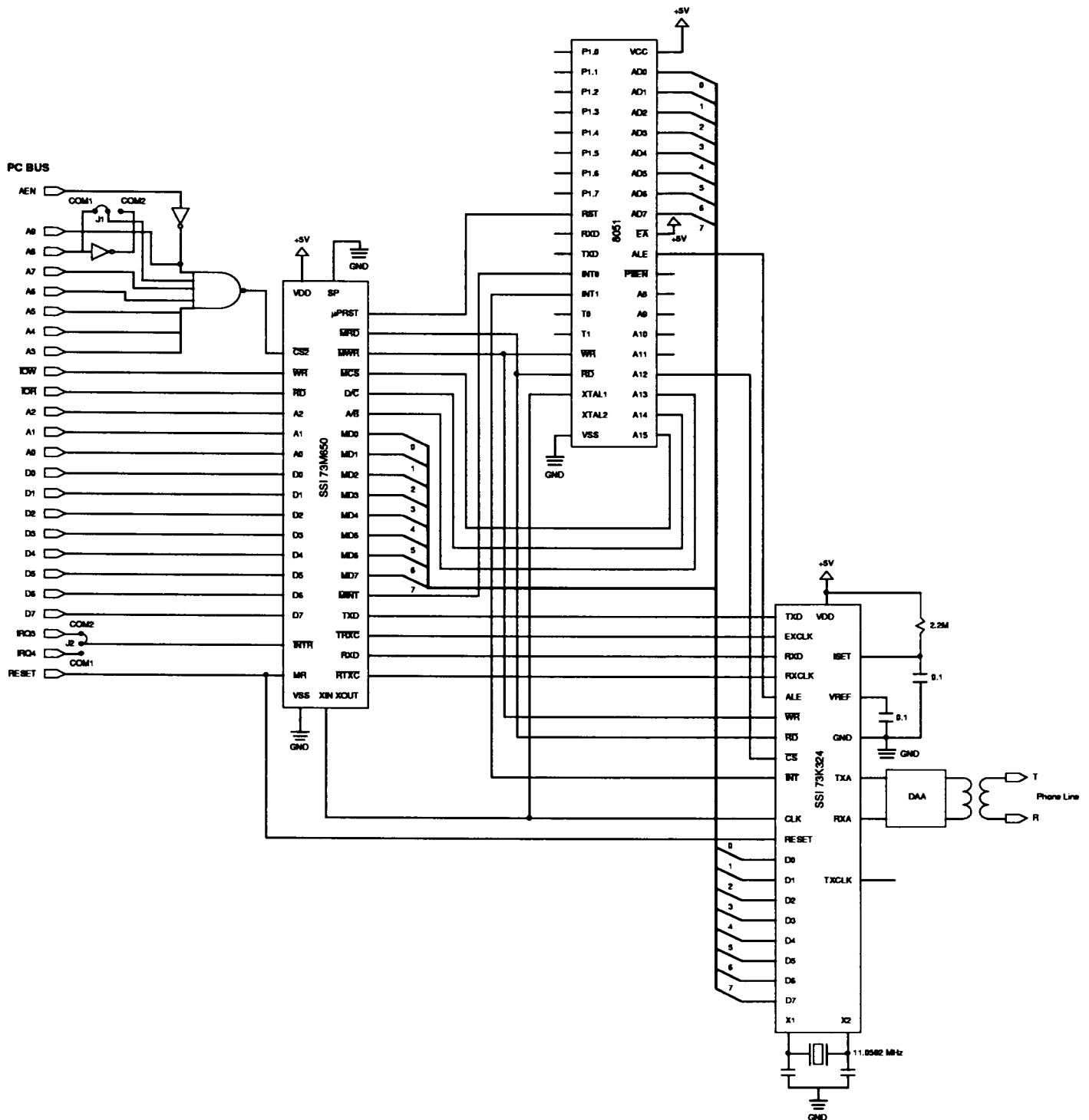


FIGURE 11: Dual-Processor Application Example

SSI 73M650/1650 Serial Packet Controller

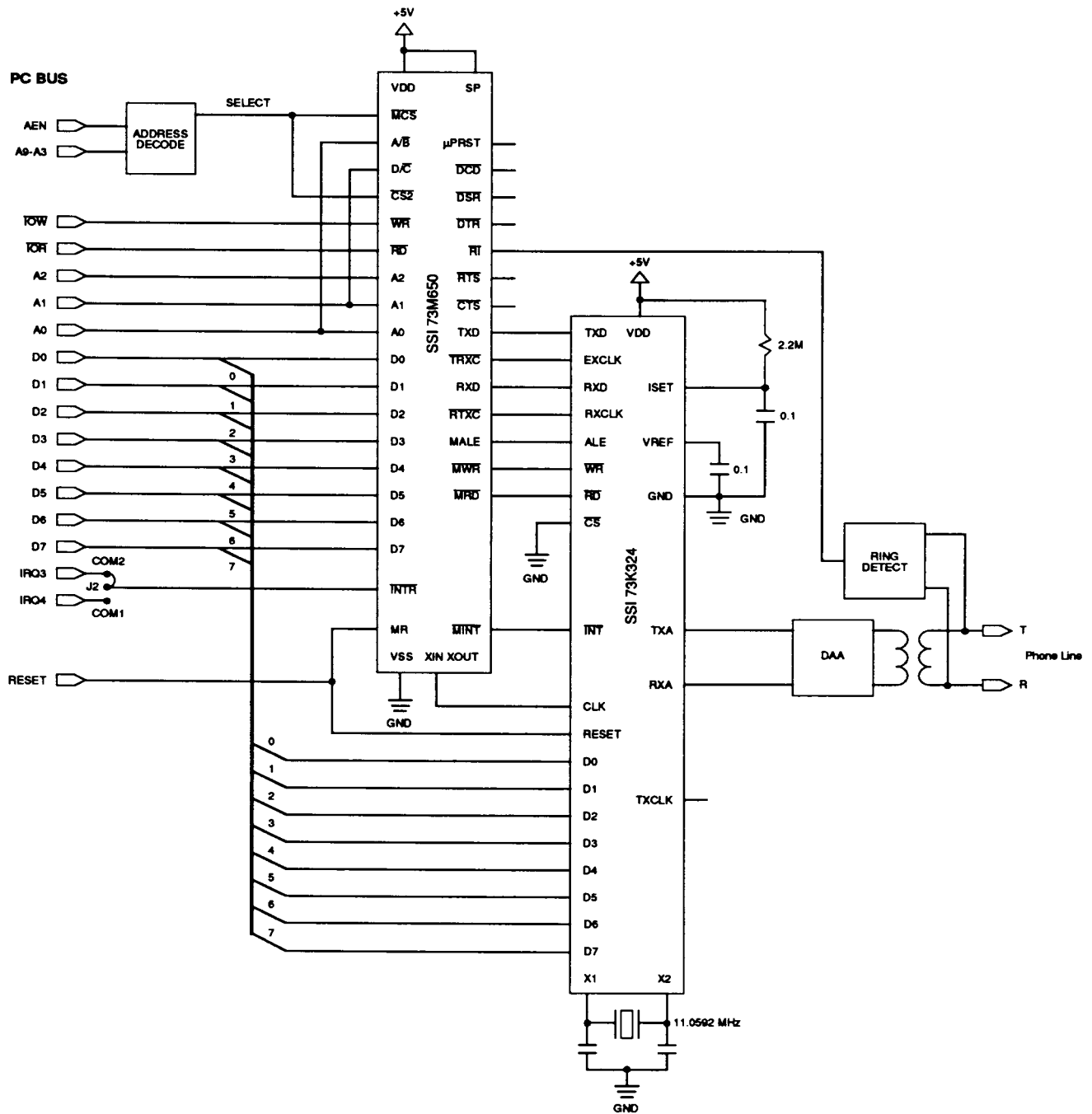


FIGURE 12: Single-Processor Mailbox Mode Application Example

SSI 73M650/1650

Serial Packet Controller

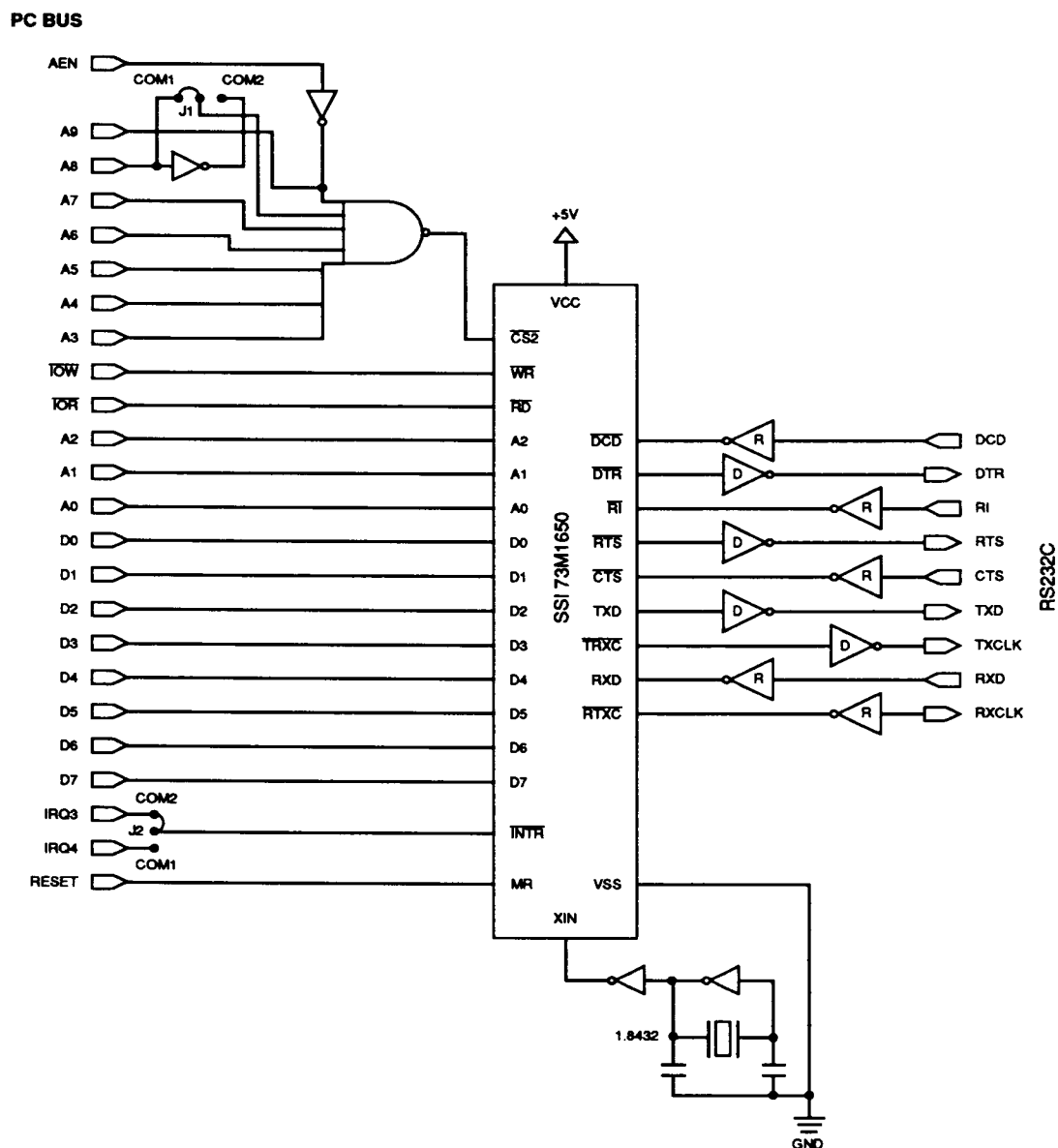
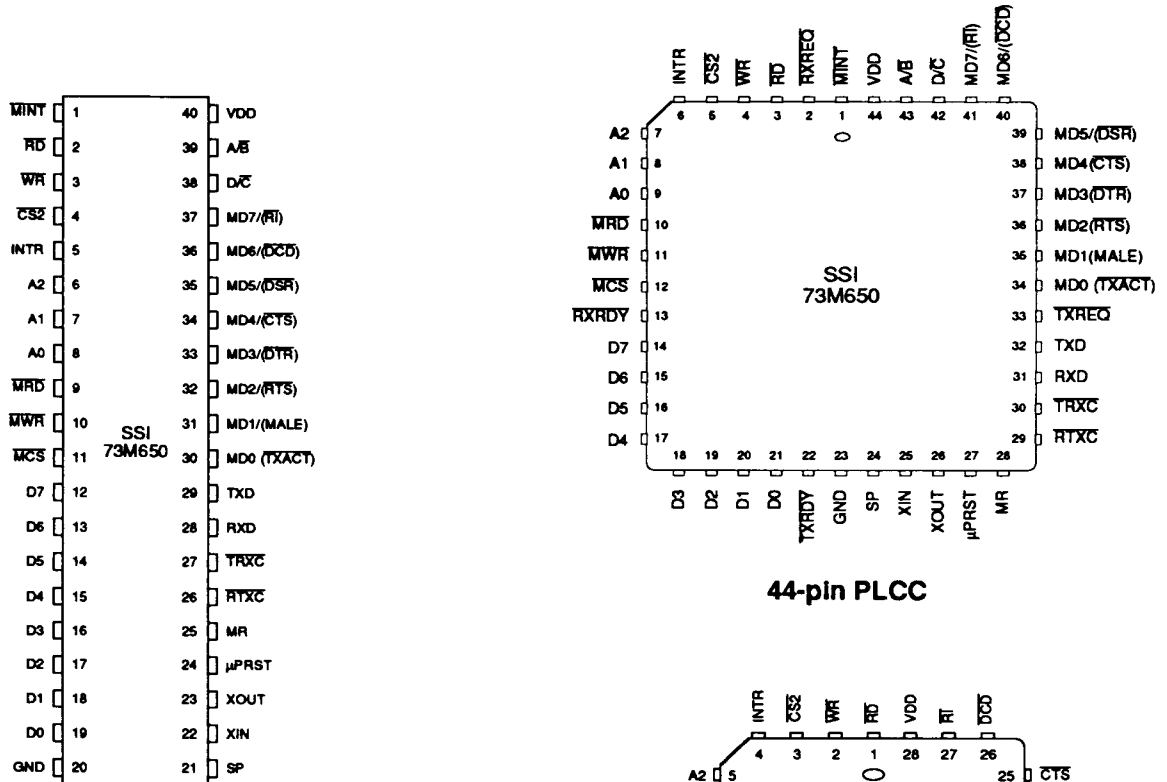


FIGURE 13: Single-Processor Non-Mailbox Mode Application Example

SSI 73M650/1650 Serial Packet Controller

PACKAGE PIN DESIGNATIONS

(Top View)



40-pin DIP

44-pin PLCC

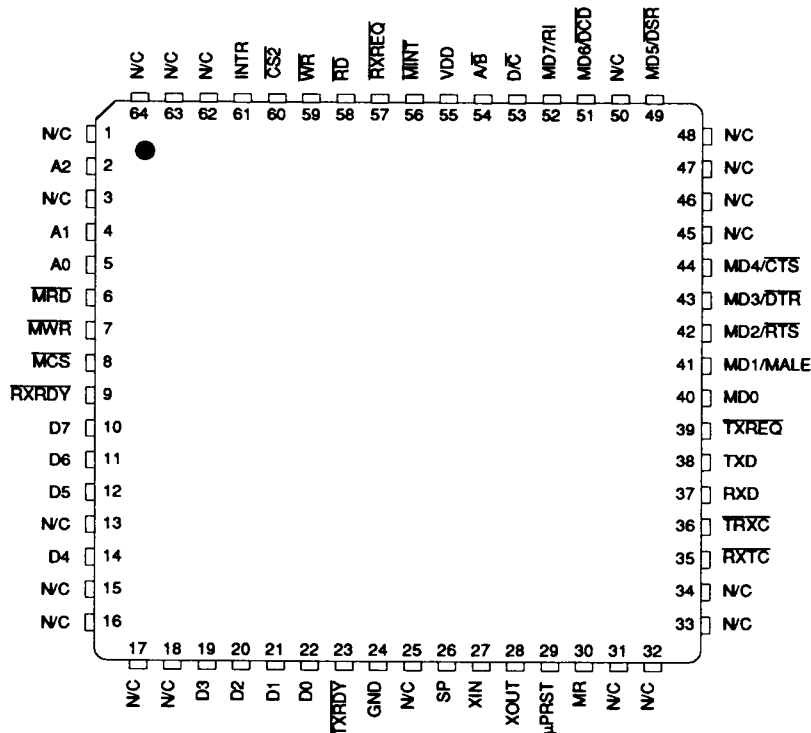
28-pin PLCC

Serial Packet Controller
Package and Configuration Matrix

	Dual Processor	Single Processor Mailbox	Single Processor Non-mailbox
73M650	Yes	Yes	Yes
73M1650	No	Yes	Yes

CAUTION: Use handling procedures necessary for a static sensitive component.

Serial Packet Controller



64-pin TQFP

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 73M650	40-pin PDIP	73M650-IP	73M650-IP
	44-pin PLCC	73M650-IH	73M650-IH
	64-pin TQFP	73M650-IGT	73M650-IGT
SSI 73M1650	28-pin PLCC	73M1650-IH	73M1650-IH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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