



# PAL20R8 Family

## 24-Pin TTL Programmable Array Logic

### DISTINCTIVE CHARACTERISTICS

- 5-ns propagation delay
- Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

### GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) includes the PAL20R8-5 Series which is ideal for high-performance applications. The PAL20R8 Family is provided in the standard 24-pin DIP and 28-pin PLCC pinouts.

The devices provide user programmable logic for replacing conventional SSI/LSI gates and flip-flops at a reduced chip cost.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

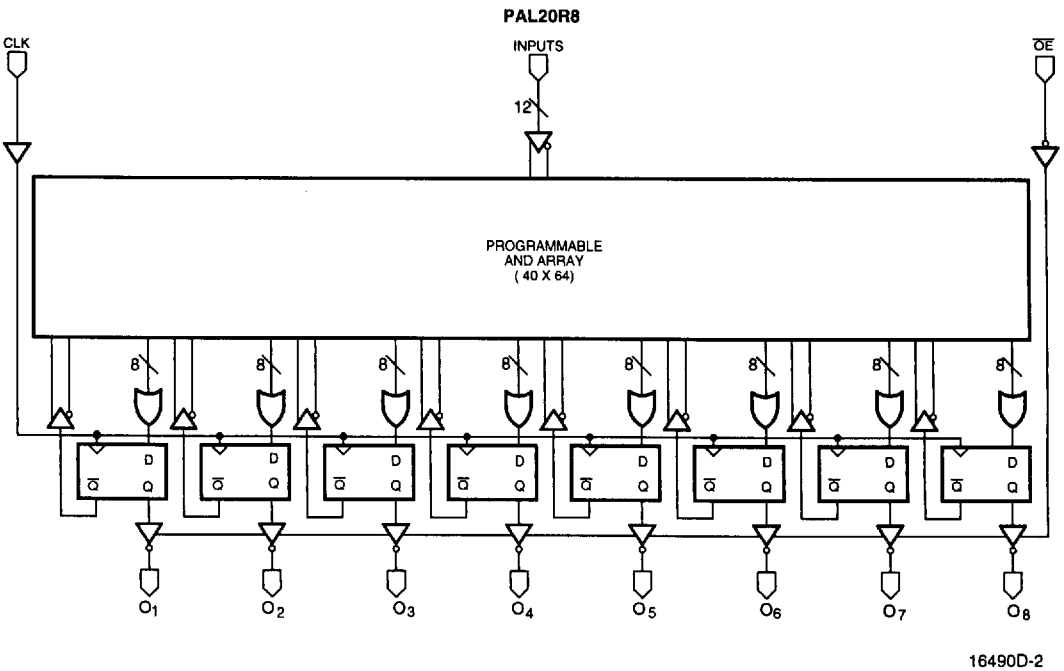
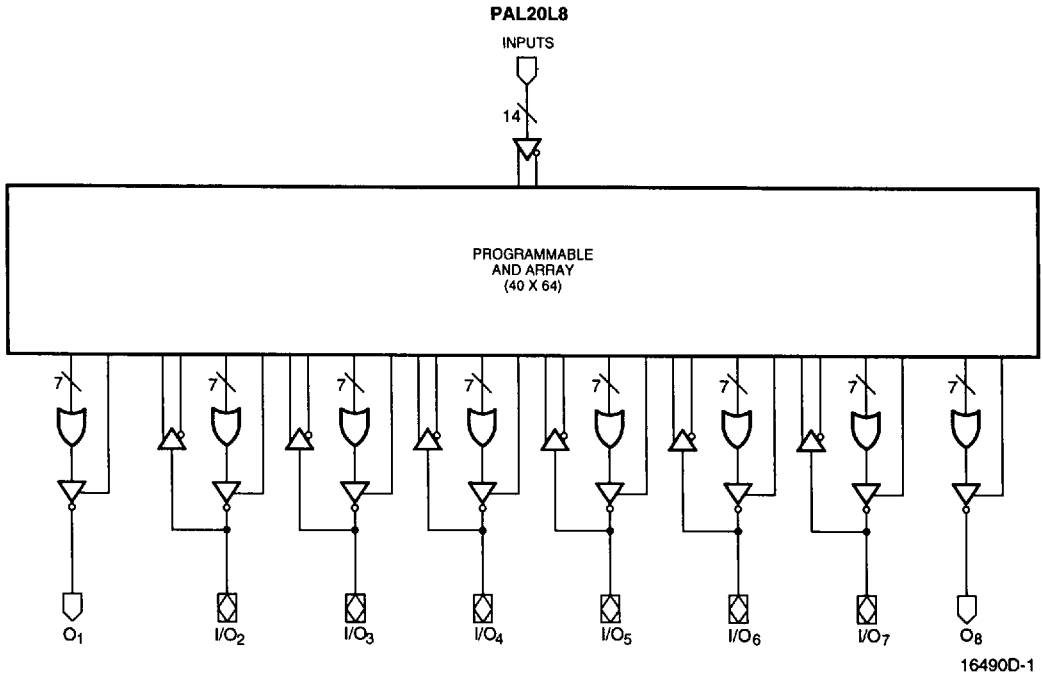
Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to V<sub>cc</sub> or GND.

AMD's FusionPLD program allows PAL20R8 Family designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

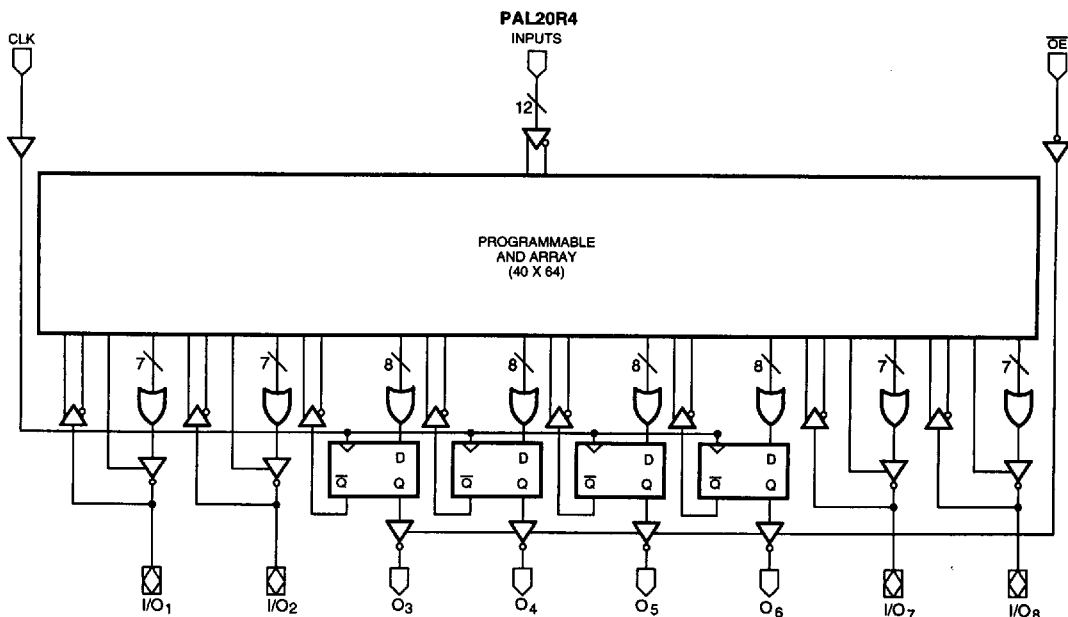
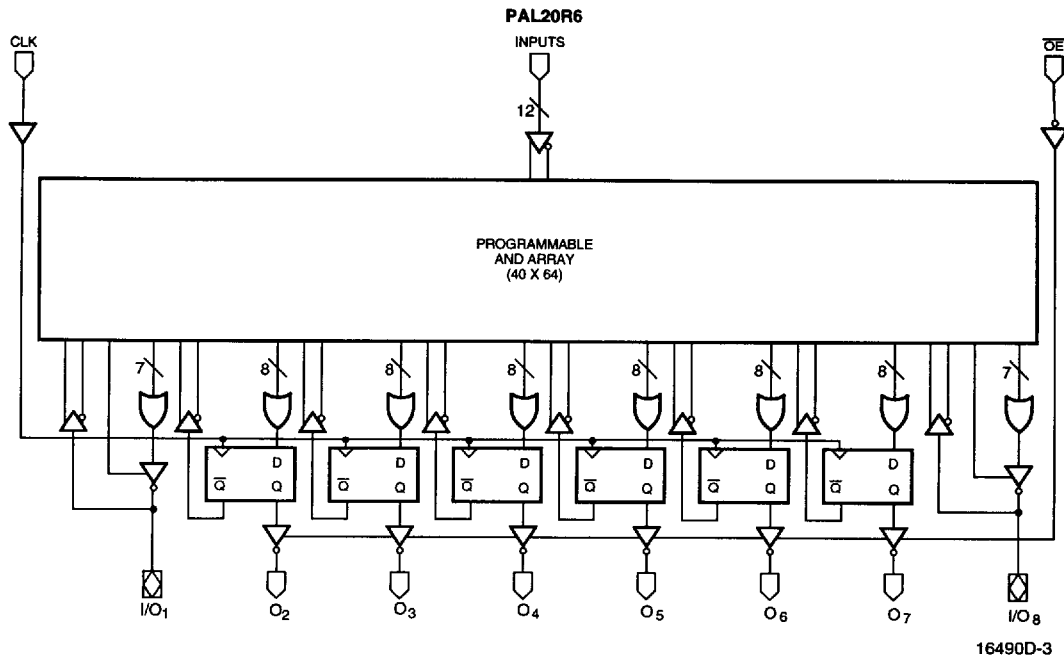
### PRODUCT SELECTOR GUIDE

| Device  | Dedicated Inputs | Outputs                         | Product Terms/Output | Feedback    | Enable         |
|---------|------------------|---------------------------------|----------------------|-------------|----------------|
| PAL20L8 | 14               | 6 comb. I/Os<br>2 comb. Outputs | 7<br>7               | I/O<br>—    | prog.<br>prog. |
| PAL20R8 | 12               | 8 reg.                          | 8                    | reg.        | pin            |
| PAL20R6 | 12               | 6 reg.<br>2 comb.               | 8<br>7               | reg.<br>I/O | pin<br>prog.   |
| PAL20R4 | 12               | 4 reg.<br>4 comb.               | 8<br>7               | reg.<br>I/O | pin<br>prog.   |

**BLOCK DIAGRAMS**



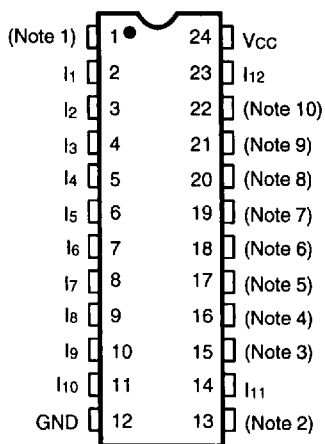
BLOCK DIAGRAMS



## CONNECTION DIAGRAMS

### Top View

#### SKINNYDIP/FLATPACK



16490D-5

**Note:** Pin 1 is marked for orientation.

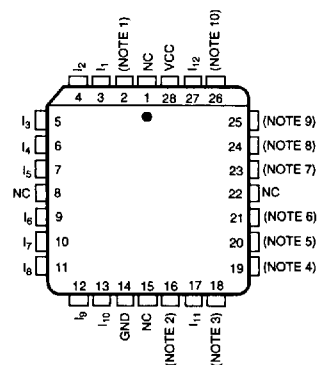
| Note | 20L8             | 20R8            | 20R6             | 20R4             |
|------|------------------|-----------------|------------------|------------------|
| 1    | I <sub>0</sub>   | CLK             | CLK              | CLK              |
| 2    | I <sub>13</sub>  | $\overline{OE}$ | $\overline{OE}$  | $\overline{OE}$  |
| 3    | O <sub>1</sub>   | O <sub>1</sub>  | I/O <sub>1</sub> | I/O <sub>1</sub> |
| 4    | I/O <sub>2</sub> | O <sub>2</sub>  | O <sub>2</sub>   | I/O <sub>2</sub> |
| 5    | I/O <sub>3</sub> | O <sub>3</sub>  | O <sub>3</sub>   | O <sub>3</sub>   |
| 6    | I/O <sub>4</sub> | O <sub>4</sub>  | O <sub>4</sub>   | O <sub>4</sub>   |
| 7    | I/O <sub>5</sub> | O <sub>5</sub>  | O <sub>5</sub>   | O <sub>5</sub>   |
| 8    | I/O <sub>6</sub> | O <sub>6</sub>  | O <sub>6</sub>   | O <sub>6</sub>   |
| 9    | I/O <sub>7</sub> | O <sub>7</sub>  | O <sub>7</sub>   | I/O <sub>7</sub> |
| 10   | O <sub>8</sub>   | O <sub>8</sub>  | I/O <sub>8</sub> | I/O <sub>8</sub> |

#### PIN DESIGNATIONS

CLK = Clock  
 GND = Ground  
 I = Input  
 I/O = Input/Output  
 NC = No Connect  
 O = Output  
 $\overline{OE}$  = Output Enable  
 Vcc = Supply Voltage

#### PLCC/LCC

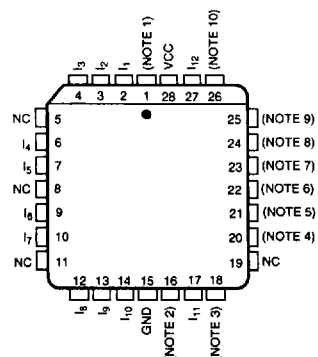
JEDEC: Applies to -5, -7, -10, B-2 Series Only



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#### PLCC

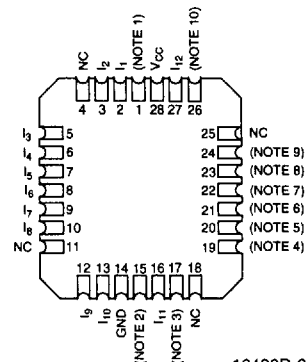
Applies to B and A Series Only



16490D-7

#### LCC

Applies to B and A Series Only

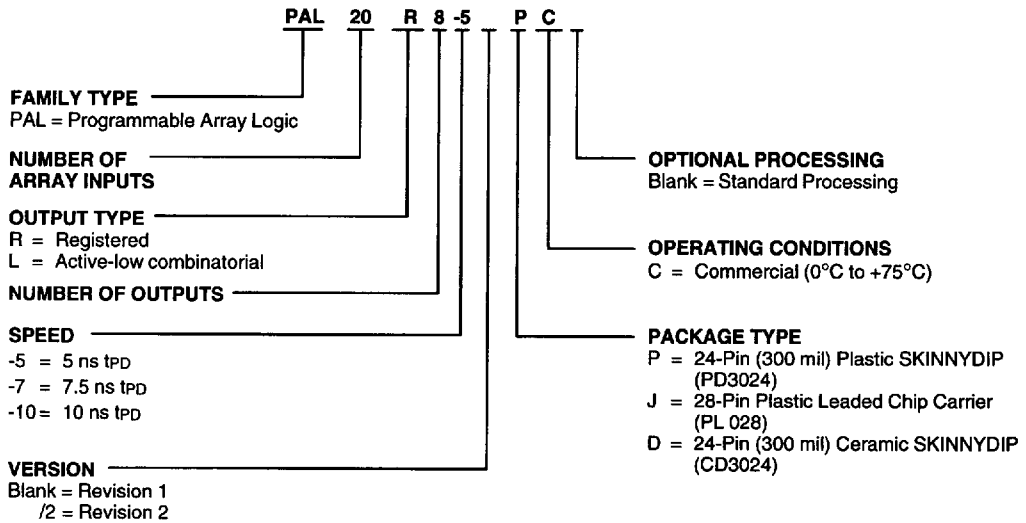


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## ORDERING INFORMATION

### Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



| Valid Combinations |            |
|--------------------|------------|
| PAL20L8-5          | PC, JC     |
| PAL20R8-5          |            |
| PAL20R6-5          |            |
| PAL20R4-5          |            |
| PAL20L8-10/2       |            |
| PAL20R8-10/2       |            |
| PAL20R6-10/2       |            |
| PAL20R4-10/2       |            |
| PAL20L8-7          | PC, JC, DC |
| PAL20R8-7          |            |
| PAL20R6-7          |            |
| PAL20R4-7          |            |

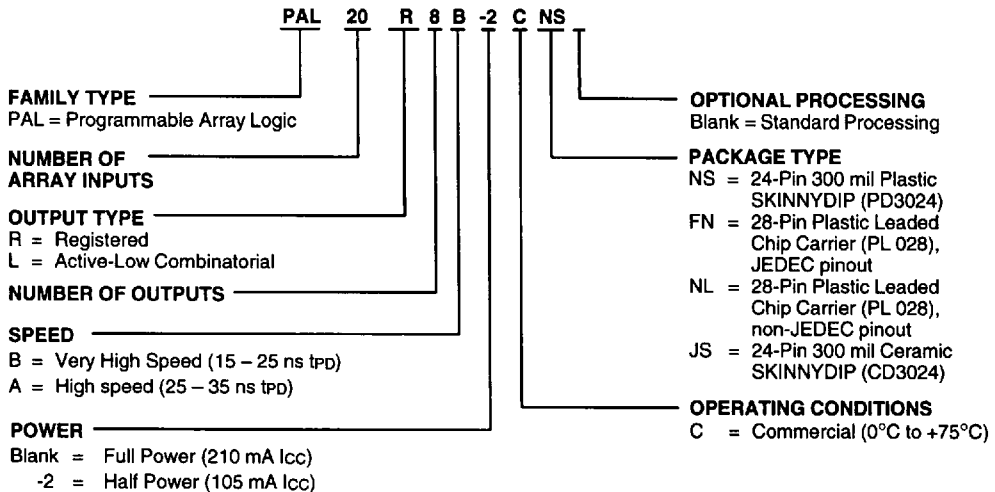
#### Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## ORDERING INFORMATION

### Commercial Products (MMI Marking Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



| Valid Combinations |      |               |
|--------------------|------|---------------|
| PAL20L8            | B-2  | CNS, CFN, CJS |
| PAL20R8            | B, A | CNS, CNL, CJS |
| PAL20R6            |      |               |
| PAL20R4            |      |               |

#### Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

*Note:* Marked with MMI logo.

## FUNCTIONAL DESCRIPTION

### Standard 24-Pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Using any of a number of development packages, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

### Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V<sub>cc</sub> or GND.

### Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

### Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock input.

### Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The V<sub>cc</sub> rise must be monotonic and the reset delay time is 1000 ns maximum.

### Register Preload

The register on the AMD marked 20R8, 20R6, and 20R4 devices can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

### Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is intact.

### Quality and Testability

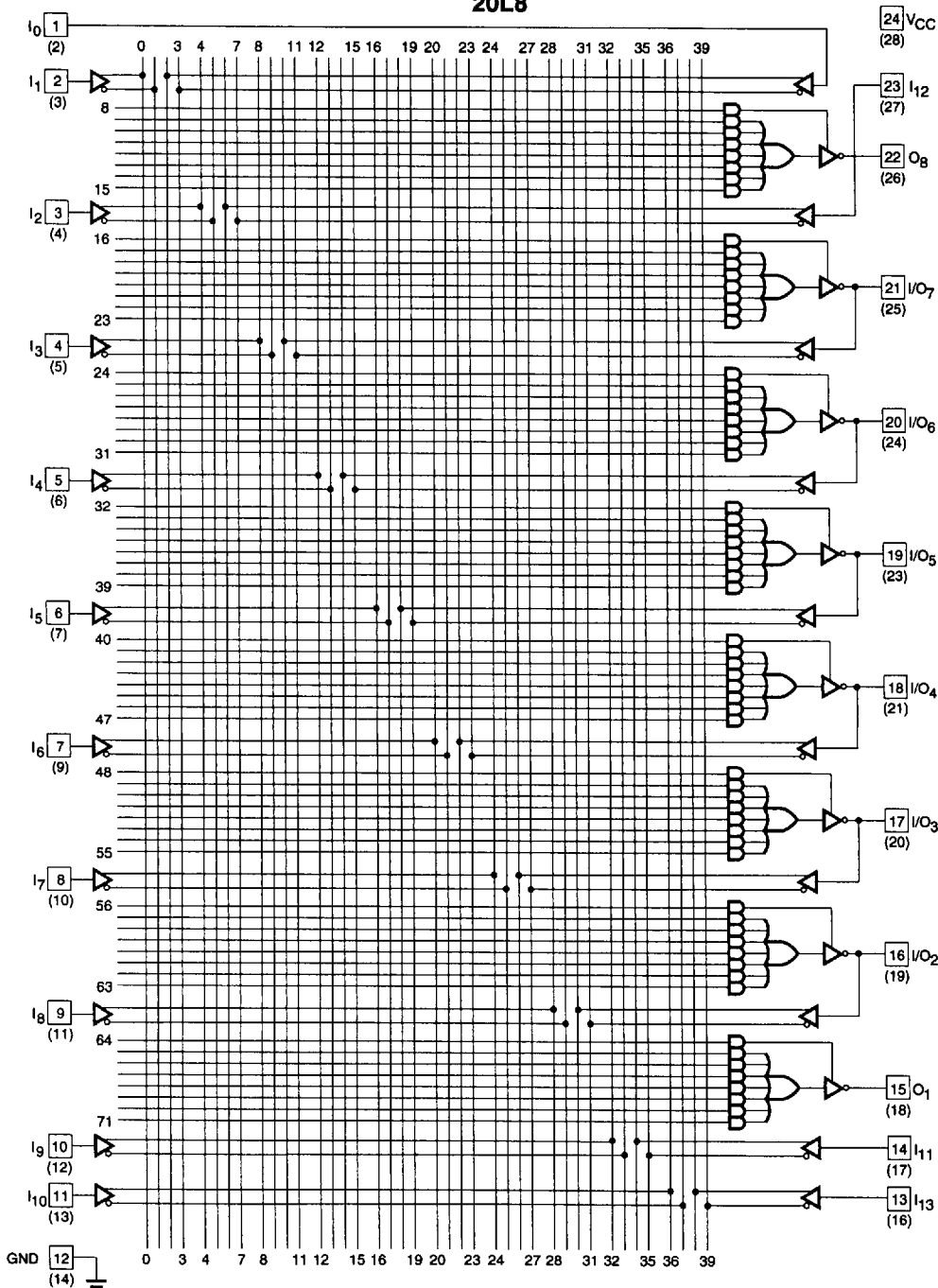
The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

### Technology

The PAL20R8-5, -7 and 10/2 are fabricated with AMD's oxide isolated process. The array connections are formed with highly reliable PtSi fuses. The PAL20R8B, B-2, and A series are fabricated with AMD's trench-isolated bipolar process. The array connections are formed with proven TiW fuses. These processes reduce parasitic capacitances and minimum geometries to provide higher performance.

**LOGIC DIAGRAM**  
**DIP (PLCC) Pinouts**

**20L8**



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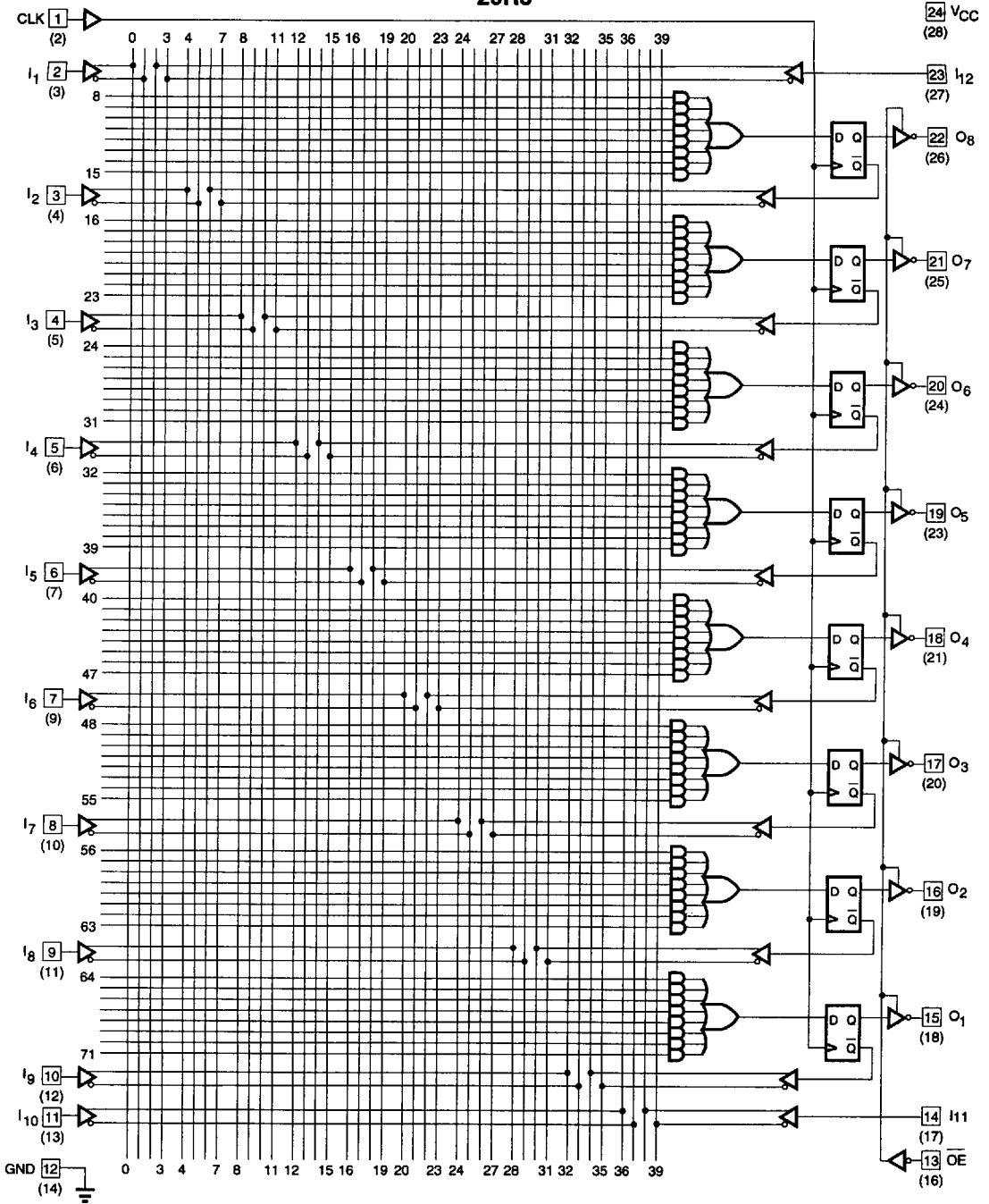
0257526 0036740 810



# LOGIC DIAGRAM

## DIP (PLCC) Pinouts

20R8

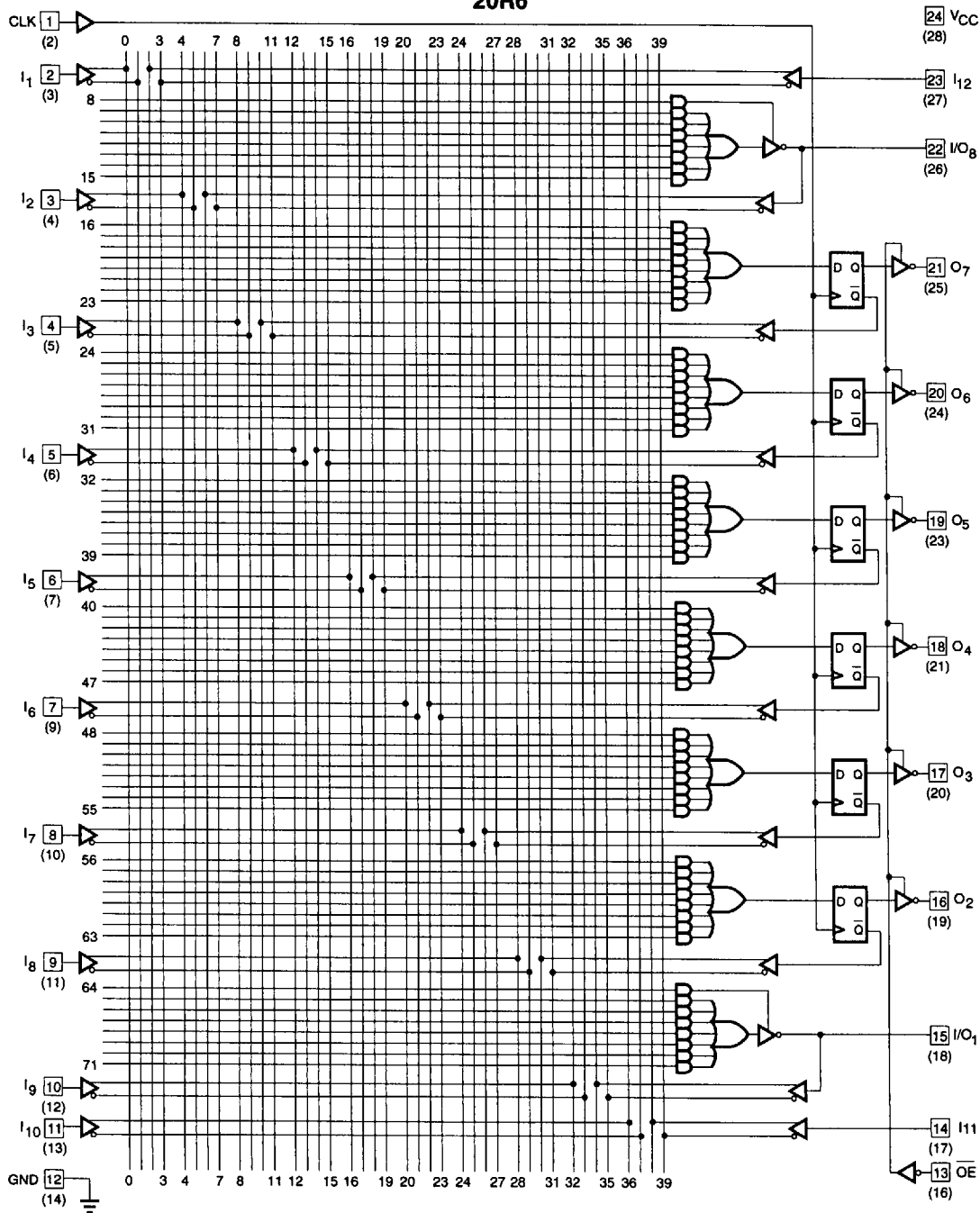


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0257526 003674J 757

**LOGIC DIAGRAM**  
**DIP (PLCC) Pinouts**

**20R6**



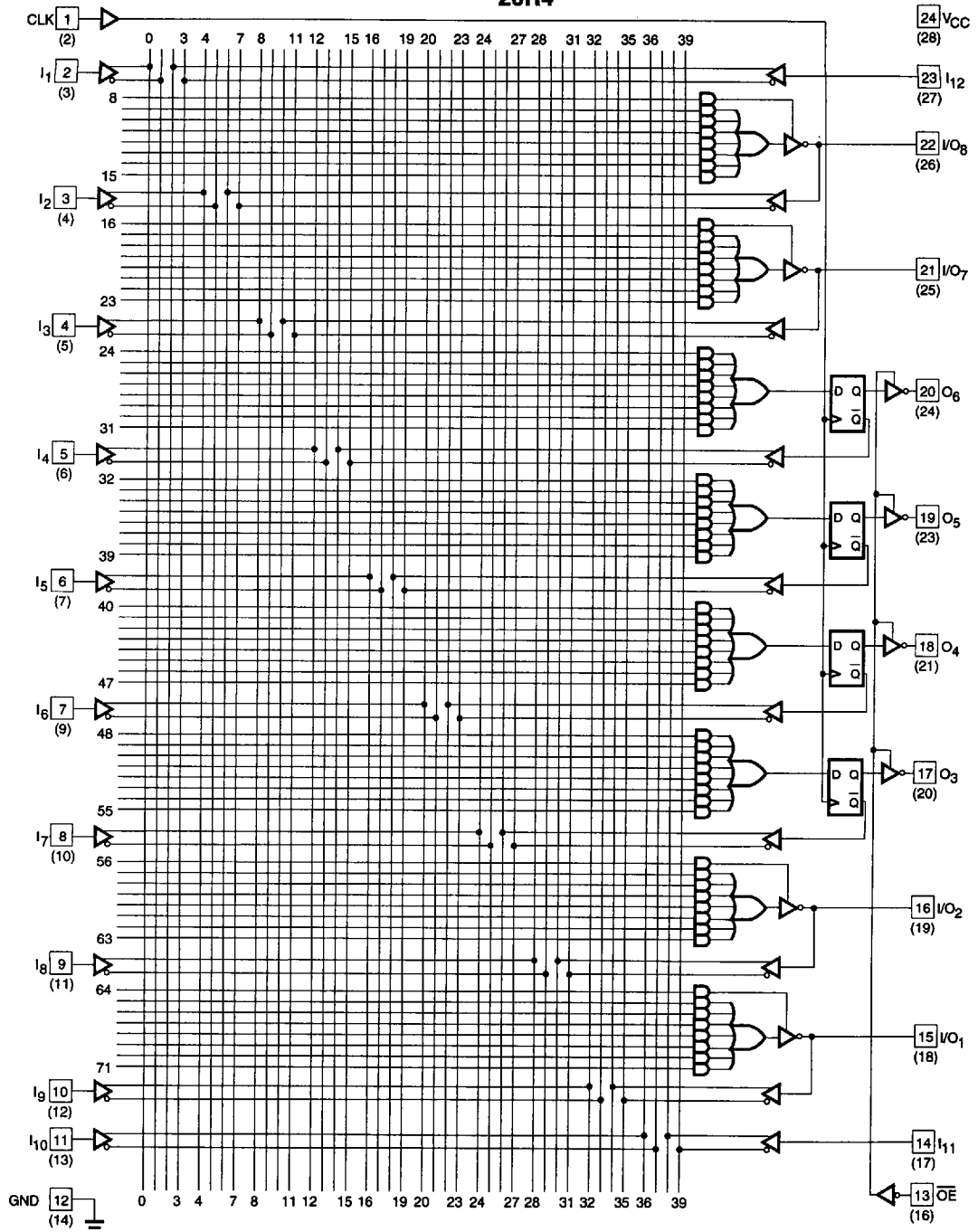
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0257526 0036742 693

# LOGIC DIAGRAM

## DIP (PLCC) Pinouts

### 20R4



## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Storage Temperature                    | -65°C to +150°C            |
| Ambient Temperature with Power Applied | -55°C to +125°C            |
| Supply Voltage with Respect to Ground  | -0.5 V to +7.0 V           |
| DC Input Voltage                       | -1.2 V to $V_{CC} + 0.5$ V |
| DC Output or I/O Pin Voltage           | -0.5 V to $V_{CC} + 0.5$ V |
| Static Discharge Voltage               | 2001 V                     |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

|  |                       |                  |
|--|-----------------------|------------------|
| Ambient Temperature ( $T_A$ )                      | Operating in Free Air | 0°C to 75°C      |
| Supply Voltage ( $V_{CC}$ ) with Respect to Ground |                       | 4.75 V to 5.25 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Max  | Unit    |
|------------------|---------------------------------------|--|-----|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$          | 2.4 |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$            |     | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)                      | 2.0 |      | V       |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)                       |     | 0.8  | V       |
| $V_i$            | Input Clamp Voltage                   | $I_{IN} = -18$ mA, $V_{CC} = \text{Min}$   |     | -1.2 | V       |
| $I_{IH}$         | Input HIGH Current                    | $V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | 25   | $\mu$ A |
| $I_{IL}$         | Input LOW Current                     | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | -250 | $\mu$ A |
| $I_i$            | Maximum Input Current                 | $V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$  |     | 1    | mA      |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | 100  | $\mu$ A |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | -100 | $\mu$ A |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)                                  | -30 | -130 | mA      |
| $I_{CC}$         | Supply Current                        | $V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA)<br>$V_{CC} = \text{Max}$          |     | 210  | mA      |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions  | Typ | Unit |
|------------------|-----------------------|--|-----|------|
| C <sub>IN</sub>  | Input Capacitance     | CLK, $\overline{OE}$   | 8   | pF   |
|                  |                       | I <sub>1</sub> – I <sub>12</sub>                               |     |      |
| C <sub>OUT</sub> | Output Capacitance    | V <sub>IN</sub> = 2.0 V  | 5   |      |
|                  |                       | V <sub>OUT</sub> = 2.0 V                                       |     |      |
|                  |                       | V <sub>CC</sub> = 5.0 V<br>T <sub>A</sub> = +25°C<br>f = 1 MHz |     |      |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol   | Parameter Description                              | Min (Note 3)     | Max                                   | Unit                                   |     |     |
|--------------------|--|------------------|---------------------------------------|--|-----|-----|
| t <sub>PD</sub>    | Input or Feedback to Combinatorial Output          | 20L8, 20R6, 20R4 | 1                                     | 5                                      | ns  |     |
| t <sub>S</sub>     | Setup Time from Input or Feedback to Clock         | 20R8, 20R6, 20R4 | 4.5                                   |  | ns  |     |
| t <sub>H</sub>     | Hold Time  |                  | 0                                     |  | ns  |     |
| t <sub>CO</sub>    | Clock to Output                                    |                  | 1                                     | 4                                      | ns  |     |
| t <sub>SKEWR</sub> | Skew Between Registered Outputs (Note 4)           |                  |                                       | 1                                      | ns  |     |
| t <sub>WL</sub>    | Clock Width  |                  | LOW                                   | 4                                      |     | ns  |
| t <sub>WH</sub>    |  |                  | HIGH                                  | 4                                      |     | ns  |
| f <sub>MAX</sub>   | Maximum Frequency (Notes 5 and 6)                  |                  | External Feedback                     | 1/(t <sub>S</sub> + t <sub>CO</sub> )  | 117 | MHz |
|                    |  |                  | Internal Feedback (f <sub>CNT</sub> ) | 1/(t <sub>S</sub> + t <sub>CF</sub> )  | 125 | MHz |
|                    |  |                  | No Feedback                           | 1/(t <sub>WH</sub> + t <sub>WL</sub> ) | 125 | MHz |
| t <sub>PZX</sub>   | $\overline{OE}$ to Output Enable                   |                  |                                       | 1                                      | 6.5 | ns  |
| t <sub>PXZ</sub>   | $\overline{OE}$ to Output Disable                  |                  | 1                                     | 5                                      | ns  |     |
| t <sub>EA</sub>    | Input to Output Enable Using Product Term Control  | 20L8, 20R6,      | 2                                     | 6.5                                    | ns  |     |
| t <sub>ER</sub>    | Input to Output Disable Using Product Term Control | 20R4             | 2                                     | 5                                      | ns  |     |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. Output delay minimums for t<sub>PD</sub>, t<sub>CO</sub>, t<sub>PZX</sub>, t<sub>EA</sub> and t<sub>ER</sub> are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.
4. Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.
5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.
6. t<sub>CF</sub> is a calculated value and is not guaranteed. t<sub>CF</sub> can be found using the following equation:  
t<sub>CF</sub> = 1/f<sub>MAX</sub> (internal feedback) – t<sub>S</sub>.

## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Storage Temperature                    | -65°C to +150°C            |
| Ambient Temperature with Power Applied | -55°C to +125°C            |
| Supply Voltage with Respect to Ground  | -0.5 V to +7.0 V           |
| DC Input Voltage                       | -1.2 V to $V_{CC} + 0.5$ V |
| DC Output or I/O Pin Voltage           | -0.5 V to $V_{CC} + 0.5$ V |
| Static Discharge Voltage               | 2001 V                     |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

|                               |                        |                    |
|-------------------------------|------------------------|--------------------|
| Ambient Temperature ( $T_A$ ) | Operating in Free Air  | 0°C to +75°C       |
| Supply Voltage ( $V_{CC}$ )   | With Respect to Ground | +4.75 V to +5.25 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Max  | Unit    |
|------------------|---------------------------------------|--|-----|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$          | 2.4 |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$            |     | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)                      | 2.0 |      | V       |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)                       |     | 0.8  | V       |
| $V_I$            | Input Clamp Voltage                   | $I_{IN} = -18$ mA, $V_{CC} = \text{Min}$   |     | -1.2 | V       |
| $I_{IH}$         | Input HIGH Current                    | $V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | 25   | $\mu$ A |
| $I_{IL}$         | Input LOW Current                     | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | -250 | $\mu$ A |
| $I_I$            | Maximum Input Current                 | $V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$  |     | 1    | mA      |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | 100  | $\mu$ A |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | -100 | $\mu$ A |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)                                  | -30 | -130 | mA      |
| $I_{CC}$         | Supply Current                        | $V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA)<br>$V_{CC} = \text{Max}$          |     | 210  | mA      |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions          |  | Typ | Unit |
|------------------|-----------------------|--------------------------|--|-----|------|
| C <sub>IN</sub>  | Input Capacitance     | V <sub>IN</sub> = 2.0 V  | V <sub>CC</sub> = 5.0 V<br>T <sub>A</sub> = +25°C<br>f = 1 MHz | 7   | pF   |
| C <sub>OUT</sub> | Output Capacitance    | V <sub>OUT</sub> = 2.0 V |  | 8   |      |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description                              |                                       |  | Min (Note 3)        | Max | Unit |     |
|------------------|--|---------------------------------------|--|---------------------|-----|------|-----|
| t <sub>PD</sub>  | Input or Feedback to Combinatorial Output          |                                       |  | 20L8, 20R6,         | 3   | 7.5  | ns  |
|                  |  | 1 Output Switching                    |  | 20R4                | 3   | 7    |     |
| t <sub>S</sub>   | Setup Time from Input or Feedback to Clock         |                                       |  | 20R8, 20R6,<br>20R4 | 7   |      | ns  |
| t <sub>H</sub>   | Hold Time  |                                       |  |                     | 0   |      | ns  |
| t <sub>CO</sub>  | Clock to Output                                    |                                       |  |                     | 1   | 6.5  | ns  |
| t <sub>SK</sub>  | Skew Between Registered Outputs (Note 4)           |                                       |  |                     |     | 1    | ns  |
| t <sub>WL</sub>  | Clock Width  | LOW                                   |  |                     | 5   |      | ns  |
|                  |  | HIGH                                  |  |                     | 5   |      | ns  |
| f <sub>MAX</sub> | Maximum Frequency (Notes 5 and 6)                  | External Feedback                     | 1/(t <sub>S</sub> + t <sub>CO</sub> )  |                     | 74  |      | MHz |
|                  |  | Internal Feedback (f <sub>CNT</sub> ) | 1/(t <sub>S</sub> + t <sub>CF</sub> )  |                     | 100 |      | MHz |
|                  |  | No Feedback                           | 1/(t <sub>WH</sub> + t <sub>WL</sub> ) |                     | 100 |      | MHz |
| t <sub>PZX</sub> | $\overline{OE}$ to Output Enable                   |                                       |  |                     | 1   | 8    | ns  |
| t <sub>PXZ</sub> | $\overline{OE}$ to Output Disable                  |                                       |  | 1                   | 8   | ns   |     |
| t <sub>EA</sub>  | Input to Output Enable Using Product Term Control  |                                       |  | 20L8, 20R6,         | 3   | 10   | ns  |
| t <sub>ER</sub>  | Input to Output Disable Using Product Term Control |                                       |  | 20R4                | 3   | 10   | ns  |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. Output delay minimums for t<sub>PD</sub>, t<sub>CO</sub>, t<sub>PZX</sub>, t<sub>PXZ</sub>, t<sub>EA</sub> and t<sub>ER</sub> are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.
4. Skew is measured with all outputs switching in the same direction.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where the frequency may be affected.
6. t<sub>CF</sub> is a calculated value and is not guaranteed. t<sub>CF</sub> can be found using the following equation:  
t<sub>CF</sub> = 1/f<sub>MAX</sub> (internal feedback) - t<sub>S</sub>.

## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Storage Temperature                    | -65°C to +150°C            |
| Ambient Temperature with Power Applied | -55°C to +125°C            |
| Supply Voltage with Respect to Ground  | -0.5 V to +7.0 V           |
| DC Input Voltage                       | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output or I/O Pin Voltage           | -0.5 V to $V_{CC}$ Max     |
| DC Input Current                       | -30 mA to 5 mA             |
| Static Discharge Voltage               | 2001 V                     |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

|  |                       |                    |
|--|-----------------------|--------------------|
| Ambient Temperature ( $T_A$ )                      | Operating in Free Air | 0°C to +75°C       |
| Supply Voltage ( $V_{CC}$ ) with Respect to Ground |                       | +4.75 V to +5.25 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Max  | Unit    |
|------------------|---------------------------------------|--|-----|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$          | 2.4 |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$            |     | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)                      | 2.0 |      | V       |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)                       |     | 0.8  | V       |
| $V_I$            | Input Clamp Voltage                   | $I_{IN} = -18$ mA, $V_{CC} = \text{Min}$   |     | -1.5 | V       |
| $I_{IH}$         | Input HIGH Current                    | $V_{IN} = 2.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | 25   | $\mu$ A |
| $I_{IL}$         | Input LOW Current                     | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | -250 | $\mu$ A |
| $I_I$            | Maximum Input Current                 | $V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$  |     | 100  | $\mu$ A |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 2.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | 100  | $\mu$ A |
| $I_{OLZ}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | -100 | $\mu$ A |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)                                  | -30 | -130 | mA      |
| $I_{CC}$         | Supply Current                        | $V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA)<br>$V_{CC} = \text{Max}$          |     | 210  | mA      |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OLZ}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.



## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Description | Test Conditions          |   | Typ | Unit |
|------------------|-----------------------|--------------------------|---|-----|------|
| C <sub>IN</sub>  | Input Capacitance     | V <sub>IN</sub> = 2.0 V  | V <sub>CC</sub> = 5.0 V<br>T <sub>A</sub> = 25°C<br>f = 1 MHz | 7   | pF   |
| C <sub>OUT</sub> | Output Capacitance    | V <sub>OUT</sub> = 2.0 V |   | 8   |      |

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description                              |                                       | Min (Note 3)     | Max                                    | Unit |    |     |
|------------------|--|---------------------------------------|------------------|--|------|----|-----|
| t <sub>PD</sub>  | Input or Feedback to Combinatorial Output          |                                       | 20L8, 20R6, 20R4 | 3                                      | 10   | ns |     |
| t <sub>S</sub>   | Setup Time from Input or Feedback to Clock         |                                       | 20R8, 20R6, 20R4 | 10                                     |      | ns |     |
| t <sub>H</sub>   | Hold Time  |                                       |                  | 0                                      |      | ns |     |
| t <sub>CO</sub>  | Clock to Output                                    |                                       |                  | 3                                      | 8    | ns |     |
| t <sub>WL</sub>  | Clock Width  | LOW                                   |                  | 7                                      |      | ns |     |
| t <sub>WH</sub>  |  | HIGH                                  |                  | 7                                      |      | ns |     |
| f <sub>MAX</sub> | Maximum Frequency (Notes 4 and 5)                  | External Feedback                     |                  | 1/(t <sub>S</sub> + t <sub>CO</sub> )  | 55.5 |    | MHz |
|                  |  | Internal Feedback (t <sub>CNT</sub> ) |                  | 1/(t <sub>S</sub> + t <sub>CF</sub> )  | 58.8 |    | MHz |
|                  |  | No Feedback                           |                  | 1/(t <sub>WH</sub> + t <sub>WL</sub> ) | 71.4 |    | MHz |
| t <sub>PZX</sub> | $\overline{OE}$ to Output Enable                   |                                       |                  |  | 2    | 10 | ns  |
| t <sub>PXZ</sub> | $\overline{OE}$ to Output Disable                  |                                       |                  |  | 2    | 10 | ns  |
| t <sub>EA</sub>  | Input to Output Enable Using Product Term Control  |                                       | 20L8, 20R6, 20R4 | 3                                      | 10   | ns |     |
| t <sub>ER</sub>  | Input to Output Disable Using Product Term Control |                                       |                  | 3                                      | 10   | ns |     |

**Notes:**

2. See Switching Test Circuit for test conditions.
3. Output delay minimums for t<sub>PD</sub>, t<sub>CO</sub>, t<sub>PZX</sub>, t<sub>PXZ</sub>, t<sub>EA</sub> and t<sub>ER</sub> are defined under best case conditions. Future process improvements may alter these values; therefore, minimum values are recommended for simulation purposes only.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.
5. t<sub>CF</sub> is a calculated value and is not guaranteed. t<sub>CF</sub> can be found using the following equation:  
t<sub>CF</sub> = 1/f<sub>MAX</sub> (internal feedback) – t<sub>S</sub>.

## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Storage Temperature                    | −65°C to +150°C            |
| Ambient Temperature with Power Applied | −55°C to +125°C            |
| Supply Voltage with Respect to Ground  | −0.5 V to +7.0 V           |
| DC Input Voltage                       | −1.5 V to $V_{CC} + 0.5$ V |
| DC Output or I/O Pin Voltage           | −0.5 V to $V_{CC} + 0.5$ V |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

|                               |                        |                    |
|-------------------------------|------------------------|--------------------|
| Ambient Temperature ( $T_A$ ) | Operating in Free Air  | 0°C to +75°C       |
| Supply Voltage ( $V_{CC}$ )   | with Respect to Ground | +4.75 V to +5.25 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Max  | Unit          |
|------------------|---------------------------------------|--|-----|------|---------------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$          | 2.4 |      | V             |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$            |     | 0.5  | V             |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)                      | 2.0 |      | V             |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)                       |     | 0.8  | V             |
| $V_I$            | Input Clamp Voltage                   | $I_{IN} = -18$ mA, $V_{CC} = \text{Min}$   |     | −1.5 | V             |
| $I_{IH}$         | Input HIGH Current                    | $V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | 25   | $\mu\text{A}$ |
| $I_{IL}$         | Input LOW Current                     | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | −250 | $\mu\text{A}$ |
| $I_I$            | Maximum Input Current                 | $V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$  |     | 100  | $\mu\text{A}$ |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | 100  | $\mu\text{A}$ |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | −100 | $\mu\text{A}$ |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)                                  | −30 | −130 | mA            |
| $I_{CC}$         | Supply Current                        | $V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA)<br>$V_{CC} = \text{Max}$          |     | 210  | mA            |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)**

| Parameter Symbol | Parameter Description                              |                   | Min                                    | Max | Unit |     |
|------------------|--|-------------------|--|-----|------|-----|
| t <sub>PD</sub>  | Input or Feedback to Combinatorial Output          |                   |  | 15  | ns   |     |
| t <sub>S</sub>   | Setup Time from Input or Feedback to Clock         |                   | 15                                     |     | ns   |     |
| t <sub>H</sub>   | Hold Time  |                   | 0                                      |     | ns   |     |
| t <sub>CO</sub>  | Clock to Output or Feedback                        |                   |  | 12  | ns   |     |
| t <sub>WL</sub>  | Clock Width  | LOW               | 10                                     |     | ns   |     |
| t <sub>WH</sub>  |  | HIGH              | 12                                     |     | ns   |     |
| f <sub>MAX</sub> | Maximum Frequency (Note 2)                         | External Feedback | 1/(t <sub>S</sub> + t <sub>CO</sub> )  |     | 37   | MHz |
|                  |  | No Feedback       | 1/(t <sub>WH</sub> + t <sub>WL</sub> ) |     | 45   | MHz |
| t <sub>PZX</sub> | $\overline{OE}$ to Output Enable                   |                   | 15                                     | ns  |      |     |
| t <sub>PXZ</sub> | $\overline{OE}$ to Output Disable                  |                   |  | 12  | ns   |     |
| t <sub>EA</sub>  | Input to Output Enable Using Product Term Control  |                   |  | 18  | ns   |     |
| t <sub>ER</sub>  | Input to Output Disable Using Product Term Control |                   |  | 15  | ns   |     |

**Notes:**

1. See Switching Test Circuit for test conditions.
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Storage Temperature                    | -65°C to +150°C            |
| Ambient Temperature with Power Applied | -55°C to +125°C            |
| Supply Voltage with Respect to Ground  | -0.5 V to +7.0 V           |
| DC Input Voltage                       | -1.5 V to $V_{CC} + 0.5$ V |
| DC Output or I/O Pin Voltage           | -0.5 V to $V_{CC} + 0.5$ V |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

|  |                       |                    |
|--|-----------------------|--------------------|
| Ambient Temperature ( $T_A$ )                      | Operating in Free Air | 0°C to +75°C       |
| Supply Voltage ( $V_{CC}$ ) with Respect to Ground |                       | +4.75 V to +5.25 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Max  | Unit    |
|------------------|---------------------------------------|--|-----|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$          | 2.4 |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$            |     | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)                      | 2.0 |      | V       |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)                       |     | 0.8  | V       |
| $V_I$            | Input Clamp Voltage                   | $I_{IN} = -18$ mA, $V_{CC} = \text{Min}$   |     | -1.5 | V       |
| $I_{IH}$         | Input HIGH Current                    | $V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | 25   | $\mu$ A |
| $I_{IL}$         | Input LOW Current                     | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | -250 | $\mu$ A |
| $I_I$            | Maximum Input Current                 | $V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$  |     | 100  | $\mu$ A |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | 100  | $\mu$ A |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | -100 | $\mu$ A |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)                                  | -30 | -130 | mA      |
| $I_{CC}$         | Supply Current                        | $V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA)<br>$V_{CC} = \text{Max}$          |     | 105  | mA      |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)**

| Parameter Symbol | Parameter Description                              |                                       | Min                                    | Max | Unit |
|------------------|--|---------------------------------------|--|-----|------|
| t <sub>PD</sub>  | Input or Feedback to Combinatorial Output          |                                       |  | 25  | ns   |
| t <sub>S</sub>   | Setup Time from Input or Feedback to Clock         |                                       | 25                                     |     | ns   |
| t <sub>H</sub>   | Hold Time  |                                       | 0                                      |     | ns   |
| t <sub>CO</sub>  | Clock to Output                                    |                                       |  | 15  | ns   |
| t <sub>WL</sub>  | Clock Width  | LOW                                   | 15                                     |     | ns   |
| t <sub>WH</sub>  |  | HIGH                                  | 15                                     |     | ns   |
| f <sub>MAX</sub> | Maximum Frequency (Notes 3 and 4)                  | External Feedback                     | 1/(t <sub>S</sub> + t <sub>CO</sub> )  |     | MHz  |
|                  |  | Internal Feedback (f <sub>CNT</sub> ) | 1/(t <sub>S</sub> + t <sub>CF</sub> )  |     | MHz  |
|                  |  | No Feedback                           | 1/(t <sub>WH</sub> + t <sub>WL</sub> ) |     | MHz  |
| t <sub>PZX</sub> | $\overline{OE}$ to Output Enable                   |                                       |  | 20  | ns   |
| t <sub>PXZ</sub> | $\overline{OE}$ to Output Disable                  |                                       |  | 20  | ns   |
| t <sub>EA</sub>  | Input to Output Enable Using Product Term Control  |                                       |  | 25  | ns   |
| t <sub>ER</sub>  | Input to Output Disable Using Product Term Control |                                       |  | 25  | ns   |

**Notes:**

1. See Switching Test Circuit for test conditions.
2. Calculated from measured f<sub>MAX</sub> internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. t<sub>CF</sub> is a calculated value and is not guaranteed. t<sub>CF</sub> can be found using the following equation:  
 $t_{CF} = 1/f_{MAX} \text{ (internal feedback)} - t_S$

## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Storage Temperature                    | -65°C to +150°C            |
| Ambient Temperature with Power Applied | -55°C to +125°C            |
| Supply Voltage with Respect to Ground  | -0.5 V to +7.0 V           |
| DC Input Voltage                       | -1.5 V to $V_{CC} + 0.5$ V |
| DC Output or I/O Pin Voltage           | -0.5 V to $V_{CC} + 0.5$ V |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## OPERATING RANGES

### Commercial (C) Devices

|  |                       |                    |
|--|-----------------------|--------------------|
| Ambient Temperature ( $T_A$ )                      | Operating in Free Air | 0°C to +75°C       |
| Supply Voltage ( $V_{CC}$ ) with Respect to Ground |                       | +4.75 V to +5.25 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description                 | Test Conditions  | Min | Max  | Unit    |
|------------------|---------------------------------------|--|-----|------|---------|
| $V_{OH}$         | Output HIGH Voltage                   | $I_{OH} = -3.2$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$          | 2.4 |      | V       |
| $V_{OL}$         | Output LOW Voltage                    | $I_{OL} = 24$ mA $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{CC} = \text{Min}$            |     | 0.5  | V       |
| $V_{IH}$         | Input HIGH Voltage                    | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)                      | 2.0 |      | V       |
| $V_{IL}$         | Input LOW Voltage                     | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)                       |     | 0.8  | V       |
| $V_I$            | Input Clamp Voltage                   | $I_{IN} = -18$ mA, $V_{CC} = \text{Min}$   |     | -1.5 | V       |
| $I_{IH}$         | Input HIGH Current                    | $V_{IN} = 2.7$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | 25   | $\mu$ A |
| $I_{IL}$         | Input LOW Current                     | $V_{IN} = 0.4$ V, $V_{CC} = \text{Max}$ (Note 2)                                   |     | -250 | $\mu$ A |
| $I_I$            | Maximum Input Current                 | $V_{IN} = 5.5$ V, $V_{CC} = \text{Max}$  |     | 100  | $\mu$ A |
| $I_{OZH}$        | Off-State Output Leakage Current HIGH | $V_{OUT} = 2.7$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | 100  | $\mu$ A |
| $I_{OZL}$        | Off-State Output Leakage Current LOW  | $V_{OUT} = 0.4$ V, $V_{CC} = \text{Max}$<br>$V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2) |     | -100 | $\mu$ A |
| $I_{SC}$         | Output Short-Circuit Current          | $V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)                                  | -30 | -130 | mA      |
| $I_{CC}$         | Supply Current                        | $V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA)<br>$V_{CC} = \text{Max}$          |     | 210  | mA      |

### Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
- Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

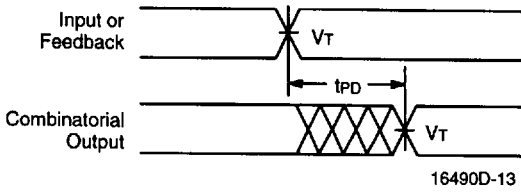
**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)**

| Parameter Symbol | Parameter Description                              |                          | Min              | Max          | Unit |     |
|------------------|--|--------------------------|------------------|--------------|------|-----|
| tpD              | Input or Feedback to Combinatorial Output          |                          | 20L8, 20R6, 20R4 | 25           | ns   |     |
| ts               | Setup Time from Input or Feedback to Clock         |                          | 20R8, 20R6, 20R4 | 25           | ns   |     |
| tH               | Hold Time  |                          |                  | 0            | ns   |     |
| tCO              | Clock to Output                                    |                          |                  | 15           | ns   |     |
| tWL              | Clock Width  | LOW                      |                  | 15           | ns   |     |
| tWH              |  | HIGH                     |                  | 15           | ns   |     |
| fMAX             | Maximum Frequency (Notes 3 and 4)                  | External Feedback        |                  | 1/(ts + tco) | 25   | MHz |
|                  |  | Internal Feedback (fcNT) |                  | 1/(ts + tCF) | 28.5 | MHz |
|                  |  | No Feedback              | 1/(tWH + tWL)    | 33           | MHz  |     |
| tpZX             | $\overline{OE}$ to Output Enable                   |                          |                  | 20           | ns   |     |
| tpXZ             | $\overline{OE}$ to Output Disable                  |                          |                  | 20           | ns   |     |
| tEA              | Input to Output Enable Using Product Term Control  |                          | 20L8, 20R6,      | 25           | ns   |     |
| tER              | Input to Output Disable Using Product Term Control |                          | 20R4             | 25           | ns   |     |

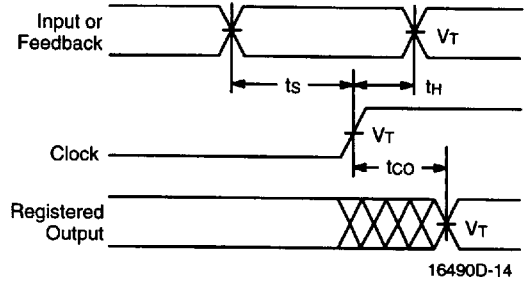
**Notes:**

1. See Switching Test Circuit for test conditions.
2. Calculated from measured fMAX internal.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. tCF is a calculated value and is not guaranteed. tCF can be found using the following equation:  
 $t_{CF} = 1/f_{MAX} \text{ (internal feedback)} - t_s$

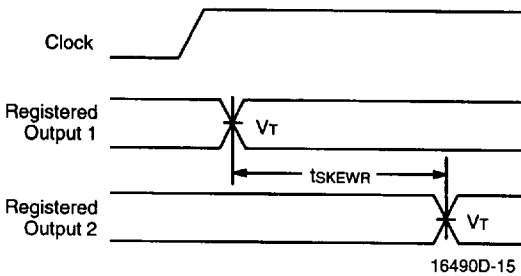
**SWITCHING WAVEFORMS**



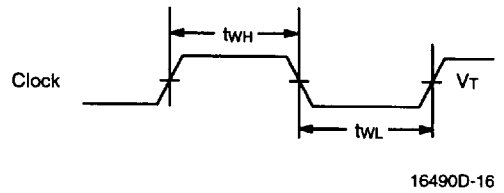
**Combinatorial Output**



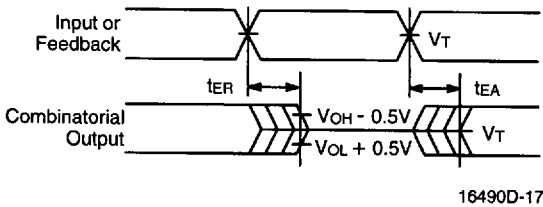
**Registered Output**



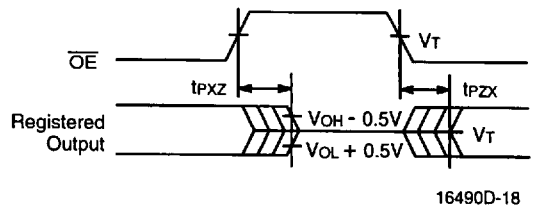
**Registered Output Skew**



**Clock Width**



**Input to Output Disable/Enable**



**OE to Output Disable/Enable**

**Notes:**

1.  $V_T = 1.5\text{ V}$
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2 ns – 3 ns typical

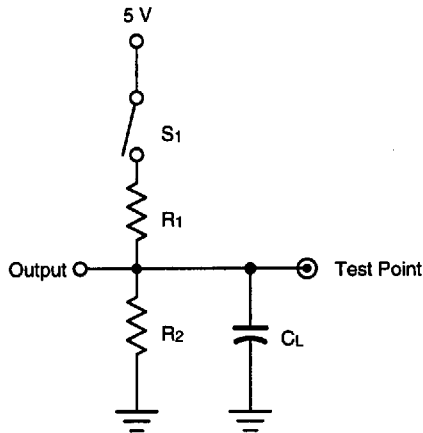


## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|----------------------------------|---|
|          | Must be Steady                   | Will be Steady                            |
|          | May Change from H to L           | Will be Changing from H to L              |
|          | May Change from L to H           | Will be Changing from L to H              |
|          | Don't Care, Any Change Permitted | Changing, State Unknown                   |
|          | Does Not Apply                   | Center Line is High-Impedance "Off" State |

KS000010-PAL

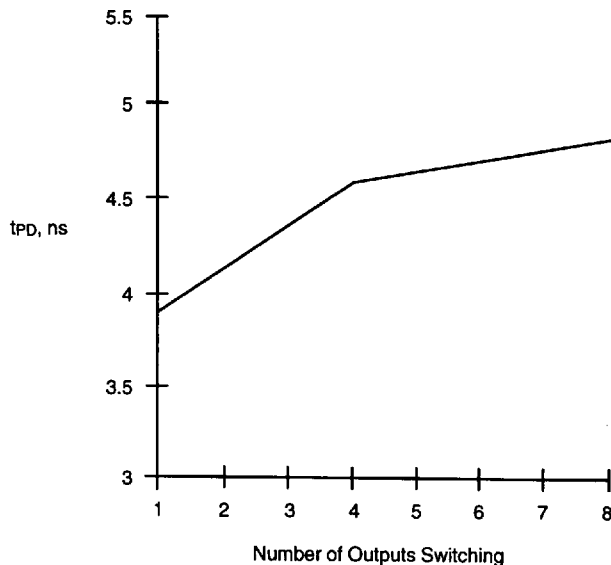
## SWITCHING TEST CIRCUIT



16490D-19

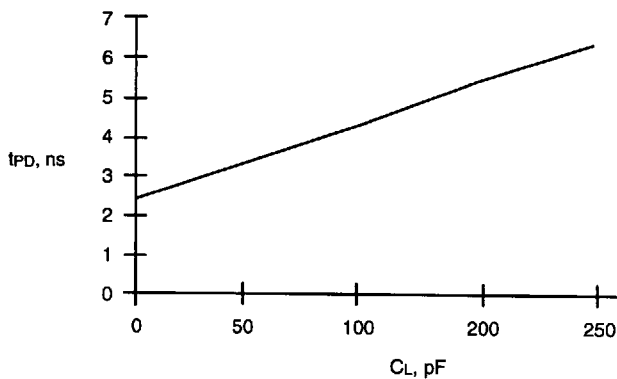
| Specification                      | S <sub>1</sub>               | C <sub>L</sub> | Commercial     |  | Military       |                | Measured Output Value |
|------------------------------------|------------------------------|----------------|----------------|--|----------------|----------------|-----------------------|
|                                    |                              |                | R <sub>1</sub> | R <sub>2</sub>   | R <sub>1</sub> | R <sub>2</sub> |                       |
| t <sub>PD</sub> , t <sub>CO</sub>  | Closed                       | 50 pF          | 200 Ω          | For -5:<br>200 Ω   | 390 Ω          | 750 Ω          | 1.5 V                 |
| t <sub>PZX</sub> , t <sub>EA</sub> | Z → H: Open<br>Z → L: Closed |                |                | For rest<br>390 Ω  |                |                | 1.5 V                 |
| t <sub>PXZ</sub> , t <sub>ER</sub> | H → Z: Open<br>L → Z: Closed | 5 pF           |                | H → Z: V <sub>OH</sub> - 0.5 V<br>L → Z: V <sub>OL</sub> + 0.5 V |                |                |                       |

**MEASURED SWITCHING CHARACTERISTICS FOR THE PAL20R8-5**



**$t_{PD}$  vs. Number of Outputs Switching**  
 $V_{CC} = 4.75 \text{ V}$ ,  $T_A = 75^\circ\text{C}$  (Note 1)

16490D-20



**$t_{PD}$  vs. Load Capacitance**  
 $V_{CC} = 5.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

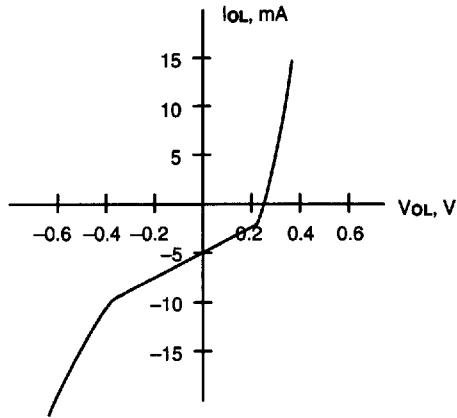
16490D-21

**Note:**

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where  $t_{PD}$  may be affected.

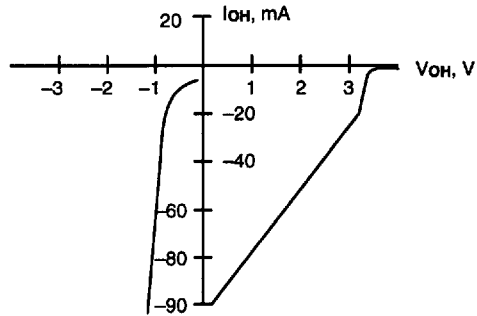
**CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS FOR THE PAL20R8-5**

$V_{CC} = 5.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$



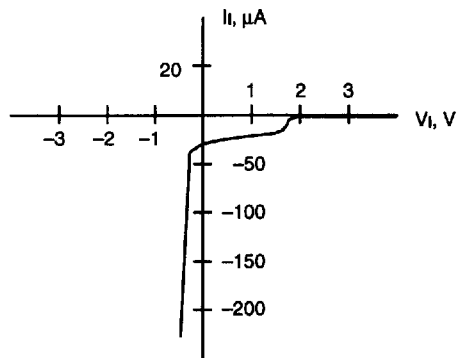
**Output, LOW**

16490D-22



**Output, HIGH**

16490D-23



**Input**

16490D-24