ELPIDA

PRELIMINARY DATA SHEET

128M bits DDR Mobile RAM™

EDK1216CFBJ (8M words × 16 bits)

Specifications

- Density: 128M bits
- Organization
  - 2M words × 16 bits × 4 banks
- Package: 60-ball FBGA
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply: VDD, VDDQ = 1.7V to 1.95V
- Clock frequency: 133MHz (max.)
- 1KB page size
  - Row address: A0 to A11
  - Column address: A0 to A8
- Four internal banks for concurrent operation
- Interface: LVCMOS
- Burst lengths (BL): 2, 4, 8, 16
- Burst type (BT):
  - Sequential (2, 4, 8, 16)
  - Interleave (2, 4, 8, 16)
- /CAS Latency (CL): 3
- Precharge: auto precharge option for each burst access
- Driver strength: normal, 1/2, 1/4, 1/8
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 4096 cycles/64ms
  - Average refresh period: 15.6µs
- Operating ambient temperature range
  - TA =–25°C to +85°C

Features

- Low power consumption
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Double-data-rate architecture; two data transfers per one clock cycle
- Bi-directional data strobe (DQS) is transmitted /received with data for capturing data at the receiver.
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- Commands entered on each positive CK edge: data and data mask referenced to both edges of DQS
- Burst termination by burst stop command and Precharge command

Pin Configurations

/xxx indicates active low signal.

60-ball FBGA

	1	2	3	4	5	6	7	8	9	10
A	VSS	DQ15	VSSQ					VDDQ	DQ0	VDD
B	VDDQ	DQ13	DQ14					DQ1	DQ2	VSSQ
C	VSSQ	DQ11	DQ12					DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10					DQ5	DQ6	VSSQ
E	VSSQ	UDQS	DQ8					DQ7	LDQS	VDDQ
F	VSS	UDM	NC					NC	LDM	VDD
G	CKE	CK	/CK					/WE	/CAS	/RAS
H	A9	A11	NC					/CS	BA0	BA1
J	A6	A7	A8					A10	A0	A1
K	VSS	A4	A5					A2	A3	VDD

(Top View)

A0 to A11	Address input
BA0, BA1	Bank select address
DQ0 to DQ15	Data-input/output
UDQS, LDQS	Input and output data strobe
/CS	Chip select
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
UDM, LDM	Write data mask
CK	Clock input
/CK	Differential clock input
CKE	Clock enable
VDD	Power for internal circuit
VSS	Ground for internal circuit
VDDQ	Power for DQ circuit
VSSQ	Ground for DQ circuit
NC	No connection

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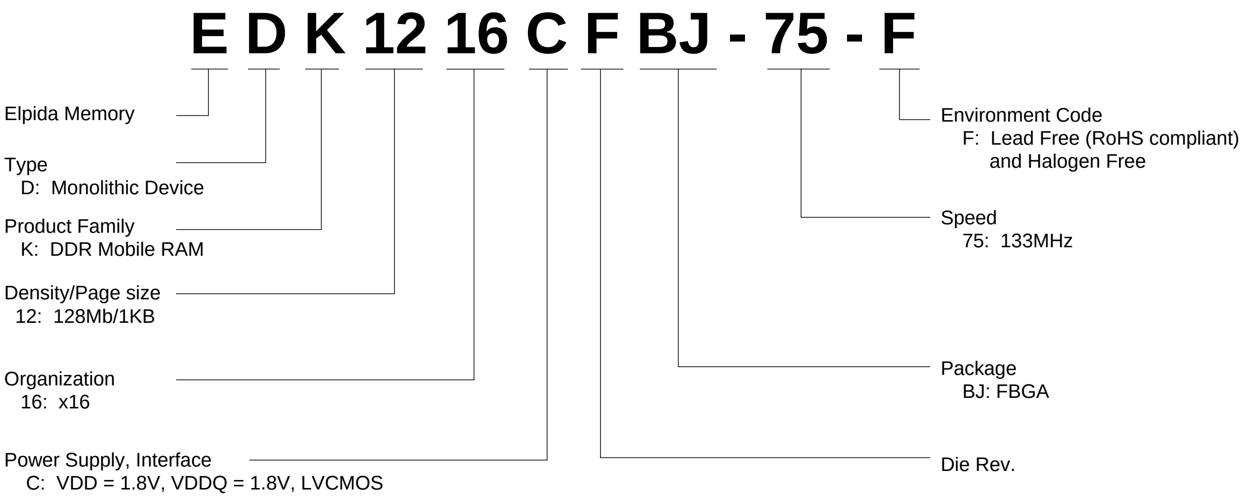
Ordering Information

Part number	Organization (words × bits)	Internal banks	Clock frequency MHz (max.)	Data rate Mbps (max.)	/CAS latency	Package
EDK1216CFBJ-75-F	8M × 16	4	133	266	3	60-ball FBGA

Part Number



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Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 200 μs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +2.45	V	
Supply voltage relative to VSS	VDD	–0.5 to +2.45	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	1.0	W	
Operating ambient temperature	TA	–25 to +85	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (TA = –25°C to +85°C)

Parameter	Pins	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage		VDD, VDDQ	1.70	1.8	1.95	V	
		VSS, VSSQ	0	0	0	V	
DC input voltage level	CK, /CK	VIN (DC)	–0.3	—	VDDQ + 0.3	V	
AC Input differential cross point voltage		VIX	0.4 × VDDQ	0.5 × VDDQ	0.6 × VDDQ	V	5
DC input differential voltage		VID (DC)	0.4 × VDDQ	—	VDDQ + 0.6	V	4
AC input differential voltage		VID (AC)	0.6 × VDDQ	—	VDDQ + 0.6	V	4
DC input high voltage	DQ, DM, DQS, address, bank select address, command signals	VIHD (DC)	0.7× VDDQ	—	VDDQ + 0.3	V	1, 2
DC input low voltage		VILD (DC)	–0.3	—	0.3 × VDDQ	V	
AC input high voltage		VIHD (AC)	0.8× VDDQ	—	VDDQ + 0.3	V	
AC input low voltage		VILD (AC)	–0.3	—	0.2 × VDDQ	V	

Notes: 1. VIH (max.) = 2.45V (pulse width ≤ 5ns).
2. VIL (min.) = –0.5V (pulse width ≤ 5ns).
3. All voltage referred to VSS and VSSQ must be same potential.
4. VID (DC) and VID (AC) are the magnitude of the difference between the input level on CK and the input level on /CK.
5. The value of VIX is expected to be 0.5 × VDDQ and must track variations in the DC level of the same.

DC Characteristics 1 (TA = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current	IDD0		40	mA	tRC ≥ tRC (min.), CKE ≥ VIH (min.), tCK = tCK (min.) Address and Command input signals are changed one time during 2tCK. Data input signals are stable	
Standby current in power down	IDD2P		0.8	mA	CKE ≤ VIL (max.), tCK = tCK (min.)	
Standby current in power down (input signal stable)	IDD2PS		0.6	mA	CKE ≤ VIL (max.), tCK = ∞	
Standby current in non power down	IDD2N		4.0	mA	CKE ≥ VIH (min.), tCK = tCK (min.), /CS ≥ VIH (min.), Input signals are changed one time during 2tCK.	
Standby current in non power down (input signal stable)	IDD2NS		2.0	mA	CKE ≥ VIH (min.), tCK = ∞, Address and Command Input signals are stable. DQ and DQS are Don't care.	
Active standby current in power down	IDD3P		3.0	mA	CKE ≤ VIL (max.), tCK = tCK (min.)	
Active standby current in power down (input signal stable)	IDD3PS		2.0	mA	CKE ≤ VIL (max.), tCK = ∞	
Active standby current in non power down	IDD3N		10	mA	CKE ≥ VIH (min.), tCK = tCK (min.), /CS ≥ VIH (min.), Input signals are changed one time during 2tCK.	
Active standby current in non power down (input signal stable)	IDD3NS		7.0	mA	CKE ≥ VIH (min.), tCK = ∞, Address and Command Input signals are stable. DQ and DQS are Don't care.	
Burst operating current	IDD4		80	mA	Burst length = 4, tCK ≥ tCK (min.), IOUT = 0mA, One bank active, 50 % data changing each burst	1
Refresh current	IDD5		70	mA	tRFC ≥ tRFC (min.)	2

Advanced Data Retention Current

(TA = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)

Parameter	Symbol	Grade	typ.	max.	Unit	Condition	Notes
Advanced data retention current (Self-refresh current) PASR="000" (Full)	IDD6		—	140	µA	–25°C ≤ TA ≤ +45°C	
PASR="001" (2BK)			—	120	µA	CKE ≤ 0.2V	
PASR="010" (1BK)			—	110	µA		
PASR="000" (Full)	IDD6		—	210	µA	+45°C < TA ≤ +85°C	
PASR="001" (2BK)			—	160	µA	CKE ≤ 0.2V	
PASR="010" (1BK)			—	140	µA		

Notes: 1. IDD4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD4 is measured on condition that addresses are changed only one time during tCK (min.).

2. IDD5 is measured on condition that addresses are changed only one time during tCK (min.).

DC Characteristics 2 (TA = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–2.0	2.0	μA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	–1.5	1.5	μA	0 ≤ VOUT ≤ VDDQ, DQ = disable	
Output high voltage	VOH	0.9 × VDDQ	—	V	IOH = – 0.1mA	
Output low voltage	VOL	—	0.1 × VDDQ	V	IOL = 0.1 mA	

Pin Capacitance (TA = +25°C, VDD and VDDQ = 1.7V to 1.95V)

Parameter	Symbol	Pins	min.	typ.	max.	Unit	Notes
Input capacitance	CI1	CK, /CK	1.5	—	3.5	pF	1
	CI2	All other input-only pins	1.5	—	3.0	pF	1
Delta input capacitance	Cdi1	CK, /CK	—	—	0.25	pF	1
	Cdi2	All other input-only pins	—	—	0.5	pF	1
Input/output capacitance	CI/O	DQ, DM, DQS	2.0	—	4.5	pF	1, 2
Delta input/output capacitance	Cdio	DQ, DM, DQS	—	—	0.5	pF	1

Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VDDQ/2, ΔVOUT = 0.2V, TA = +25°C.

2. DOUT circuits are disabled.

AC Characteristics (TA = –25°C to +85°C, VDD and VDDQ = 1.7V to 1.95V, VSS and VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Notes
Clock cycle time	tCK	7.5	100	ns	
CK high-level width	tCH	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	tCK	
CK half period	tHP	min. (tCH, tCL)	—	tCK	
DQ output access time from CK, /CK	tAC	2.5	6.0	ns	2, 8
DQS-in cycle time	tDSC	0.9	1.1	tCK	
DQS output access time from CK, /CK	tDQSCK	2.5	6.0	ns	2, 8
DQ-out high-impedance time from CK, /CK	tHZ	—	6.0	ns	5, 8
DQ-out low-impedance time from CK, /CK	tLZ	1.0	—	ns	6, 8
DQS to DQ skew	tDQSQ	—	0.6	ns	3
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	ns	4
Data hold skew factor	tQHS	—	0.75	ns	
DQ and DM input setup time	tDS	0.8	—	ns	3
DQ and DM input hold time	tDH	0.8	—	ns	3
DQ and DM input pulse width	tDIPW	1.8	—	ns	
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
Write preamble setup time	tWPRES	0	—	ns	
Write preamble	tWPRE	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	tCK	7

Parameter	Symbol	min.	max.	Unit	Notes
Write command to first DQS latching transition	tDQSS	0.75	1.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	tCK	
DQS input high pulse width	tDQSH	0.4	0.6	tCK	
DQS input low pulse width	tDQSL	0.4	0.6	tCK	
Address and control input setup time	tIS	1.3	—	ns	3
Address and control input hold time	tIH	1.3	—	ns	3
Address and control input pulse width	tIPW	2.6	—	ns	3
Mode register set command cycle time	tMRD	2	—	tCK	
Active to Precharge command period	tRAS	45	120000	ns	
Active to Active/Auto refresh command period	tRC	75	—	ns	
Auto refresh to Active/Auto refresh command period	tRFC	97.5	—	ns	
Active to Read/Write delay	tRCD	22.5	—	ns	
Precharge to active command period	tRP	22.5	—	ns	
Active to active command period	tRRD	15	—	ns	
Column address to column address delay	tCCD	1	—	tCK	
Write recovery time	tWR	15	—	ns	
Autoprecharge write recovery and precharge time	tDAL	—	—		9
Self-Refresh Exit Period	tSREX	120	—	ns	
Internal Write to Read command delay	tWTR	1	—	tCK	
Refresh period	tREF	—	64	ms	

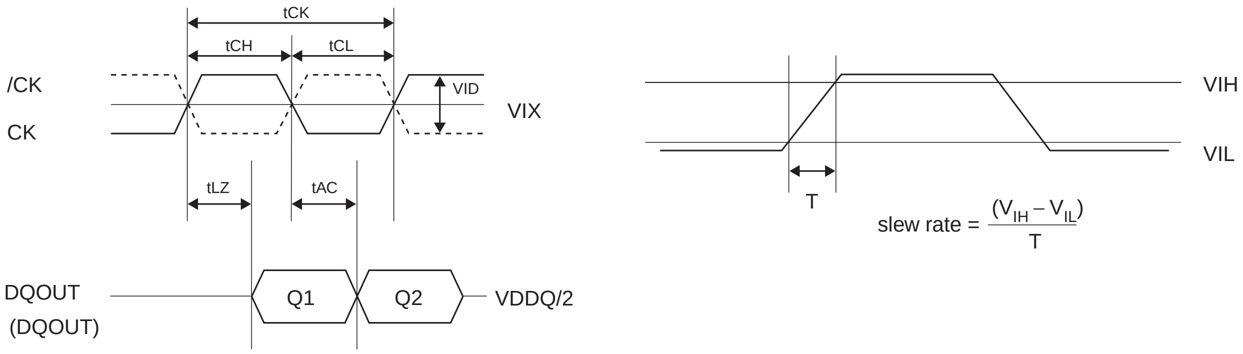
Notes:
1. On all AC measurements, we assume the test conditions shown in “Test conditions” and full driver strength is assumed for the output load, that is both A6 and A5 of EMRS is set to be “L”.
2. This parameter defines the signal transition delay from the cross point of CK and /CK. The signal transition is defined to occur when the signal level crossing VDDQ/2.
3. The timing reference level is VDDQ/2.
4. Output valid window is defined to be the period between two successive transition of data out signals. The signal transition is defined to occur when the signal level crossing VDDQ/2.
5. tHZ is defined as DOUT transition delay from low-Z to high-Z at the end of read burst operation. The timing reference is cross point of CK and /CK. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ is defined as DOUT transition delay from high-Z to low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. The transition from low-Z to high-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
8. tAC, tDQSCK, tHZ and tLZ are specified with 20pF bus loading condition.
9. Minimum 3 clocks of tDAL (= tWR + tRP) is required because it need minimum 2 clocks for tWR and minimum 1 clock for tRP.

   tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms above, if not already an integer, round to the next higher integer.

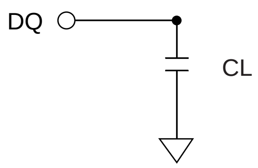
Test Conditions

Parameter	Symbol	Value	Unit	Note
Input high voltage	VIH (AC)	0.8 × VDDQ	V	1
Input low voltage	VIL (AC)	0.2 × VDDQ	V	1
Input differential voltage, CK and /CK inputs	VID (AC)	1.4	V	1
Input differential cross point voltage, CK and /CK inputs	VIX (AC)	VDDQ/2 with VDD=VDDQ	V	
Input signal slew rate	SLEW	1	V/ns	1
Output load	CL	20	pF	

Note: 1. VDD = VDDQ



Test Condition (Wave form and Timing Reference)



Output Load

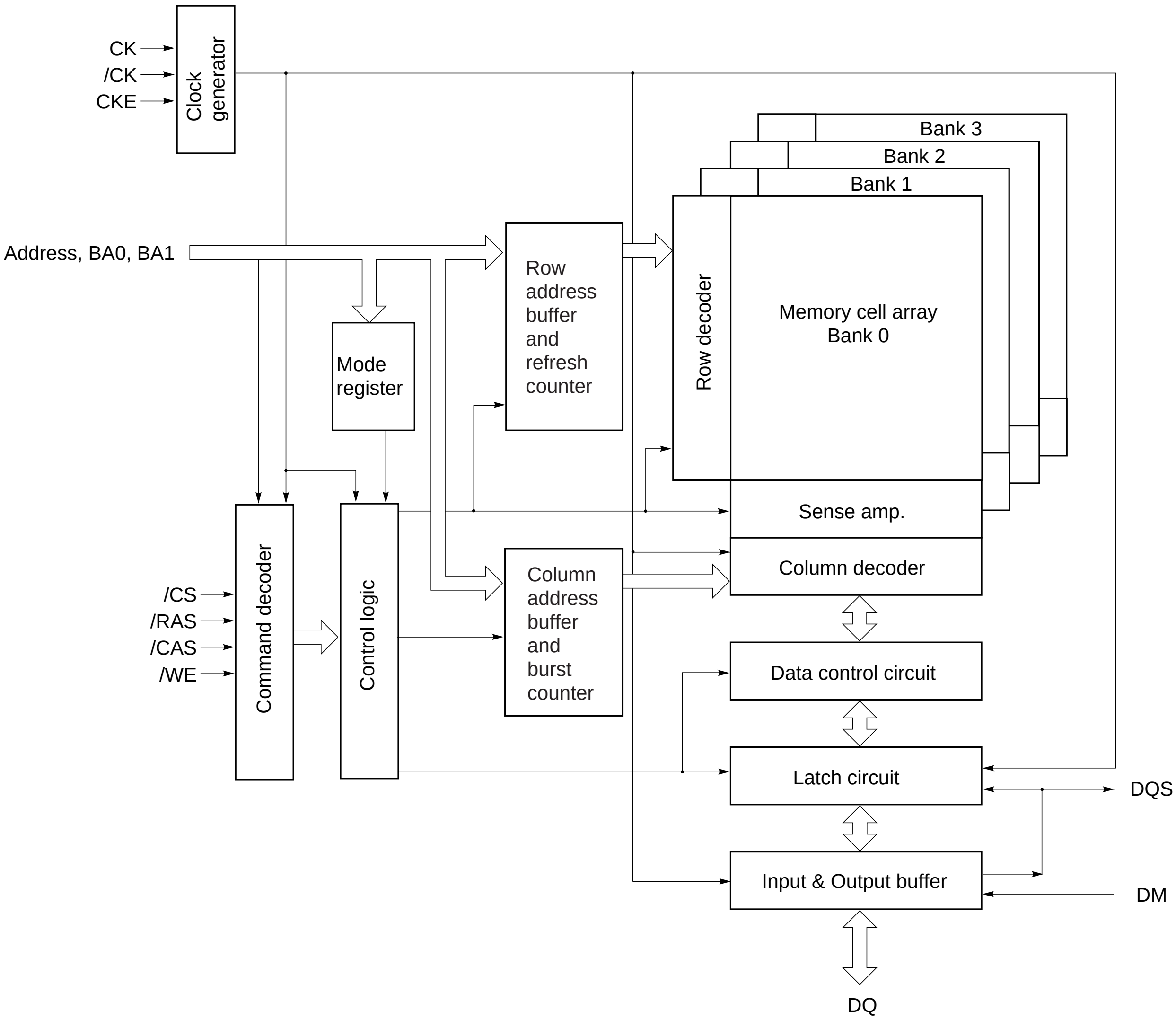
Timing Parameter Measured in Clock Cycle

Number of clock cycle	tCK	7.5ns			
Parameter	Symbol	min.	max.	Unit	Notes
Write to pre-charge command delay (same bank)	tWPD	3 + BL/2	—	tCK	
Read to pre-charge command delay (same bank)	tRPD	BL/2	—	tCK	
Write to read command delay (to input all data)	tWRD	2 + BL/2	—	tCK	
Burst stop command to write command delay (CL = 3)	tBSTW	3	—	tCK	
Burst stop command to DQ high-Z (CL = 3)	tBSTZ	3	—	tCK	
Read command to write command delay (to output all data) (CL = 3)	tRWD	3 + BL/2	—	tCK	
Pre-charge command to high-Z (CL = 3)	tHZP	3	—	tCK	
Write command to data in latency	tWCD	1	—	tCK	
Write recovery	tWR	2	—	tCK	
DM to data in latency	tDMD	0	—	tCK	
Mode register set command cycle time	tMRD	2	—	tCK	
Self-refresh exit to non-column command	tSREX	16	—	tCK	
Auto refresh period	tRFC	13	—	tCK	
Power down entry	tPDEN	2	—	tCK	1
Power down exit to command input	tPDEX	1	—	tCK	2
CKE minimum pulse width	tCKE	1	—	tCK	2

Notes: 1. The device will be into power down mode at the second CK rising edge after CKE to be low level with NOP or DESL command.

2. If PDEN command is issued but CKE stay in low level just for one clock (=tCKE min.) then CKE return to high level, the device will not be into power down mode.

Block Diagram



Pin Function

CK, /CK (input pins)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK and the /CK. The other input signals are referred at CK rising edge.

/CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A11 (input pins)

Row address (AX0 to AX11) is determined by the A0 to the A11 level at the cross point of the CK rising edge and the /CK falling edge in a bank active command cycle. Column address is loaded at the cross point of the CK rising edge and the /CK falling edge in a read or a write command cycle (See “Address Pins Table”). This column address becomes the starting address of a burst operation.

[Address Pins Table]

		Address (A0 to A11)	
Part number	Organization	Row address	Column address
EDK1216CFBJ	× 16 bits	AX0 to AX11	AY0 to AY8

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1/BA0 is precharged. If A10 = high when read or write command, auto-precharge function is enabled.

BA0 and BA1 (input pins)

BA0 and BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE controls power down mode, self-refresh function with other command inputs.

The CKE minimum pulse width should be 1 tCK.

DQ0 to DQ15 (input/output pins)

Data are input to and output from these pins.

UDQS and LDQS (input and output pin): DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

UDM and LDM (input pin)

DM is the reference signals of the data input mask function. DM is sampled at the cross point of DQS and VDDQ/2. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up.
Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

[DQS and DM Correspondence Table]

Part number	Organization	DQS	Data mask	DQs
EDK1216CFBJ	× 16 bits	LDQS	LDM	DQ0 to DQ7
		UDQS	UDM	DQ8 to DQ15

VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers. VDD and VDDQ must have same voltage range (1.7V to 1.95V).

Command Operation

Command Truth Table

The DDR Mobile RAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Command	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	BA1	BA0	AP	Address
Ignore command	DESL	H	H	H	×	×	×	×	×	×	×
No operation	NOP	H	H	L	H	H	H	×	×	×	×
Burst stop command	BST	H	H	L	H	H	L	×	×	×	×
Column address and read command	READ	H	H	L	H	L	H	V	V	L	V
Read with auto-precharge	READA	H	H	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	H	L	H	L	L	V	V	L	V
Write with auto-precharge	WRITA	H	H	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACT	H	H	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	L	×
Precharge all bank	PALL	H	H	L	L	H	L	×	×	H	×
Refresh	REF	H	H	L	L	L	H	×	×	×	×
	SELF	H	L	L	L	L	H	×	×	×	×
Mode register set	MRS	H	H	L	L	L	L	L	L	L	V
	EMRS	H	H	L	L	L	L	H	L	L	V

Remark: H: VIH. L: VIL. ×: Don't Care V: Valid address input

Note: The CKE level must be kept for 1 CK cycle at least.

Ignore command [DESL]

When /CS is high at the cross point of the CK rising edge and the VDDQ/2 level, all input signals are neglected and internal state is held.

No operation [NOP]

As long as this command is input at the cross point of the CK rising edge and the VDDQ/2 level, address and data input are neglected and internal state is held.

Burst stop command [BST]

This command stops a current burst operation.

Column address strobe and read command [READ]

This command starts a read operation. The start address of the burst read is determined by the column address (See "Address Pins Table" in Pin Function) and the bank select address. After the completion of the read operation, all output buffers become high-Z.

Read with auto-precharge [READA]

This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]

This command starts a write operation. The start address of the burst write is determined by the column address (See "Address Pins Table" in Pin Function) and the bank select address.

Write with auto-precharge [WRITA]

This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACT]

This command activates the bank that is selected by BA0 and BA1 and determines the row address (AX0 to AX12). (See Bank Select Signal Table)

Precharge selected bank [PRE]

This command starts precharge operation for the bank selected by BA0 and BA1. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

Precharge all banks [PALL]

This command starts a precharge operation for all banks.

Refresh [REF/SELF]

This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]

The DDR Mobile RAM has the two mode registers, the mode register and the extended mode register, to defines how it works. The both mode registers are set through the address pins (the A0 to the A11, BA0 to BA1) in the mode register set cycle. For details, refer to "Mode register and extended mode register set".

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR Mobile RAM.

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation
Precharging*[1]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL*[11]
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[11]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	×	×		ILLEGAL
Idle*[2]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[11]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[11]
	L	L	H	H	BA, RA	ACT	Activating
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh/ Self-refresh*[12]
	L	L	L	L	MODE	MRS	Mode register set*[12]
Refresh (auto-refresh)*[3]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	H	H	H	L	×	BST	ILLEGAL
	L	H	L	×	×		ILLEGAL
	L	L	×	×	×		ILLEGAL
Activating*[4]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL*[11]
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[11]
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[11]
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11]
	L	L	L	×	×		ILLEGAL
Active*[5]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge
	L	L	L	×	×		ILLEGAL

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation
Read*[6]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	Burst stop
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[13]
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start pre-charge
	L	L	L	×	×		ILLEGAL
Read with auto-pre-charge*[7]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11]
	L	L	L	×	×		ILLEGAL
Write*[8]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	Burst Stop
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.
	L	L	L	×	×		ILLEGAL
Write recovering*[9]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*[11]
	L	L	L	×	×		ILLEGAL

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation
Write with auto- pre-charge*[10]	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11]
	L	L	L	×	×		ILLEGAL

Remark: H: VIH. L: VIL. ×: Don’t Care

Notes: 1. The DDR Mobile RAM is in "Precharging" state for tRP after precharge command is issued.

2. The DDR Mobile RAM reaches "IDLE" state tRP after precharge command is issued.
3. The DDR Mobile RAM is in "Refresh" state for tRFC after auto-refresh command is issued.
4. The DDR Mobile RAM is in "Activating" state for tRCD after ACT command is issued.
5. The DDR Mobile RAM is in "Active" state after "Activating" is completed.
6. The DDR Mobile RAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR Mobile RAM is in "READ with auto-precharge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR Mobile RAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR Mobile RAM is in "Write recovering" for tWR after the last data are input.
10. The DDR Mobile RAM is in "Write with auto-precharge" until tWR after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. All banks must be in "IDLE".
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued.

CKE Truth Table

Current state	Command	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address	Notes
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×	2
Idle/Active	Power down entry (PDEN)	H	L	L	H	H	H	×	
		H	L	H	×	×	×	×	
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Power down	Power down exit (PDEX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	

Notes: 1. H: VIH . L: VIL × : Don't Care .
2. All the banks must be in IDLE before executing this command.
3. The CKE level must be kept for 1 clock cycle at least.

Auto-refresh command [REF]

This command executes auto-refresh. The bank and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The output buffer becomes high-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACT or MRS command can be issued tRFC after the last auto-refresh command.

The average refresh cycle is 15.6µs. To allow for improved efficiency in scheduling, some flexibility in the absolute refresh interval (64ms) is provided. A maximum of eight auto-refresh commands can be posted to the DDR Mobile RAM or the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 8 × tREF.

Self-refresh entry [SELF]

This command starts self-refresh. The self-refresh operation continues as long as CKE is held low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power down mode entry [PDEN]

tPDEN (= 2 clocks) after the cycle when [PDEN] is issued, the DDR Mobile RAM enters into power-down mode. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held low. No internal refresh operation occurs during the power down mode.

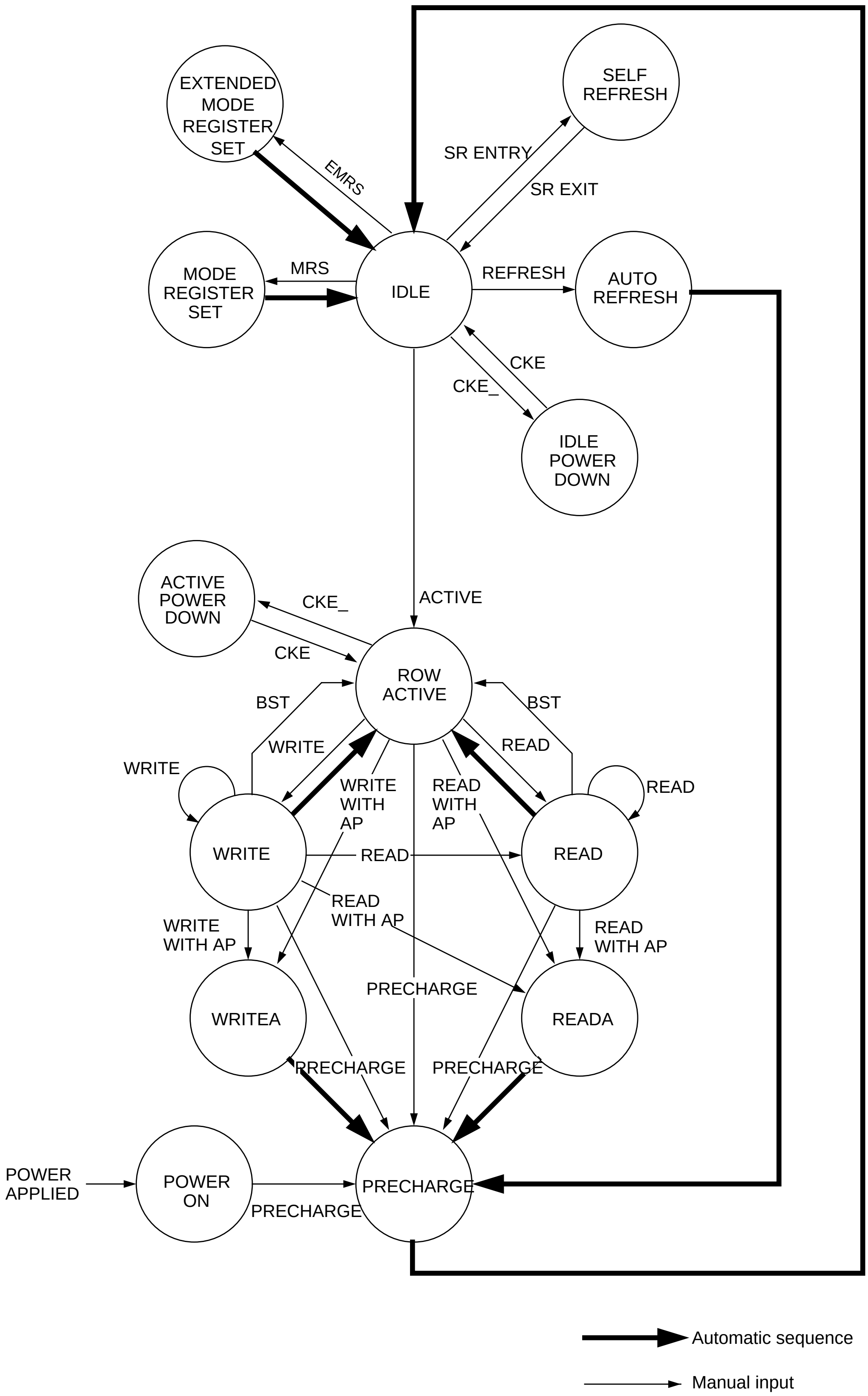
Self-refresh exit [SELFX]

This command is executed to exit from self-refresh mode. tSREX after [SELFX], the device will be into idle state.

Power down exit [PDEX]

The DDR Mobile RAM can exit from power down mode tPDEX (1 cycle min.) after the cycle when [PDEX] is issued.

Simplified State Diagram



Operation of the DDR Mobile RAM

Initialization

The DDR Mobile RAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 200µs or longer pause must precede any signal toggling. VDD should be turned on simultaneously or before VDDQ.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum tRP is satisfied, two or more Auto refresh must be performed.

(4) The mode register must be programmed and the extended mode register should be programmed. After the mode register set cycle or the extended mode register set cycle, tMRD (2 clocks minimum) pause must be satisfied.

Remarks:

1 The sequence of Auto refresh, mode register programming and extended mode register programming above may be transposed.

2 CKE must be held high until the Precharge command is issued to ensure data-bus high-Z.

Mode Register and Extended Mode Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A11 and BA0 and BA1 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A11 and BA0 and BA1 pins during mode register set cycles. BA0 and BA1 determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.

Mode register

The mode register has four fields;

Reserved	: A11 through A7
/CAS latency	: A6 through A4
Wrap type	: A3
Burst length	: A2 through A0

Following mode register programming, no command can be issued before at least 2 clocks have elapsed.

/CAS Latency

/CAS latency must be set to 3.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become high-Z. The burst length is programmable as 2, 4, 8 and 16.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. “Burst Operation” shows the addressing sequence for each burst length for each wrap type.

Extended Mode Register

The extended mode register has three fields;

Reserved	: A11 through A7, A4, A3
Driver Strength	: A6 through A5
Partial Array Self Refresh	: A2 through A0

Following extended mode register programming, no command can be issued before at least 2 clocks have elapsed.
Note: EMRS has default value at power up. [A9 : A0] = [00 0000 0000].

Driver Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Advanced Temperature Compensated Self Refresh (ATCSR)

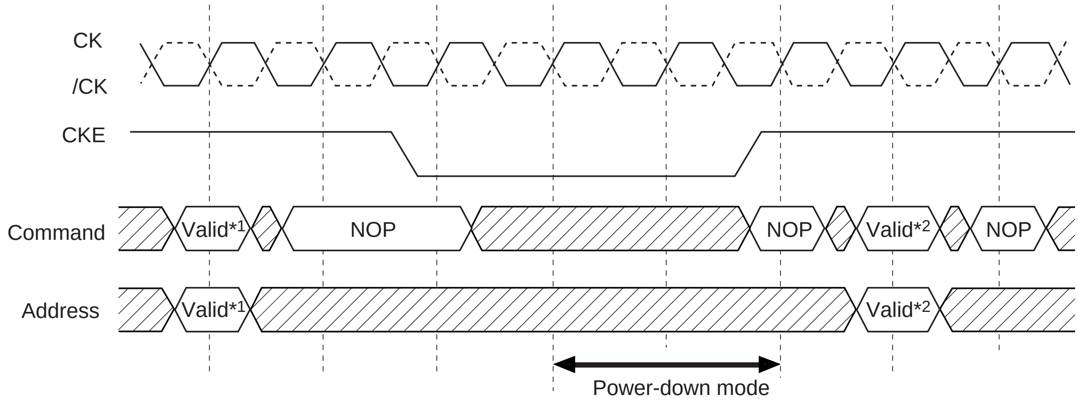
The DDR Mobile RAM automatically changes the self-refresh cycle by on die temperature sensor. No extended mode register program is required. Manual TCSR (Temperature Compensated Self-Refresh) is not implemented.

Partial Array Self Refresh

Memory array size to be refreshed during self-refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self-refresh.

Power-Down Mode and CKE Control

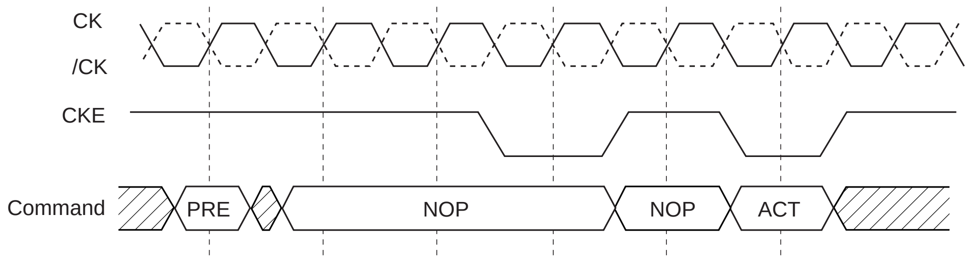
DDR Mobile RAM will be into power-down mode at the second CK rising edge after CKE to be low level with NOP or DESL command at first CK rising edge after CKE signal to be low.



Notes: 1. Valid*1 can be either Activate command or Precharge command, When Valid*1 is Activate command, power-down mode will be active power-down mode, while it will be precharge power down mode, if Valid*1 will be Precharge command.
2. Valid*2 can be any command as long as all of specified AC parameters are satisfied.

Power-Down Entry and Exit

However, if the CKE has one clock cycle high and on clock cycle low just as below, even DDR Mobile RAM will not enter power-down mode, this command flow does not hurt any data and can be done.



Note: Assume PRE and ACT command is closing and activating same bank.

CKE Control

Mode Register Definition

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

Latency mode

Bits6-4	/CAS latency
000	R
001	R
010	R
011	3
100	R
101	R
110	R
111	R

Burst length

Bits2-0	WT = 0	WT = 1
000	R	R
001	2	2
010	4	4
011	8	8
100	16	16
101	R	R
110	R	R
111	R	R

Wrap type

0	Sequential
1	Interleave

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	0	0	0	DS		0	0	PASR			Extended Mode Register Set

Driver Strength

Bits6-5	Strength
00	Normal
01	1/2 strength
10	1/4 strength
11	1/8 strength

Partial Array Self Refresh

Bits2-0	Refresh Array
000	All banks
001	Bank A & Bank B (BA1=0)
010	Bank A (BA0=BA1=0)
011	R
100	R
101	R
110	R
111	R

Remark R : Reserved

Burst Operation

The burst type (BT) and the first three bits of the column address determine the order of a data out.

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1	0, 1
1	1, 0	1, 0

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3	0, 1, 2, 3
0	1	1, 2, 3, 0	1, 0, 3, 2
1	0	2, 3, 0, 1	2, 3, 0, 1
1	1	3, 0, 1, 2	3, 2, 1, 0

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Burst length = 16

Starting Ad.				Addressing(decimal)	
A3	A2	A1	A0	Sequence	Interleave
0	0	0	0	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15
0	0	0	1	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, 11, 10, 13, 12, 15, 14
0	0	1	0	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1	2, 3, 0, 1, 6, 7, 4, 5, 10, 11, 8, 9, 14, 15, 12, 13
0	0	1	1	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4, 11, 10, 9, 8, 15, 14, 13, 12
0	1	0	0	4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3, 12, 13, 14, 15, 8, 9, 10, 11
0	1	0	1	5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2, 13, 12, 15, 14, 9, 8, 11, 10
0	1	1	0	6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1, 14, 15, 12, 13, 10, 11, 8, 9
0	1	1	1	7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0, 15, 14, 13, 12, 11, 10, 9, 8
1	0	0	0	8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7	8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7
1	0	0	1	9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8	9, 8, 11, 10, 13, 12, 15, 14, 1, 0, 3, 2, 5, 4, 7, 6
1	0	1	0	10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9	10, 11, 8, 9, 14, 15, 12, 13, 2, 3, 0, 1, 6, 7, 4, 5
1	0	1	1	11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	11, 10, 9, 8, 15, 14, 13, 12, 3, 2, 1, 0, 7, 6, 5, 4
1	1	0	0	12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	12, 13, 14, 15, 8, 9, 10, 11, 4, 5, 6, 7, 0, 1, 2, 3
1	1	0	1	13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13, 12, 15, 14, 9, 8, 11, 10, 5, 4, 7, 6, 1, 0, 3, 2
1	1	1	0	14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	14, 15, 12, 13, 10, 11, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
1	1	1	1	15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

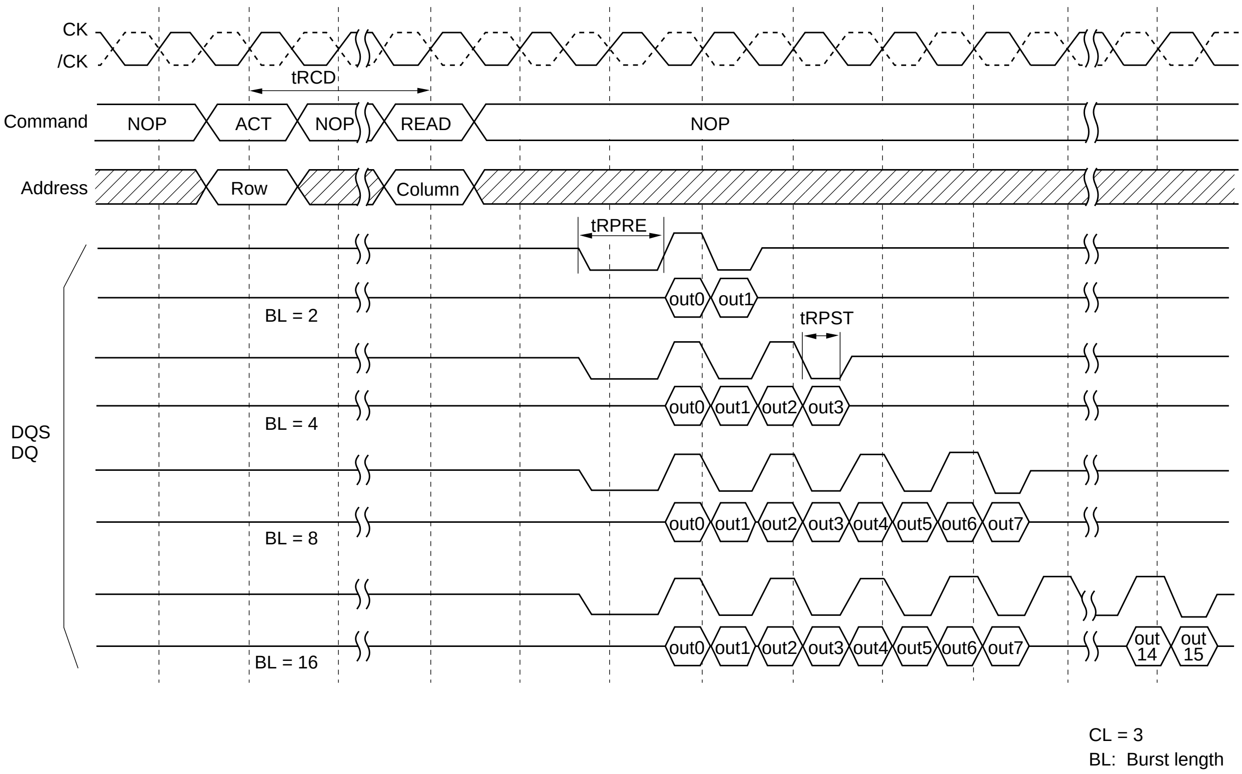
Read/Write Operations

Bank Active

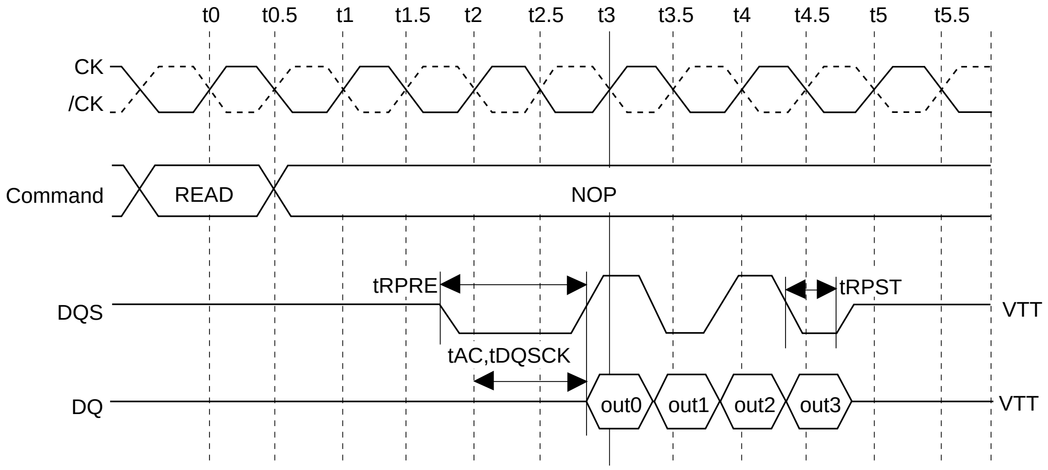
A read or a write operation begins with the bank active command [ACT]. The bank active command determines a bank address and a row address. For the bank and the row, a read or a write command can be issued tRCD after the ACT is issued.

Read operation

The burst length (BL), the /CAS latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command that can be set to 2, 4, 8 or 16. The starting address of the burst read is defined by the column address, the bank select address which is loaded via the A0 to A11 and BA0 and BA1 pins in the cycle when the read command is issued. The data output timing is characterized by CL and tAC. The read burst start (CL-1) × tCK + tAC (ns) after the clock rising edge where the read command is latched. The DDR Mobile RAM outputs the data strobe through DQS pins simultaneously with data. tRPRE prior to the first rising edge of the data strobe, the DQS pins are driven low from high-Z state. This low period of DQS is referred as read preamble. The burst data are output coincidentally at both the rising and falling edge of the data strobe. The DQ pins become high-Z in the next cycle after the burst read operation completed. tRPST from the last falling edge of the data strobe, the DQS pins become high-Z. This low period of DQS is referred as read postamble.



Read Operation (Burst Length)

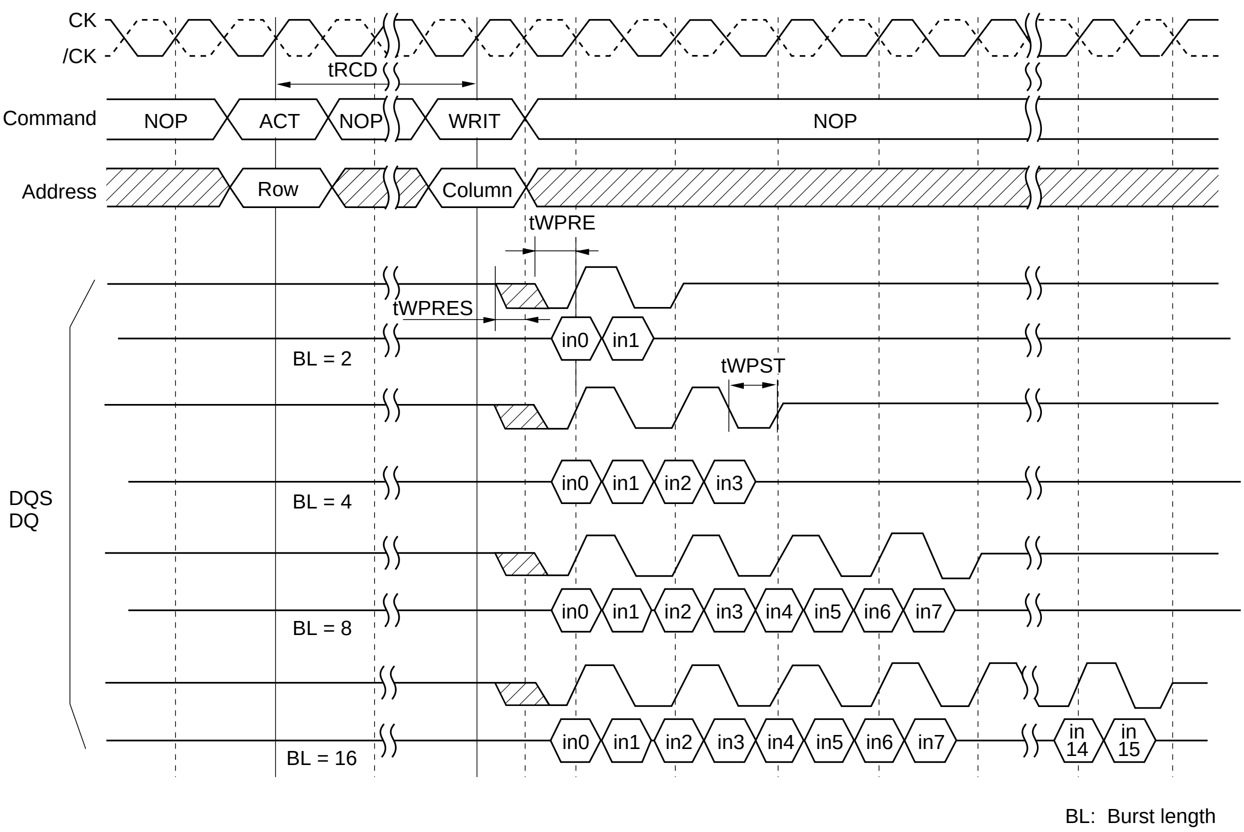


Read Operation (/CAS Latency)

Write operation

The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued. The burst length (BL) determines the length of a sequential data input by the write command that can be set to 2, 4, 8 or 16. The latency from write command to data input is fixed to 1. The starting address of the burst write is defined by the column address, the bank select address which is loaded via the A0 to A11, BA0 to BA1 pins in the cycle when the write command is issued. DQS should be input as the strobe for the input-data and DM as well during burst operation. tWPRE prior to the first rising edge of DQS, DQS must be set to low. tWPST after the last falling edge of DQS, the DQS pins can be changed to high-Z. The leading low period of DQS is referred as write preamble. The last low period of DQS is referred as write postamble.

Example



Write Operation

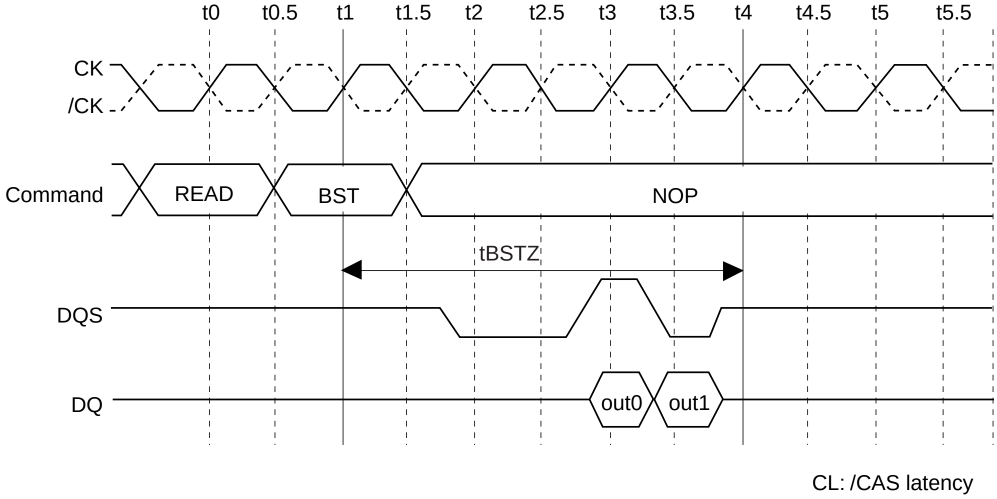
Burst Stop

Burst stop command during burst operation

The burst stop (BST) command stops the burst read and sets all output buffers to high-Z. tBSTZ (= CL) cycles after a BST command issued, all DQ and DQS pins become high-Z.

The BST command is also supported for the burst write operation. No data will be written in subsequent cycles.

Note that bank address is not referred when this command is executed.

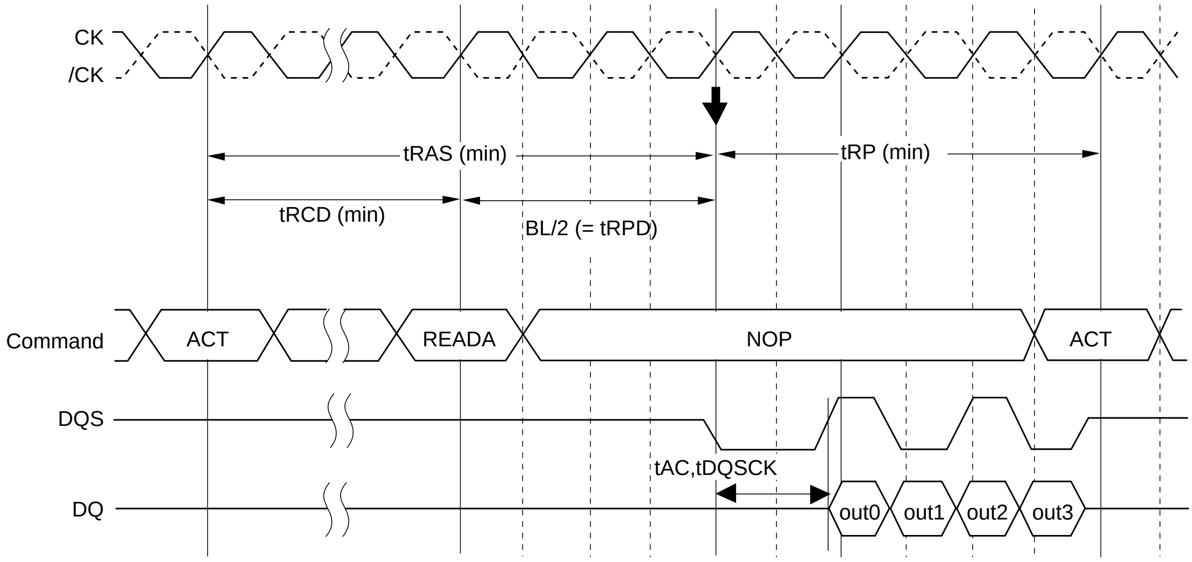


Burst Stop during a Read Operation

Auto-Precharge

Read with auto-precharge

The precharge is automatically performed after completing a read operation. The precharge starts BL/2 (= tRPD) clocks after READA command input. tRAS lock out mechanism for READA allows a read command with auto precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the tRAS (min) specification. A column command to the other active bank can be issued the next cycle after the last data output. Read with auto-precharge command does not limit row commands execution for other bank.



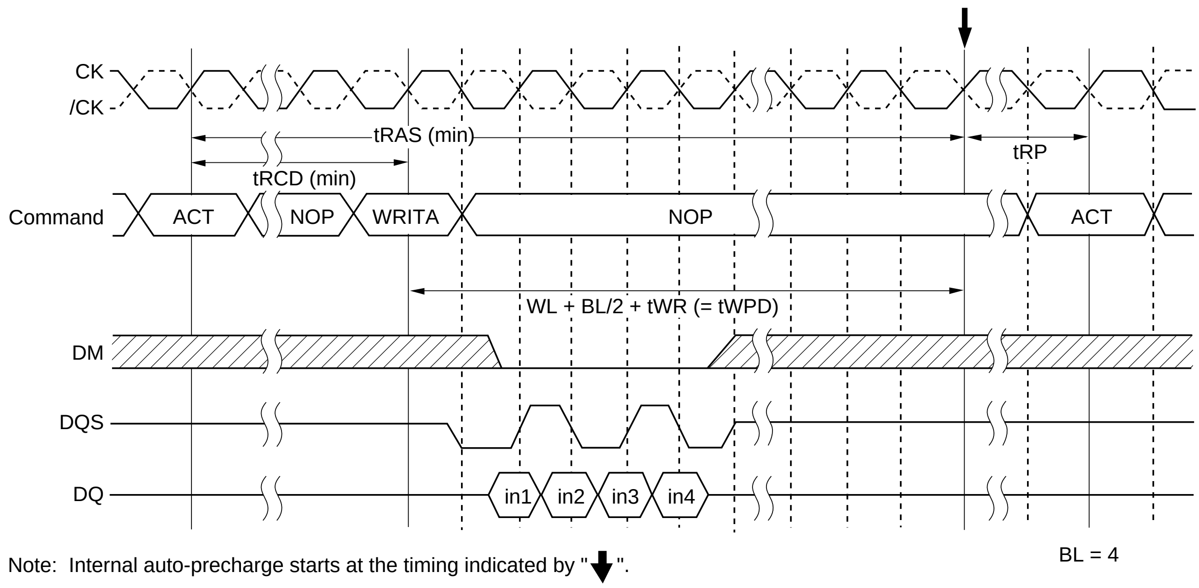
Note: Internal auto-precharge starts at the timing indicated by "↓".

Read with auto-precharge

Write with auto-precharge

The precharge is automatically performed after completing a burst write operation. The precharge operation is started (WL) + BL/2 + tWR (= tWPD) clocks after WRITA command issued.

A column command to the other banks can be issued the next cycle after the internal precharge command issued. Write with auto-precharge command does not limit row commands execution for other bank.



Note: Internal auto-precharge starts at the timing indicated by "↓".

Burst Write (BL = 4)

The Concurrent Auto Precharge

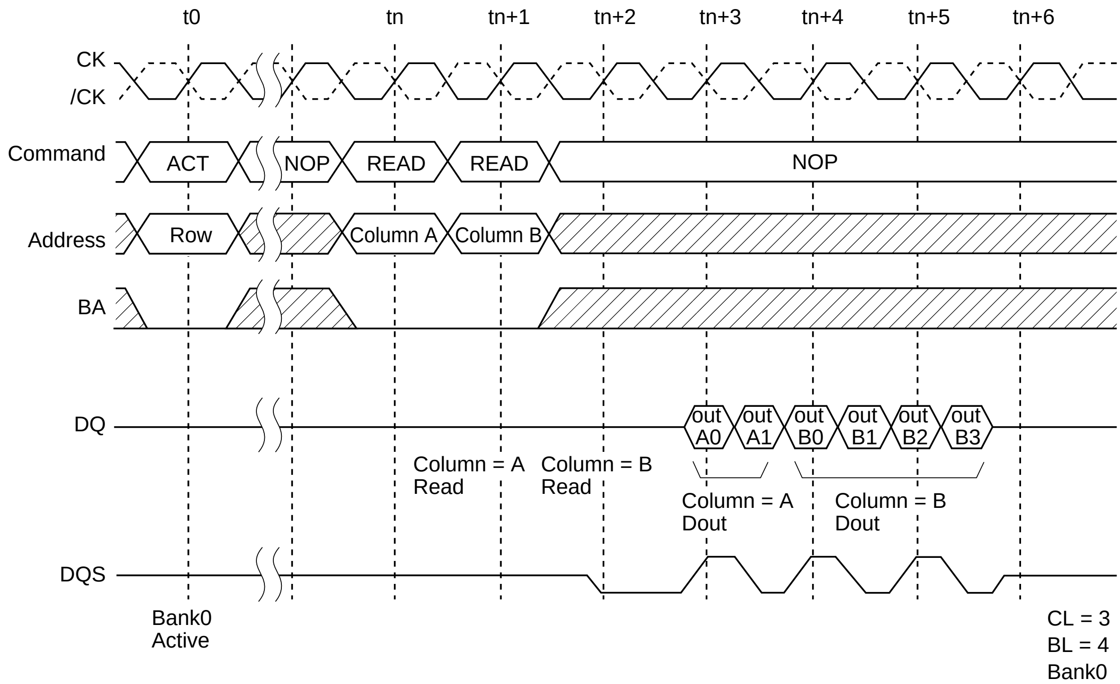
The DDR Mobile RAM supports the concurrent auto precharge feature, a read with auto-precharge or a write with auto-precharge, can be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided.) The minimum delay from a read or write command with auto precharge, to a command to a different bank, is summarized below.

From command	To command (different bank, non-interrupting command)	Minimum delay (Concurrent AP supported)	Units
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	CL (rounded up)+ (BL/2)	tCK
	Precharge or Activate	1	tCK
Write w/AP	Read or Read w/AP	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK

Command Intervals

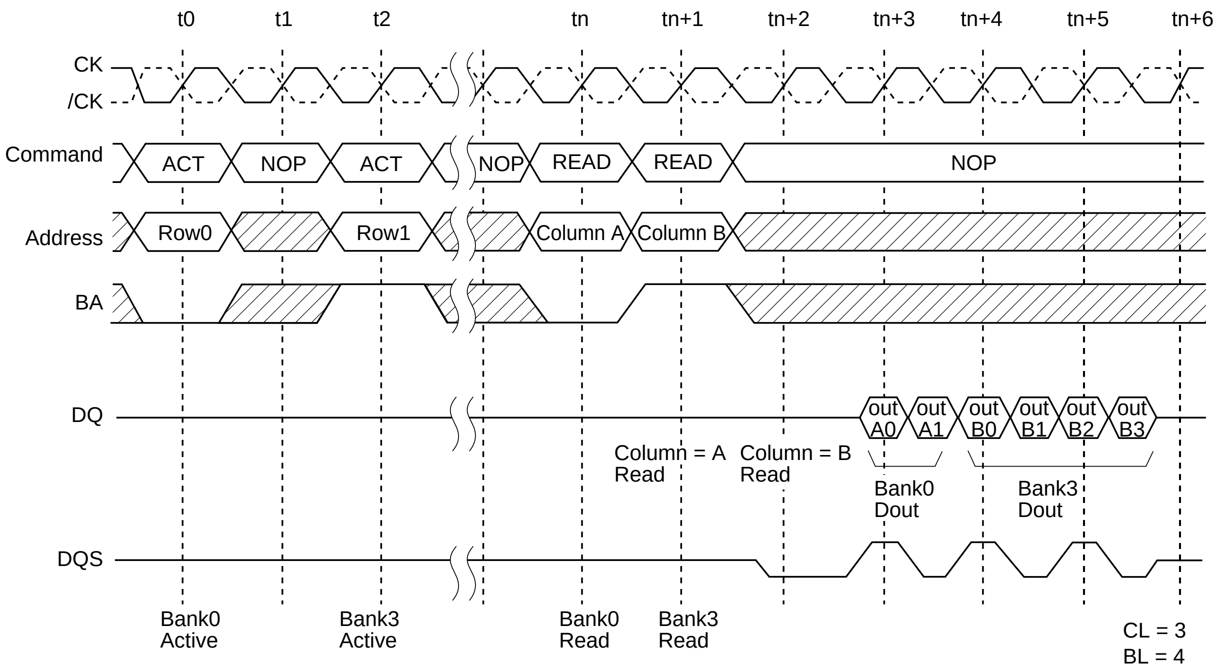
A Read command to the consecutive Read command Interval

	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
2.	Same	Different	—	Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See ‘A read command to the consecutive precharge interval’ section.
3.	Different	Any	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued.



READ to READ Command Interval (same ROW address in the same bank)*

Note: n ≥ 3

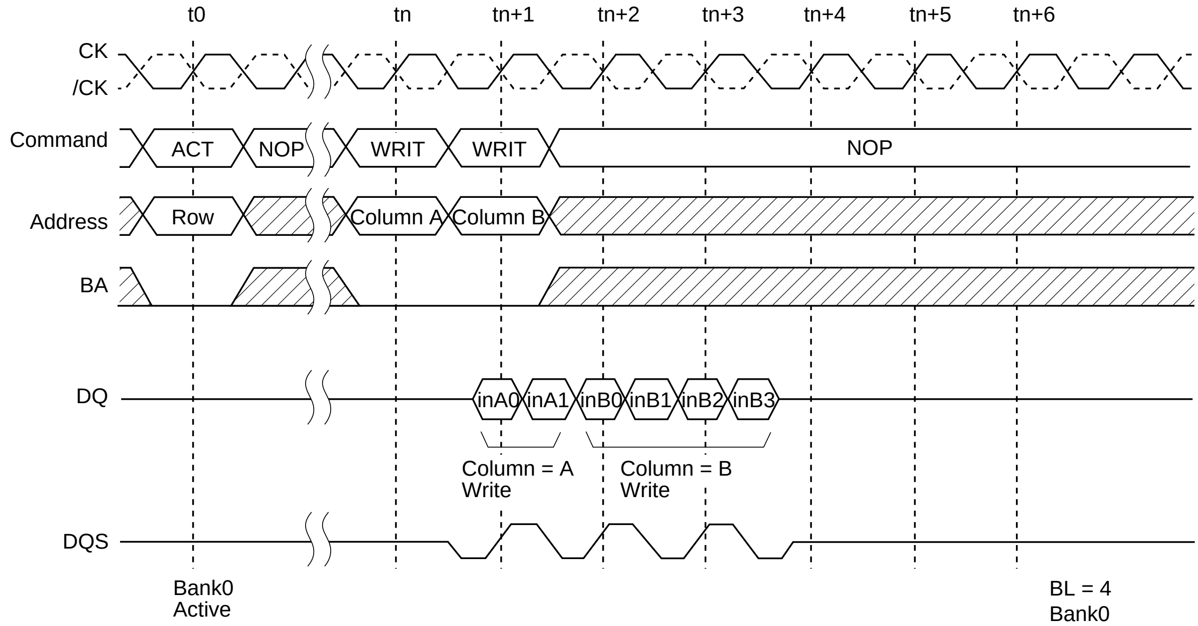


READ to READ Command Interval (different bank)*

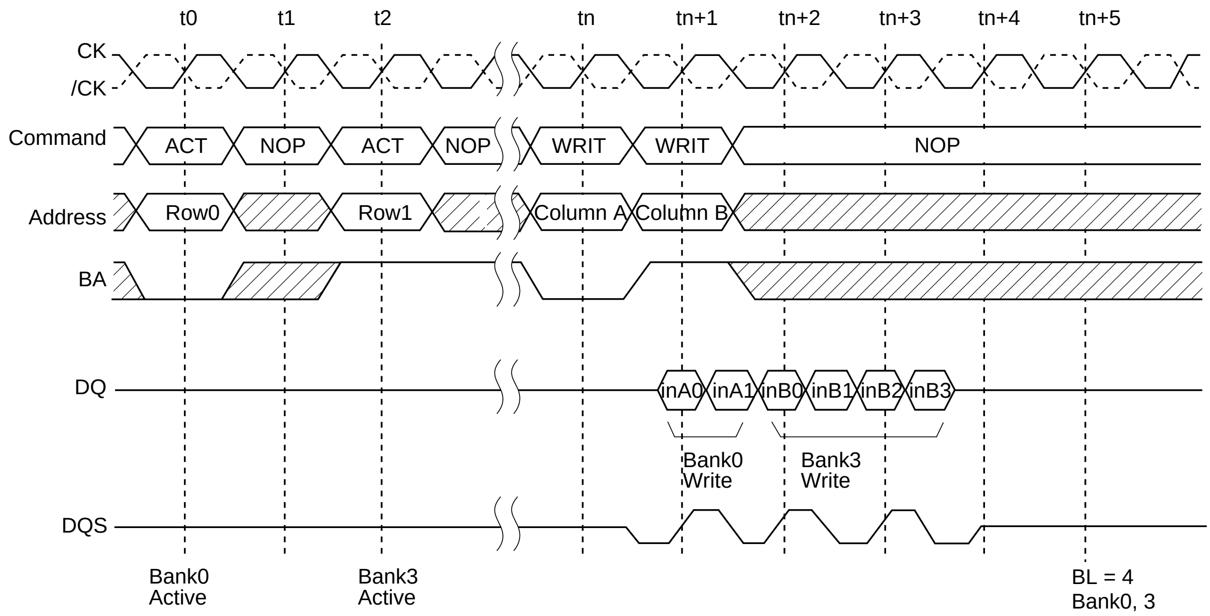
Note: $n \geq 3$

A Write command to the consecutive Write command Interval

Destination row of the consecutive write command: Bank address	Row address	State	Operation
1. Same	Same	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
2. Same	Different	—	Precharge the bank to interrupt the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See 'A write command to the consecutive precharge interval' section.
3. Different	Any	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
		IDLE	Precharge the bank without interrupting the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued.



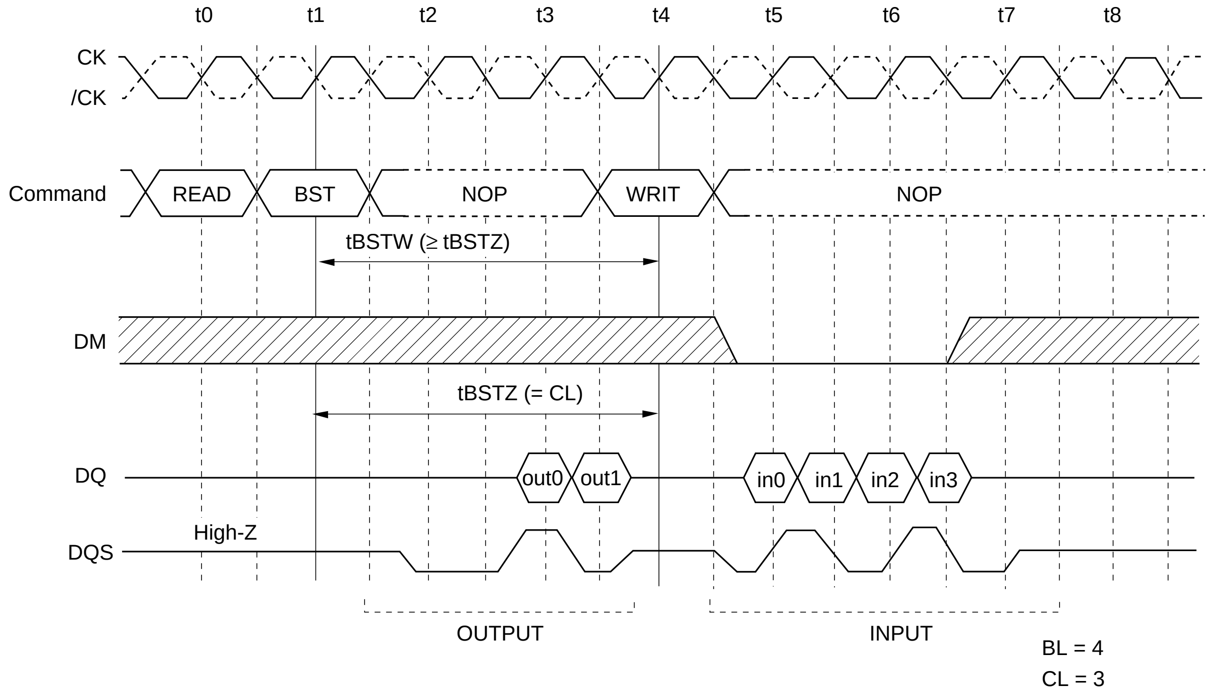
WRITE to WRITE Command Interval (same ROW address in the same bank)



WRITE to WRITE Command Interval (different bank)

A Read command to the consecutive Write command interval with the BST command

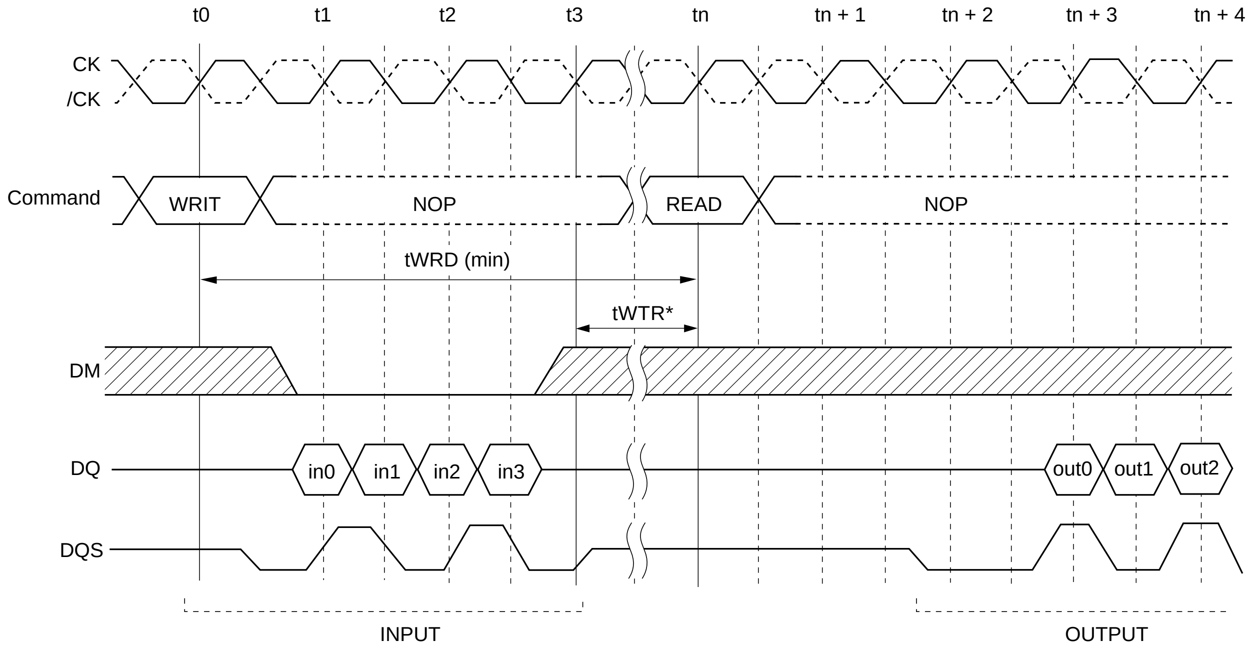
	Destination row of the consecutive write command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	Issue the BST command. tBSTW (≥ tBSTZ) after the BST command, the consecutive write command can be issued.
2.	Same	Different	—	Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	Issue the BST command. tBSTW (≥ tBSTZ) after the BST command, the consecutive write command can be issued.
			IDLE	Precharge the bank independently of the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued.



READ to WRITE Command Interval

A Write command to the consecutive Read command interval: To complete the burst operation

	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	To complete the burst operation, the consecutive read command should be performed tWRD (= BL/ 2 + 2) after the write command.
2.	Same	Different	—	Precharge the bank tWPD after the preceding write command. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3.	Different	Any	ACTIVE	To complete a burst operation, the consecutive read command should be performed tWRD (= BL/ 2 + 2) after the write command.
			IDLE	Precharge the bank independently of the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued.



Note: tWTR is referenced from the first positive CK edge after the last desired data in pair tWTR.

BL = 4
CL = 3

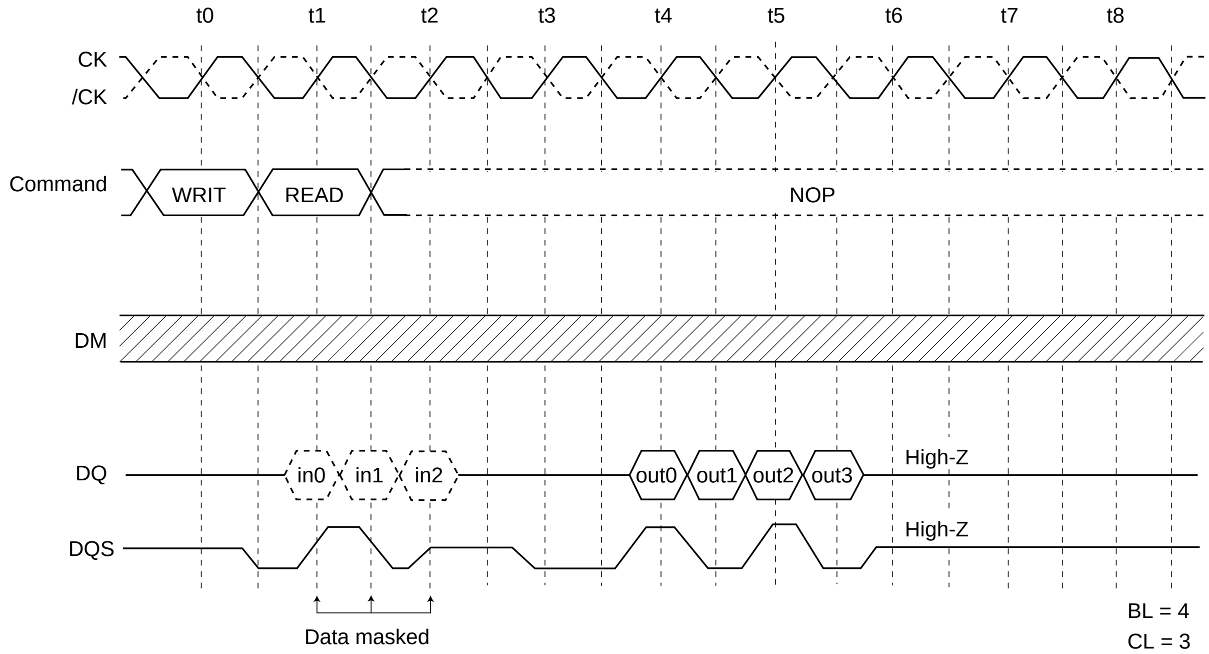
WRITE to READ Command Interval

A Write command to the consecutive Read command interval: To interrupt the write operation

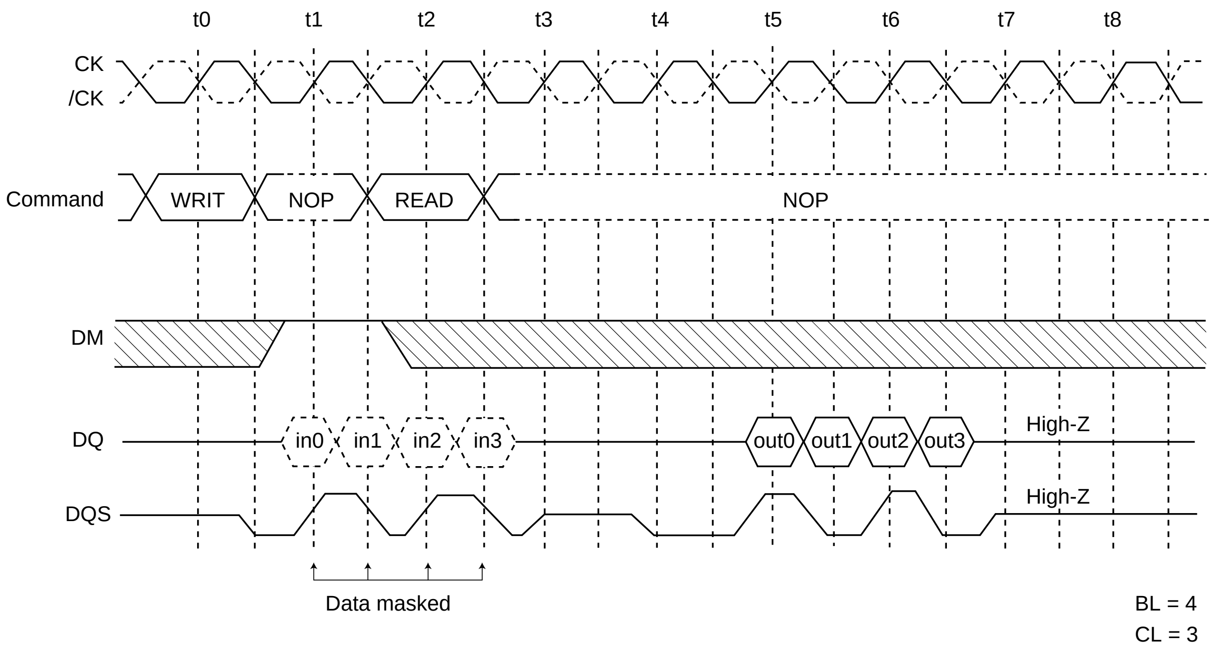
	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1.	Same	Same	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
2.	Same	Different	—	—*[1]
3.	Different	Any	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
			IDLE	—*[1]

Note: 1. Precharge must be preceded to read command. Therefore read command can not interrupt the write operation in this case.

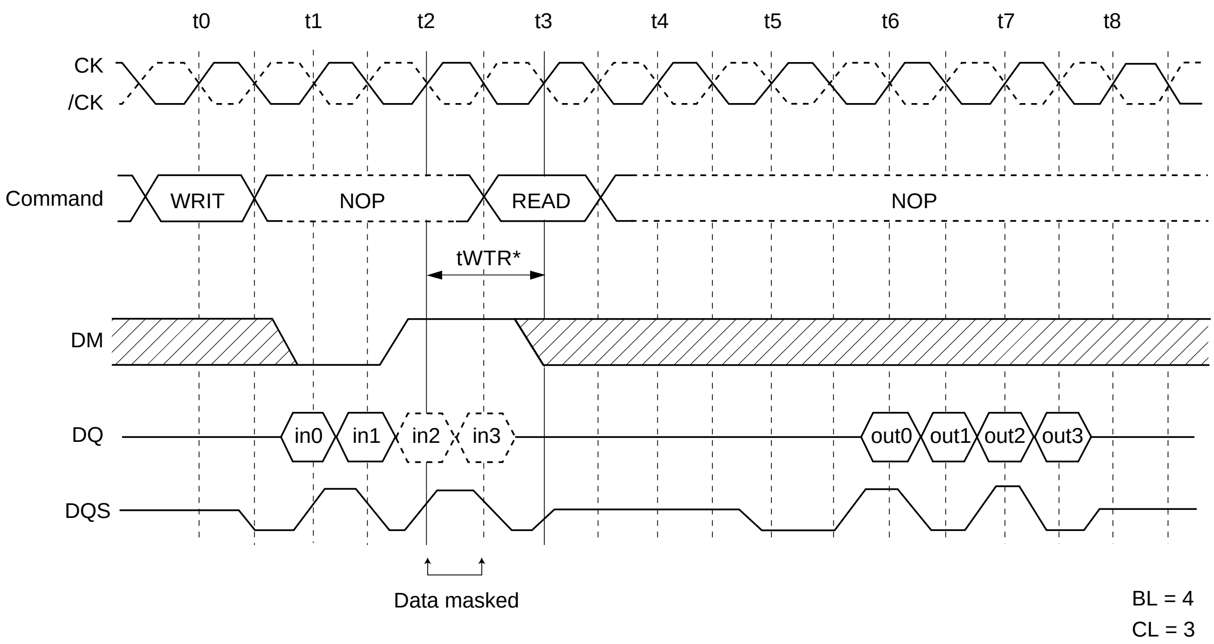
WRITE to READ Command Interval (Same bank, same ROW address)



[WRITE to READ delay = 1 clock cycle]



[WRITE to READ delay = 2 clock cycle]

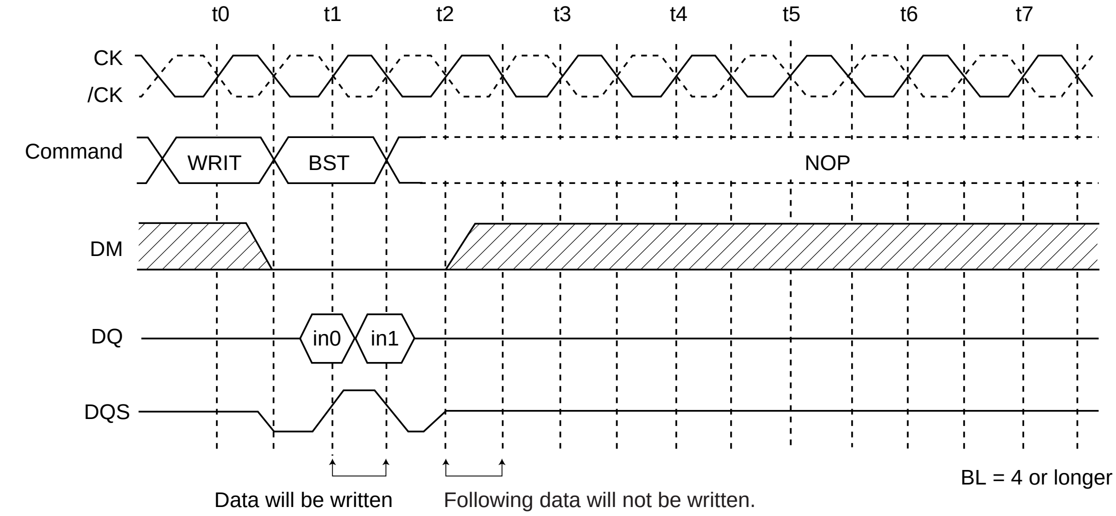


Note: tWTR is referenced from the first positive CK edge after the last desired data in pair tWTR.

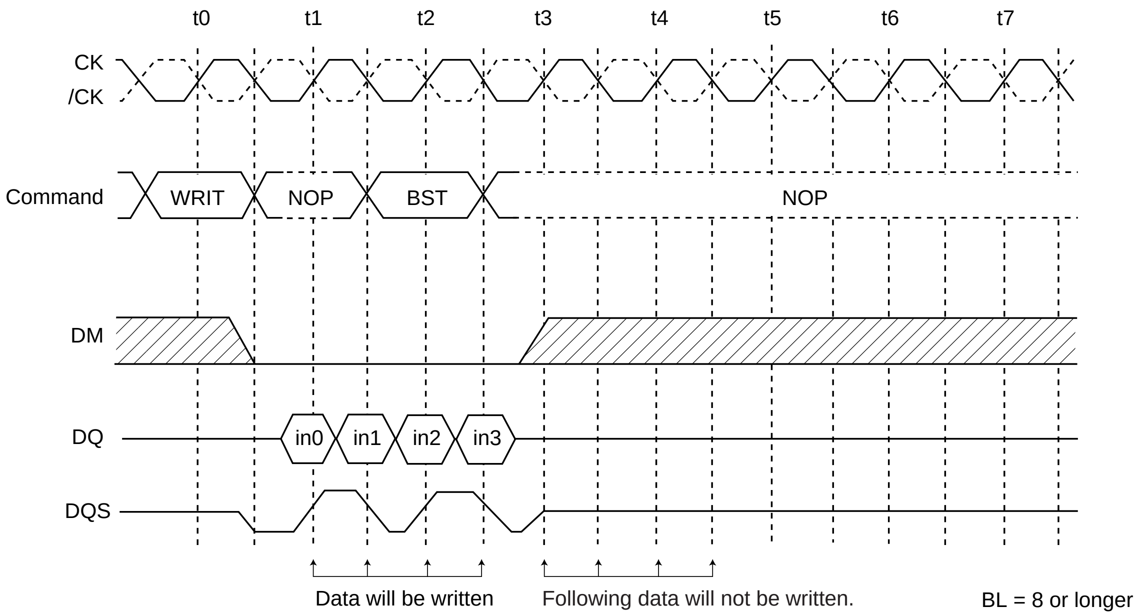
[WRITE to READ delay = 3 clock cycle]

A Write command to the Bust stop command interval: To interrupt the write operation

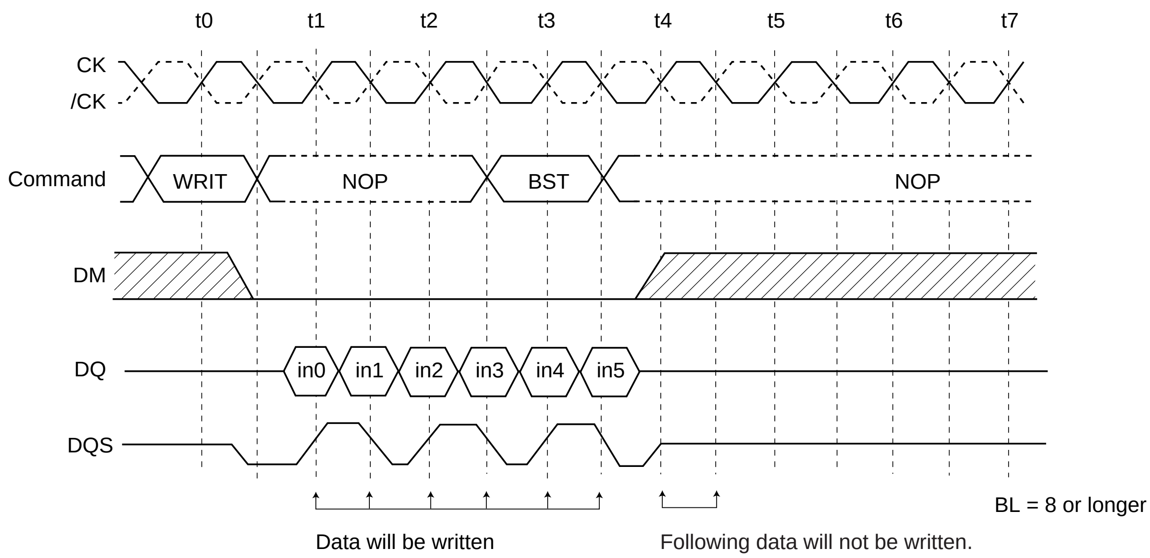
WRITE to BST Command Interval (Same bank, same ROW address)



[WRITE to BST delay = 1 clock cycle]



[WRITE to BST delay = 2 clock cycle]



[WRITE to BST delay = 3 clock cycle]

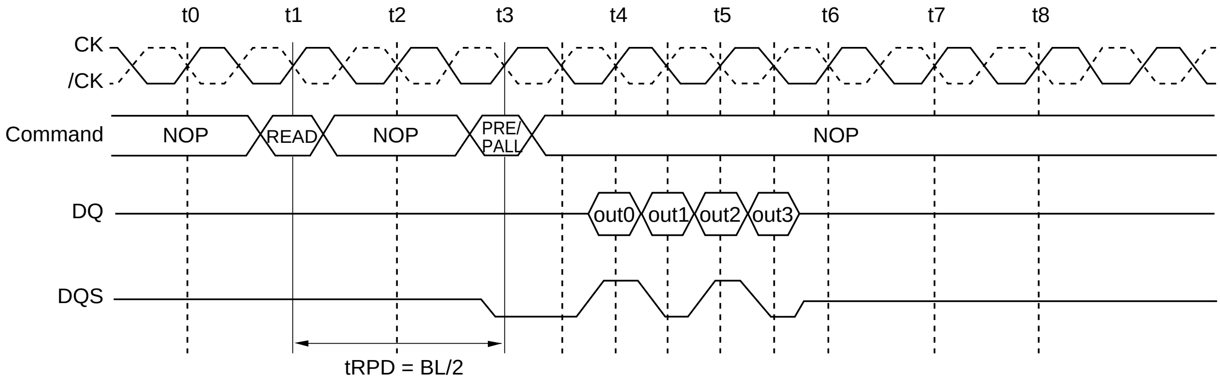
A Read command to the consecutive Precharge command interval

Operation by each case of destination bank of the consecutive Precharge command.

	Bank address	Operation
1.	Same	The PRE and PALL command can interrupt a read operation. To complete a burst read operation, tRPD is required between the read and the precharge command. Please refer to the following timing chart.
2.	Different	The PRE command does not interrupt a read command. No interval timing is required between the read and the precharge command.

READ to PRECHARGE Command Interval (same bank) : To output all data

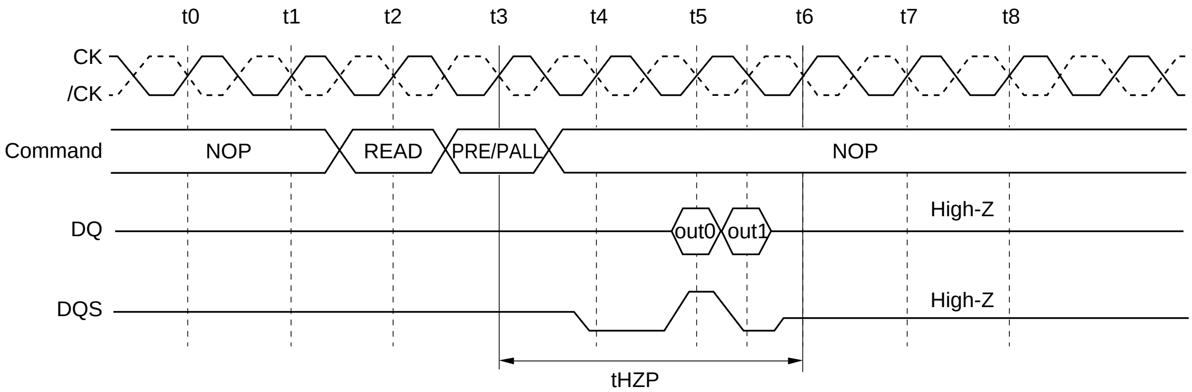
To complete a burst read operation and get a burst length of data, the consecutive precharge command must be issued tRPD (= BL/ 2 cycles) after the read command is issued.



READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)

READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with a precharge command. All DQ pins and DQS pins become high-Z tHZP (= CL) after the precharge command.



READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 4, 8)

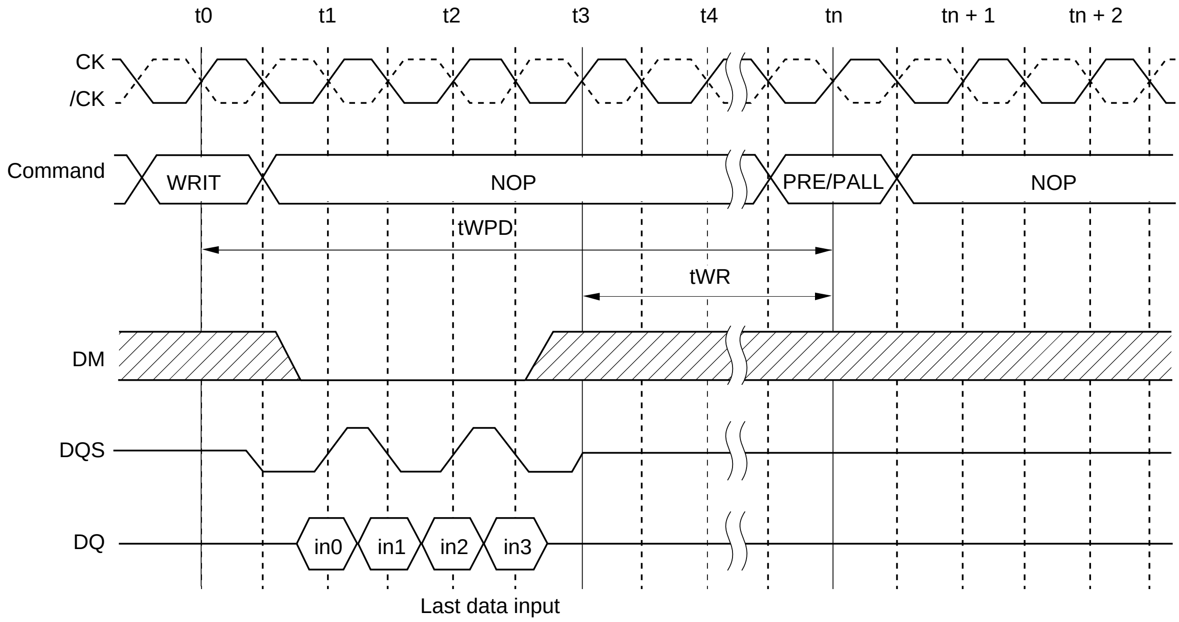
A Write command to the consecutive Precharge command interval

Operation by each case of destination bank of the consecutive Precharge command.

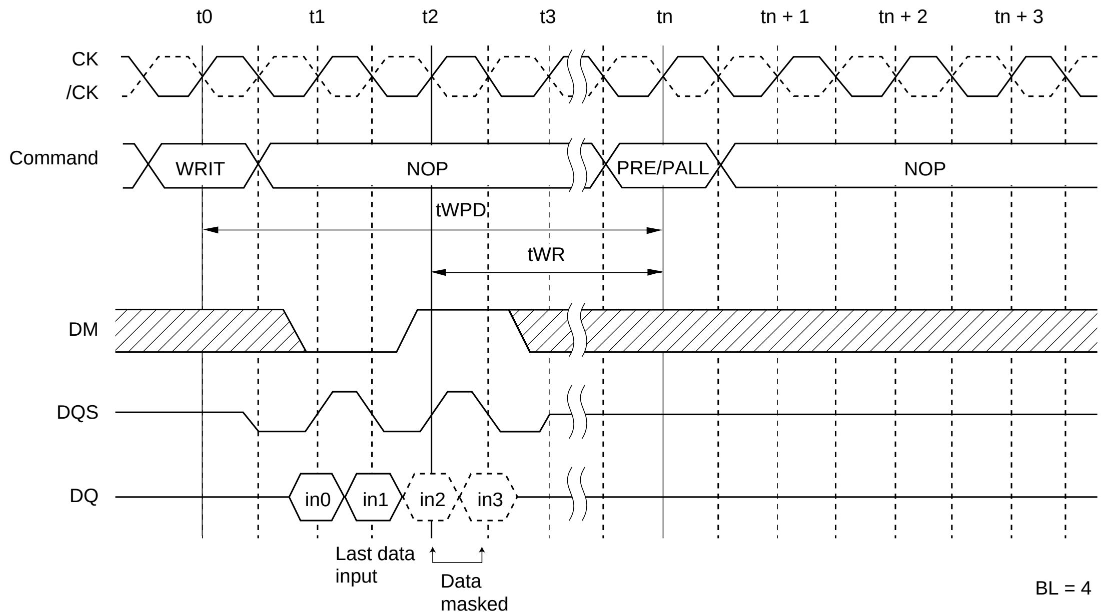
	Bank address	Operation
1.	Same	The PRE and PALL command can interrupt a write operation. To complete a burst write operation, tWPD is required between the write and the precharge command. Please refer to the following timing chart.
2.	Different	The PRE command does not interrupt a write command. No interval timing is required between the write and the precharge command.

WRITE to PRECHARGE Command Interval (same bank)

The minimum interval tWPD is necessary between the write command and the precharge command.



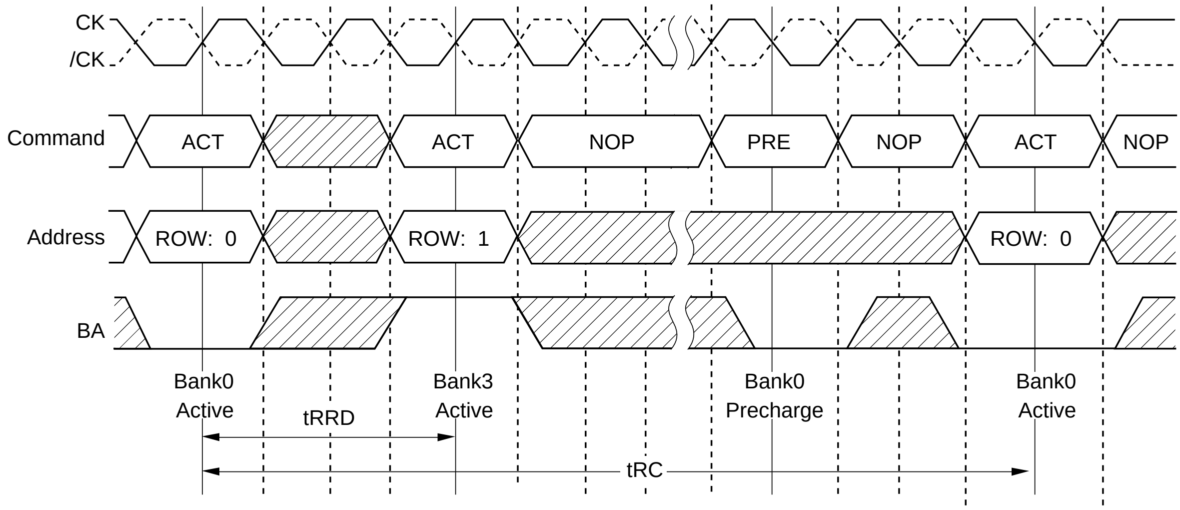
WRITE to PRECHARGE Command Interval (same bank) (BL = 4)



WRITE to PRECHARGE Command Interval (same bank) (BL = 4, DM to mask data)

Bank active command interval

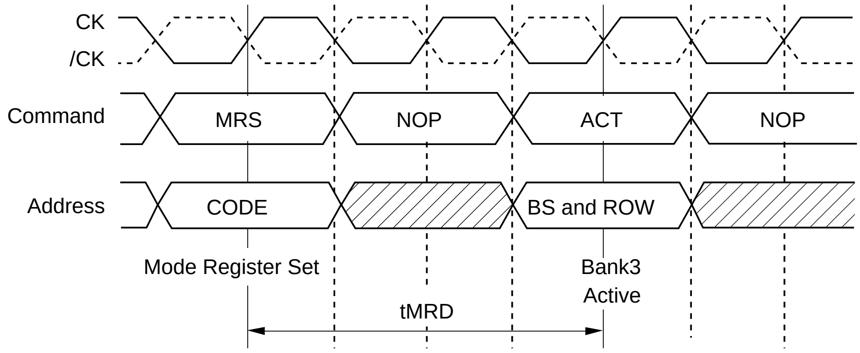
	Destination row of the consecutive ACT command			
	Bank address	Row address	State	Operation
1.	Same	Any	ACTIVE	Two successive ACT commands can be issued at tRC interval. In between two successive ACT operations, precharge command should be executed.
2.	Different	Any	ACTIVE	Precharge the bank. tRP after the precharge command, the consecutive ACT command can be issued.
			IDLE	tRRD after an ACT command, the next ACT command can be issued.



Bank Active to Bank Active

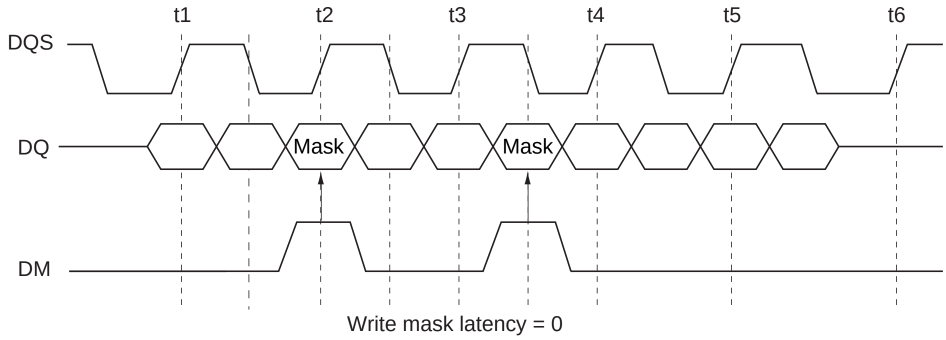
Mode register set to Bank-active command interval

The interval between setting the mode register and executing a bank-active command must be no less than tMRD.



DM Control

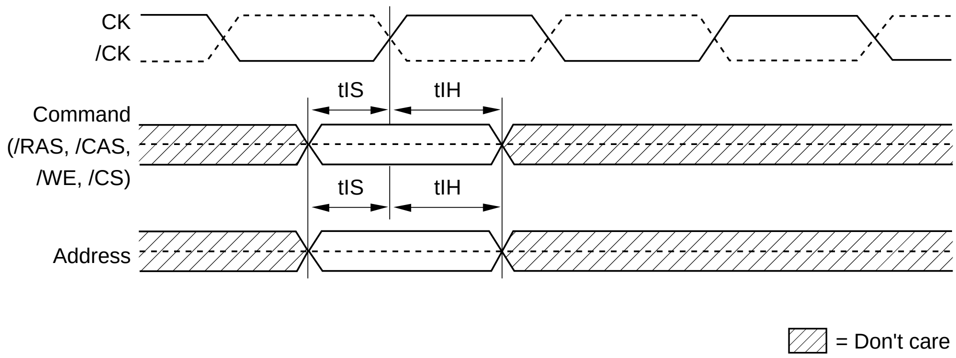
DM can mask input data. By setting DM to low, data can be written. UDM and LDM can mask the upper and lower byte of input data, respectively. When DM is set to high, the corresponding data is not written, and the previous data is held. The latency between DM input and enabling/disabling mask function is 0.



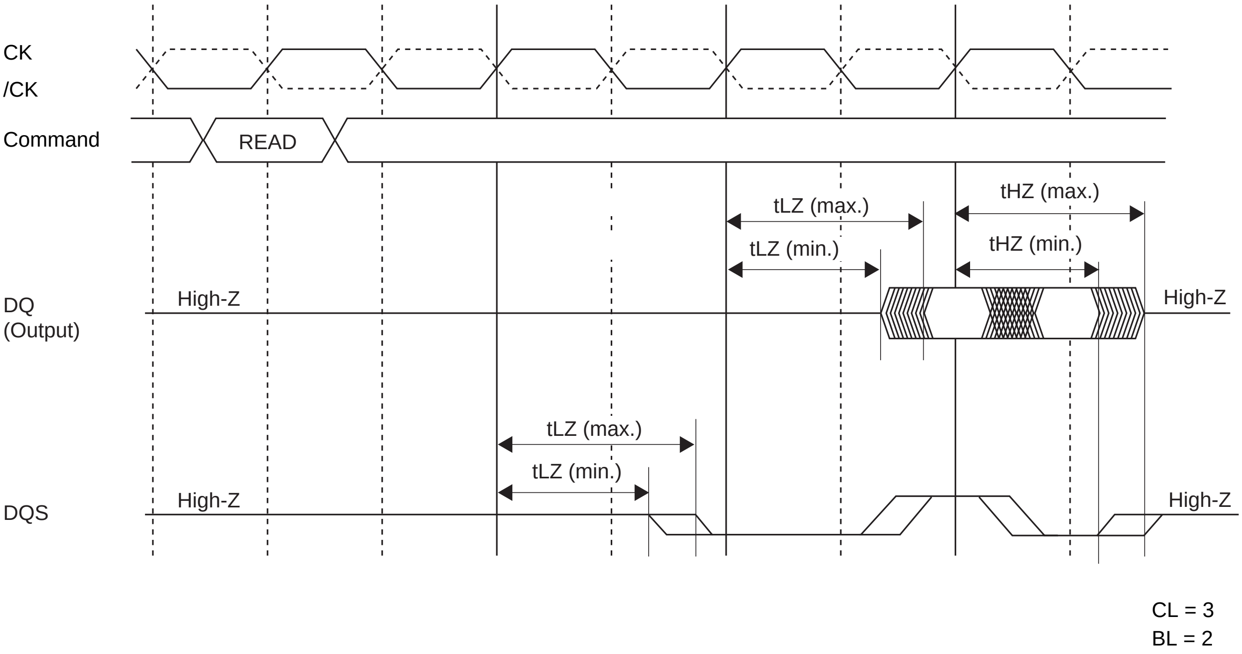
DM Control

Timing Waveforms

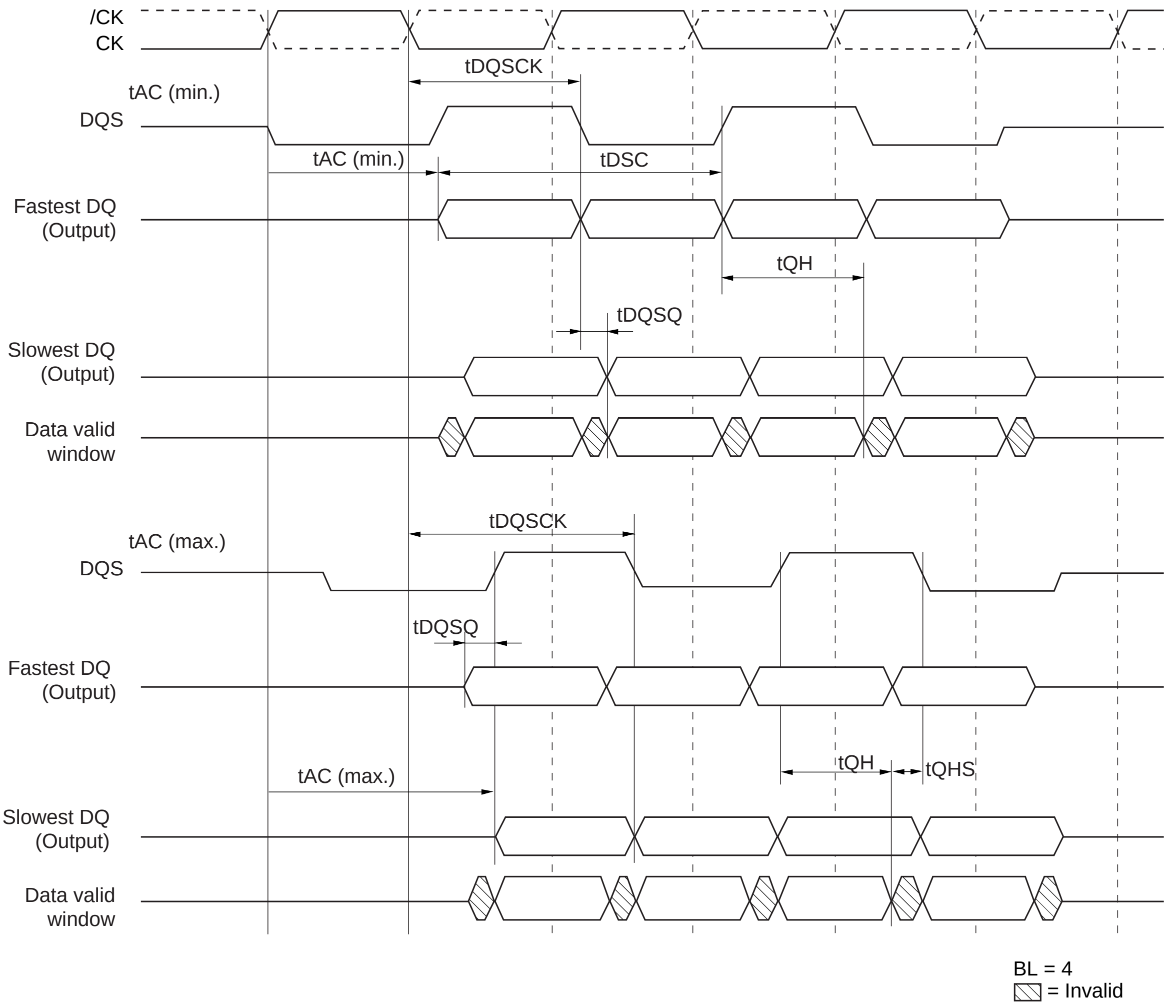
Command and Addresses Input Timing Definition



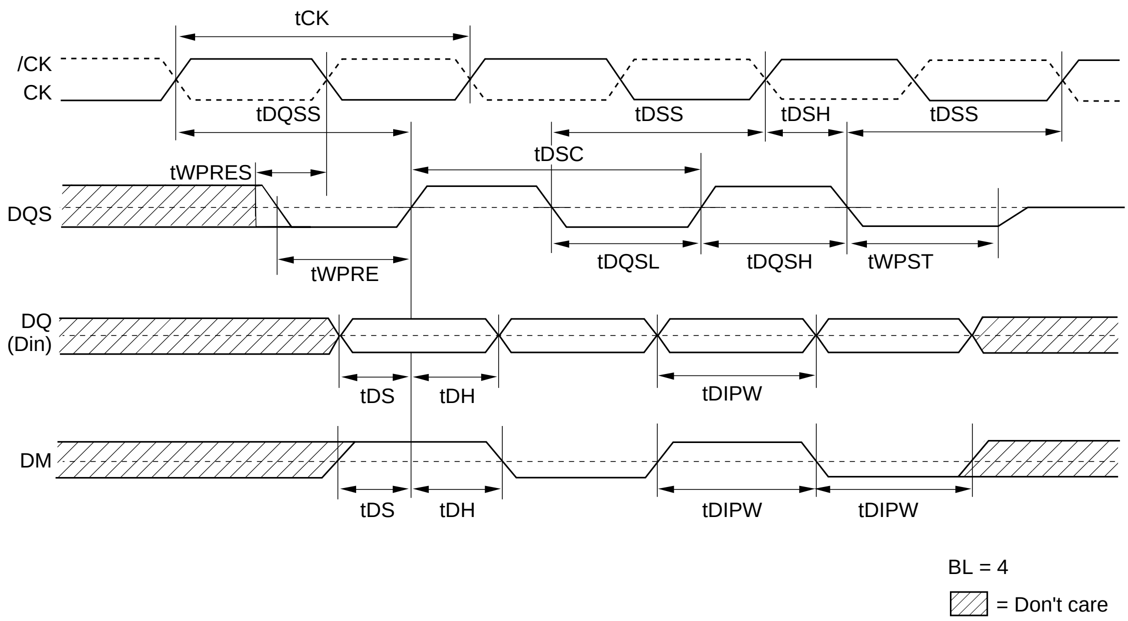
Read Timing Definition (1)



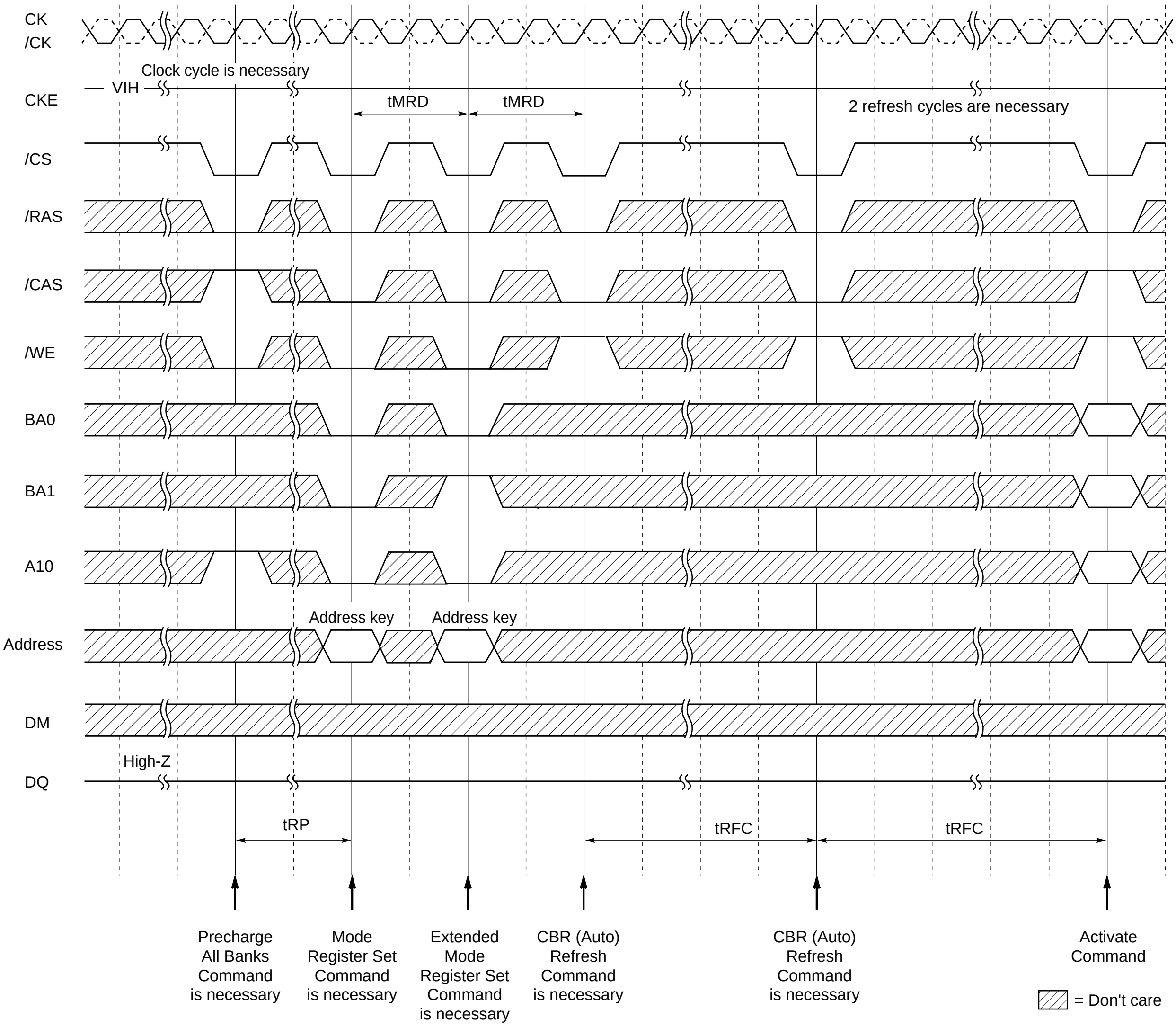
Read Timing Definition (2)



Write Timing Definition

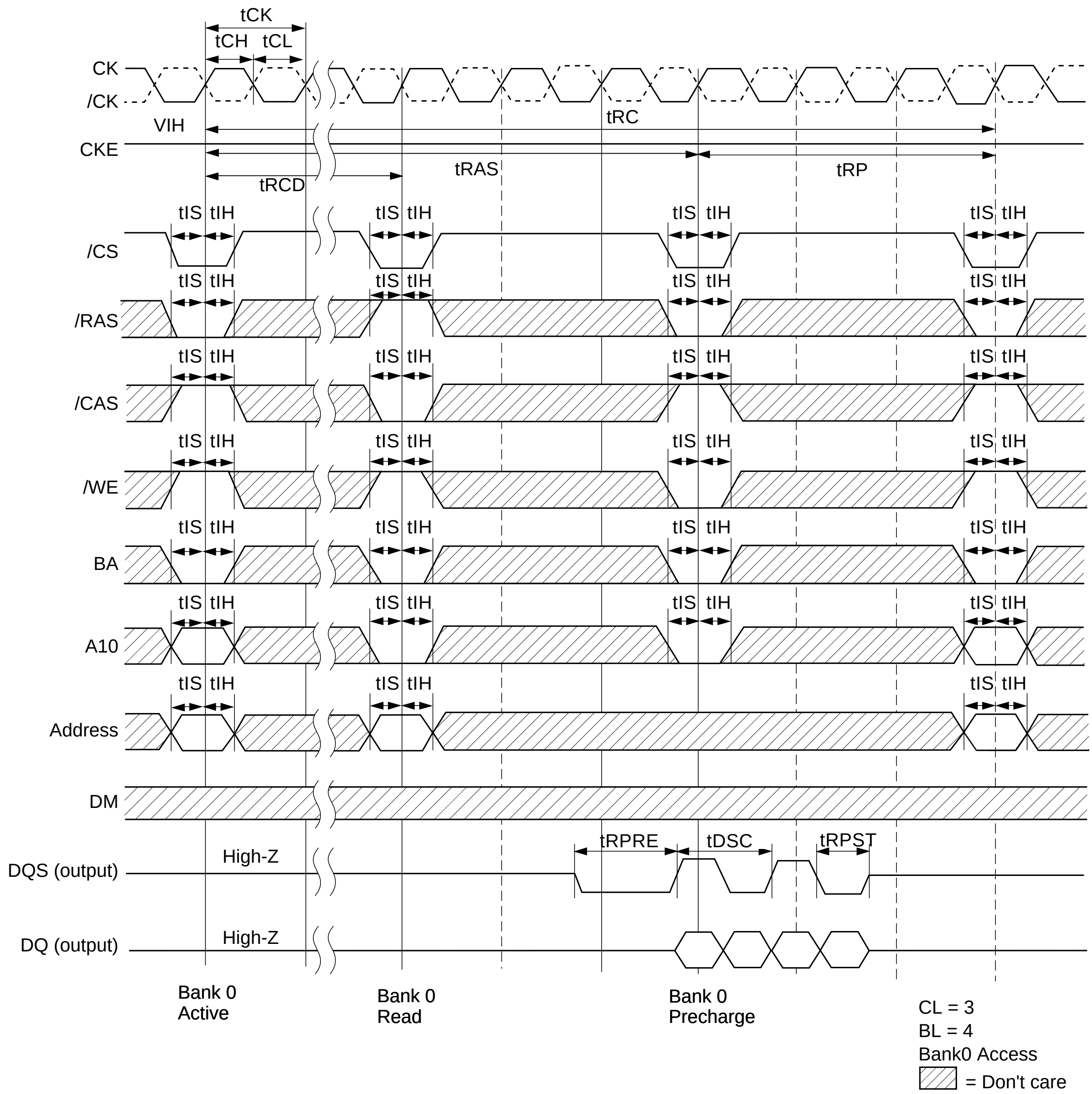


Power on Sequence*

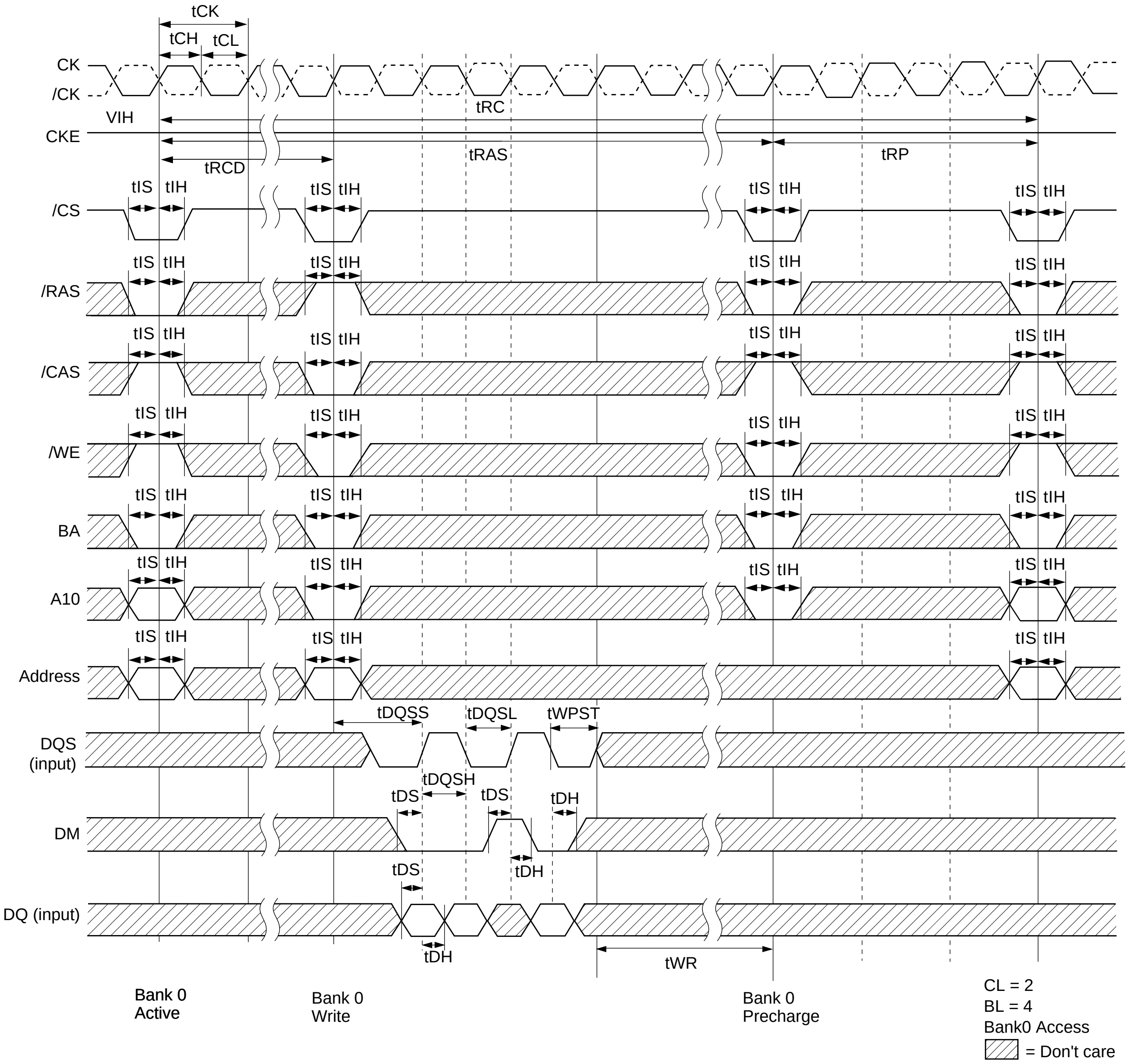


Note: The sequence of auto refresh, mode register programming and extended mode register programming above may be transposed.

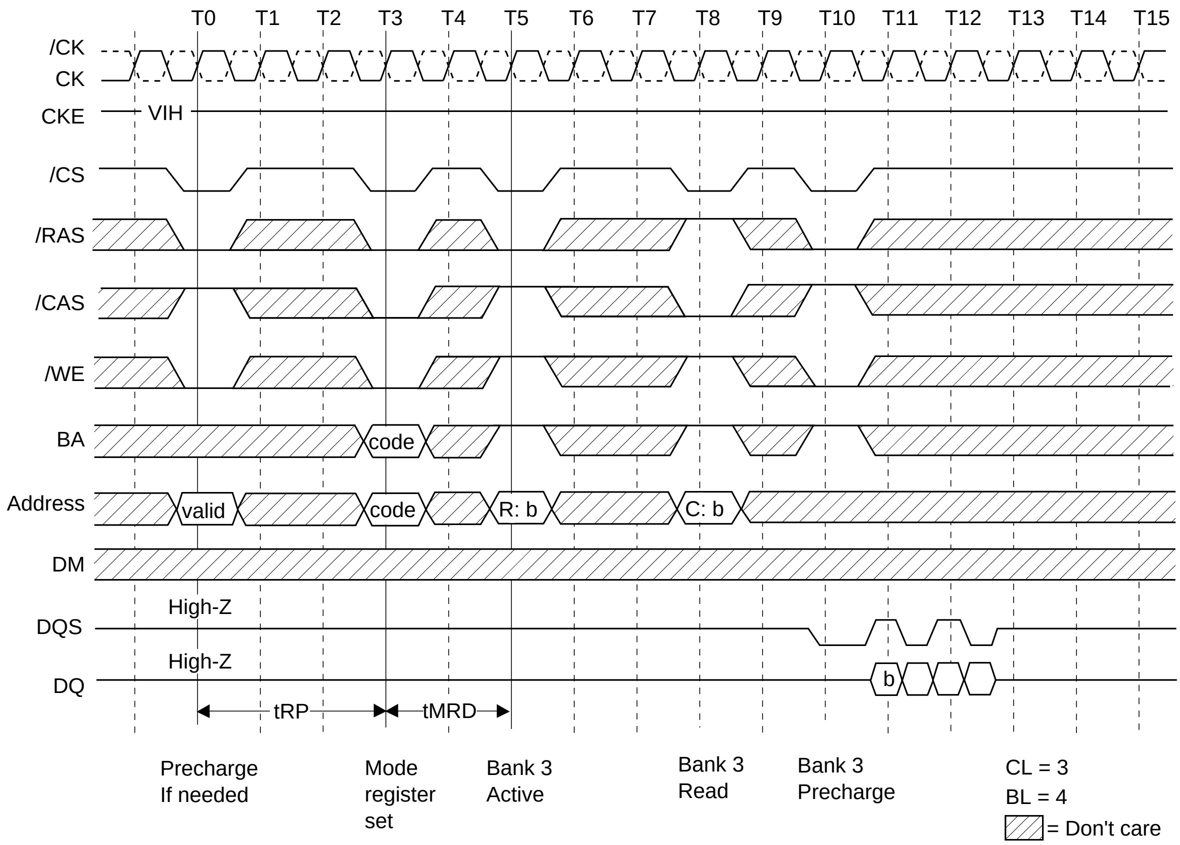
Read Cycle


tCK
tCH tCL
CK
/CK
VIH
tRC
CKE
tRAS
tRP
tRCD
tIS tIH
/CS
/RAS
/CAS
/WE
BA
A10
Address
DM
DQS (output)
High-Z
tRPRE
tDSC
tRPST
DQ (output)
High-Z
Bank 0
Active
Bank 0
Read
Bank 0
Precharge
CL = 3
BL = 4
Bank0 Access
= Don't care

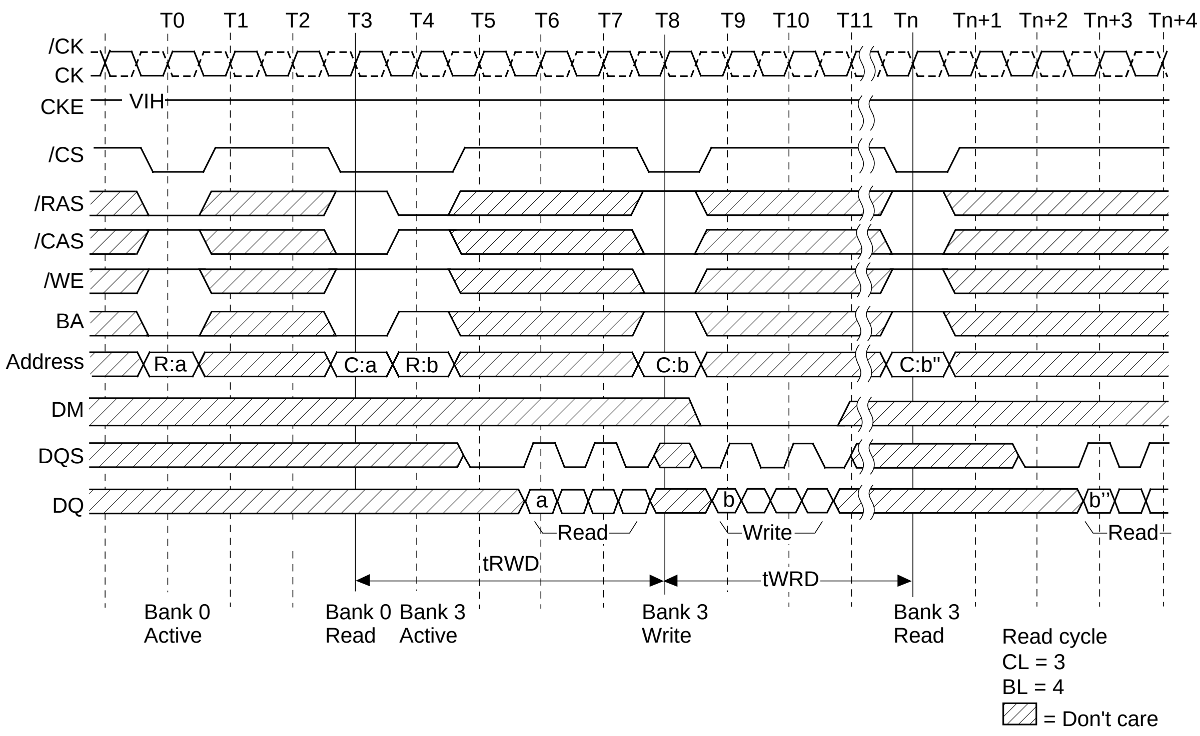
Write Cycle


tCK
tCH
tCL
CK
/CK
VIH
CKE
tRC
tRAS
tRP
tRCD
/CS
/RAS
/CAS
/WE
BA
A10
Address
tIS
tIH
DQS
(input)
tDQSS
tDQSL
tWPST
tDQSH
DM
tDS
tDH
DQ (input)
tWR
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CL = 2
BL = 4
Bank0 Access
= Don't care

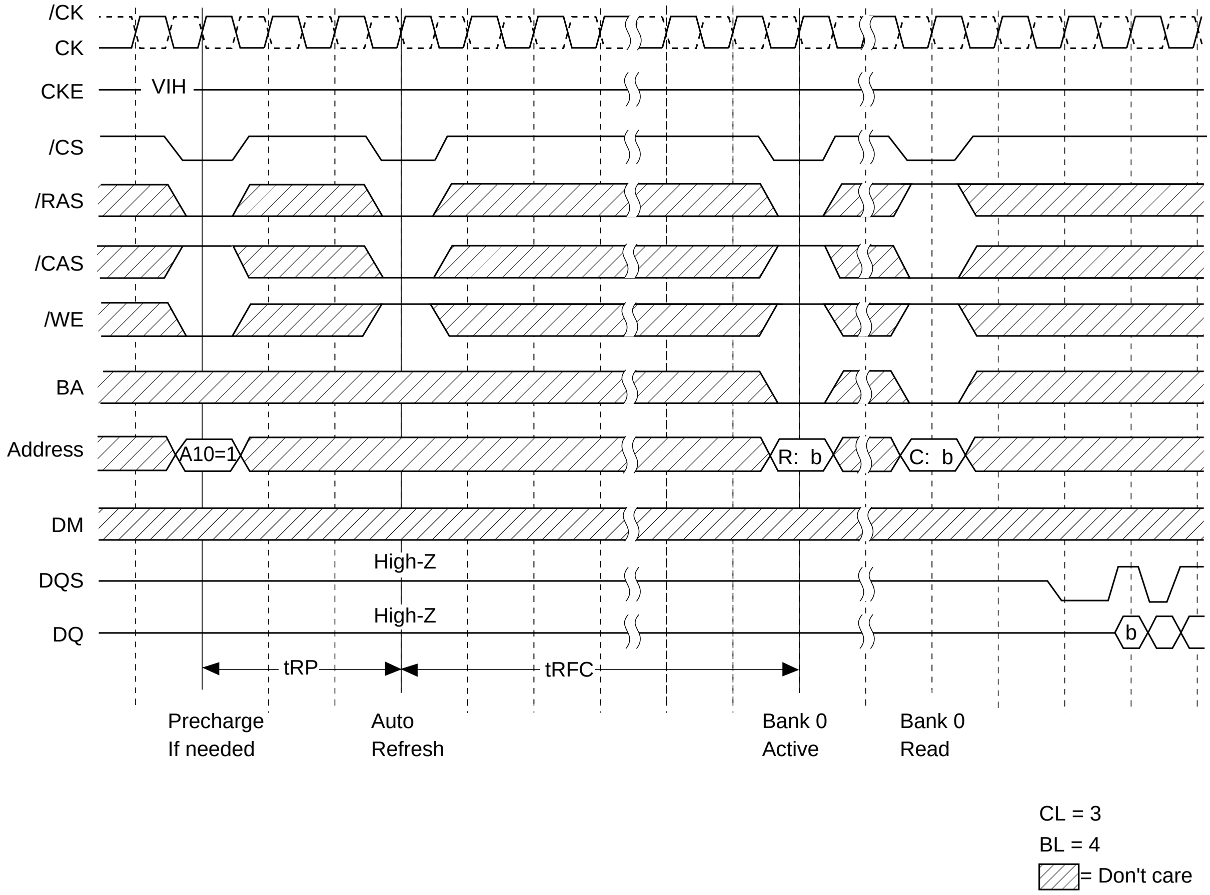
Mode Register Set Cycle



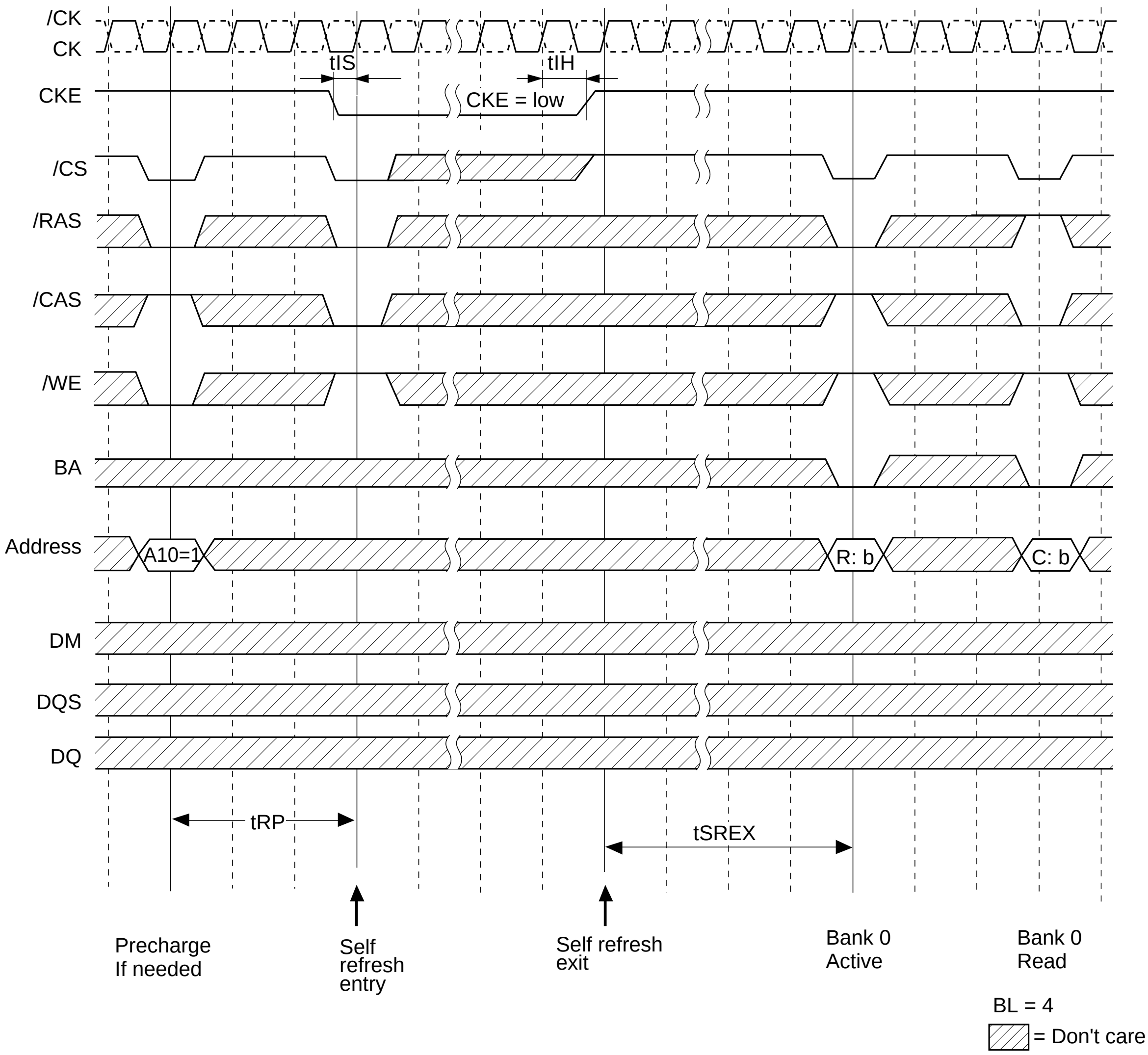
Read/Write Cycle



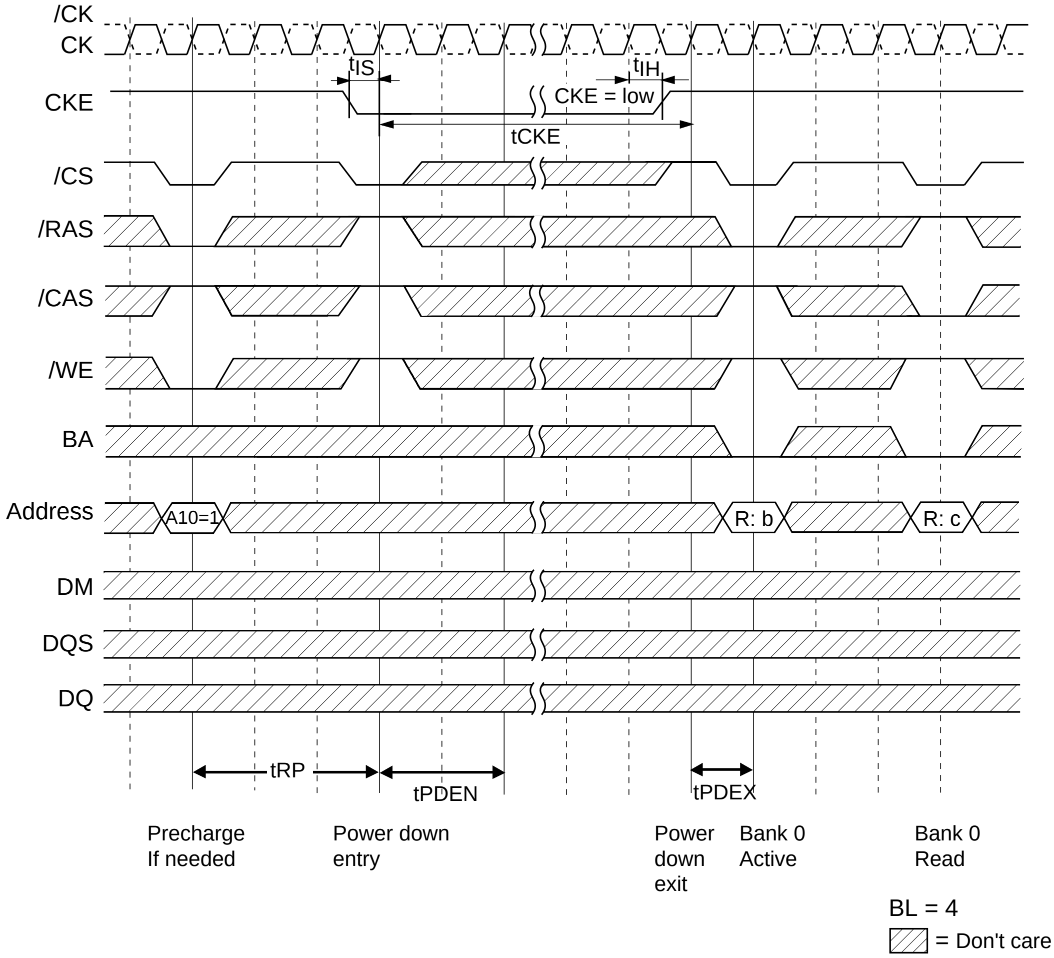
Auto Refresh Cycle



Self-Refresh Cycle



Power Down Entry and Exit

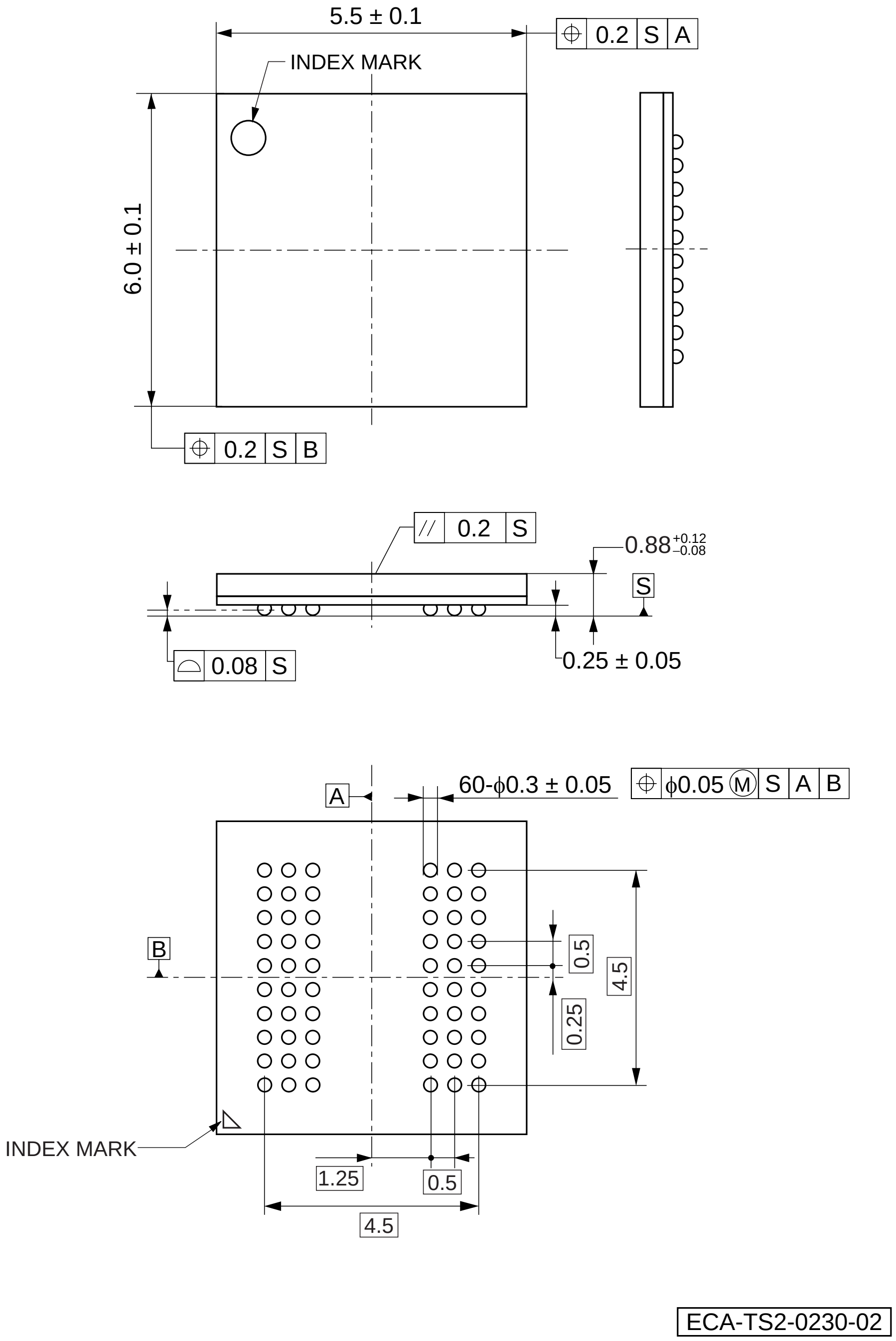


Package Drawing

60-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDK1216CFBJ.

Type of Surface Mount Device

EDK1216CFBJ: 60-ball FBGA < Lead free (Sn-Ag-Cu) >

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Product usage]
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[Usage environment]

Usage in environments with special characteristics as listed below was not considered in the design.
Accordingly, our company assumes no responsibility for loss of a customer or a third party when used in environments with the special characteristics listed below.

Example:
1) Usage in liquids, including water, oils, chemicals and organic solvents.
2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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M01E0706