One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Direct Digital Synthesizers in Clocking Applications
Time Jitter in Direct Digital Synthesizer-Based Clocking Systems

by David Brandon

This application note describes the Time Jitter performance that can be attained by using direct digital synthesizer-based (DDS) clock systems. The importance of frequency planning, output power, and reconstruction filtering in enhancing the jitter performance of these systems is demonstrated.

The primary advantage in using a DDS for clock generation is the extremely fine frequency tuning resolution. The attainable tuning resolution for standard DDS products from ADI is 28 bits, 32 bits, or 48 bits. A 48-bit tuning word results in microhertz of tuning resolution for a 400 MHz system clock. Also, a DDS can be frequency tuned from DC to a maximum of one-half of its internal system clock rate. However, in practice the upper frequency bound is usually limited to ~45% of maximum to accommodate external filtering requirements. Phase tuning resolution, which for clock circuits translates to delay adjust resolution, is typically 14 bits. This correlates to 0.022 degrees of phase offset resolution. In addition, excellent residual phase noise performance is available from a DDS-based clock system.

The primary challenge in using DDS for low jitter clock generation is mitigating the deterministic time jitter that is generated due to the discrete spurious components that are present on the DDS output signal.

To expand on this point, the process of generating a square wave for clocking from a DDS needs to be understood. Figure 1 shows ideal time and frequency domain representations at each point in the process. A real-world representation of the frequency domain is shown at the bottom of Figure 1.

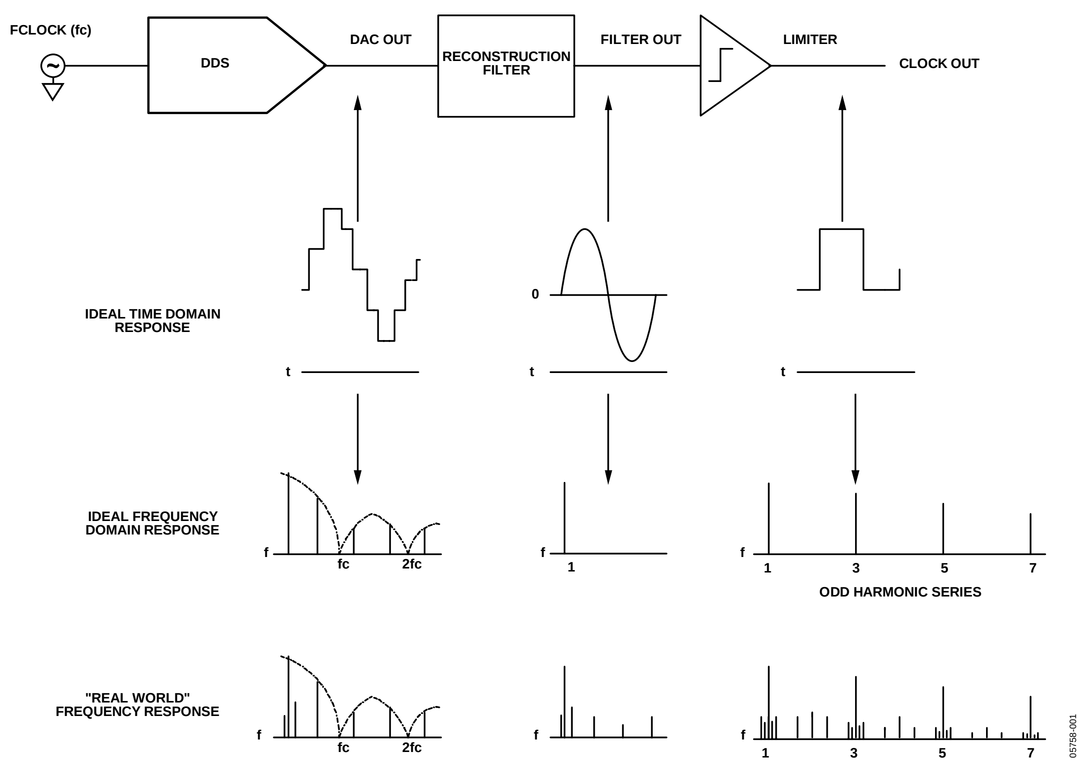

Figure 1. The Process of Generating a Clock from a DDS

As shown, the ideal time domain output of the DDS is a sampled sine wave. The ideal frequency domain representation of a sampled sine wave consists of the fundamental signal and its images. To convert the sampled sine wave into a clock signal, it must be processed in two steps. First, the signal must be filtered, usually a low-pass implementation, to remove the images resulting from the sampling process. Although not a perfect process, the reconstruction filter nominally converts the signal into a pure sine wave, as shown. The corner frequency of this low-pass filter is typically set at about 40% to 45% of the system clock to take advantage of the full tuning bandwidth while also sufficiently attenuating the images. Step two is to convert the filtered sine wave into a square wave by means of a limiter, sometimes referred to as a squaring circuit. The input of the squaring device acts as a comparator that, ideally, switches its output to the desired high or low logic state at the precise instant that the input waveform crosses a threshold voltage. To minimize noise coupling, it is advantageous to have a 2-wire, balanced connection between the DAC output and the limiter input.

As seen in Figure 1, the real-world spectrum of an unfiltered DDS output is rich in spurious content. It contains DAC related harmonic distortion as well as the images of the fundamental frequency. The harmonics of the fundamental are a result of the nonlinearities of the DAC transfer function.

The images of the fundamental reside above the cutoff frequency of the reconstruction filter. However, the harmonics of the fundamental are also reproduced in the images. Images that extend into the 1st Nyquist zone (DC to ½ fc), appear as aliased versions of the harmonics. Thus, the images may appear within the filter pass band. These in band images of the DAC harmonics as well as out-of-band images not sufficiently attenuated by the filter can contribute significantly to the jitter observed on the output of the limiter. The jitter present at the output of the limiter is due to spur-induced, cycle-to-cycle, modulation of the time interval at which the limiter threshold voltage is crossed. The jitter that is generated by this process is classified as deterministic jitter; it is related to the specific frequencies of the spurious content of the signal. The process of spurious components being converted to a phase, or timing error (jitter) via the limiting function is referred to as AM to PM conversion. If the bandwidth of the filter is reduced, either by using a low-pass filter with a reduced cutoff frequency, or a band-pass filter, the amount of spurious noise is reduced. Bandwidth limiting this spurious noise in turn reduces the magnitude of time jitter that is produced.

The magnitude of the time jitter produced is proportional to the magnitude of the spurious components with respect to the slew rate of the fundamental signal. Because the DDS output is a sine wave, its slew rate is proportional to the signal frequency and amplitude. Noise coupling between the DAC output and the limiter input, including device noise from the limiter itself, can also contribute to increased jitter. In general, increased slew rate at the input to a limiter translates to less sensitivity to jitter induced by coupled noise. Because slew rate is proportional to frequency and amplitude, an increase in either parameter tends to improve jitter performance.

The key points in minimizing jitter in DDS-based clock systems are maximizing the DAC output slew rate and implementing effective filtering of the DDS spurious components. The following series of bench data illustrates these points.

The circuit configuration in Figure 2 shows a DDS-based clock generator, consisting of a DDS followed by a reconstruction filter and an AD9515 clock distribution device, used to provide the sampling clock for an analog-to-digital converter (ADC). The DDS sampling clock is derived from a Rohde and Schwarz SMA signal generator. Data was taken on two different DDSs, the AD9958 and the AD9858. The jitter measurement was made by using the clock derived by the DDS and the AD9515 to encode an ADC that subsamples a clean 170 MSPS sine wave. The ADC used in this test is the AD6645, a 14-bit, 100 MSPS device. By evaluating the contribution of the ADC's differential nonlinearity and the thermal noise to the measured SNR, then applying the DDS-based clock and measuring the SNR, the added jitter attributable to the DDS-based clock can be derived from the following formula.

$$t_{JITTER}\, rms = \frac{\left(\sqrt{\left(10^{\frac{-SNR}{20}}\right)^2}\right) - \left(\frac{1+\varepsilon}{2^N}\right)}{2\pi f_{IF}}$$

where:

SNR is the high frequency SNR of the ADC.
N is the number of bits from the converter.
ε is the converters average DNL plus thermal noise.
f_{IF} is the IF analog input frequency to the ADC.

Further details on this formula and its use for evaluating the jitter on ADC sampling clocks can be found in ADI Application Note AN-501.

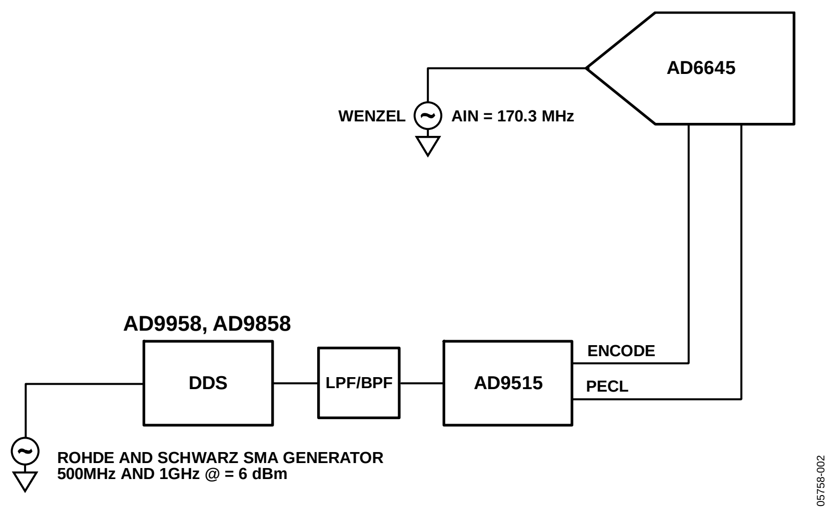

Figure 2. DDS-Based Clock Generator and Jitter Measurement Circuit

DISCUSSION OF TESTS AND RESULTS

Using the configuration in Figure 2, a series of jitter measurements was taken to quantify the effects of filtering and frequency planning.

Jitter data was taken for three frequencies. At each of these frequencies three different filter configurations were used to demonstrate the impact of slew rate (frequency) and bandwidth limiting on the measured jitter. The power of the output level for each setting is also shown in order to monitor the slew rate at the limiter input for each test condition.

The nominal filter bandwidth is set to about 40% of the sampling rate, a general rule for setting the corner frequency in wideband DDS applications. For applications that do not need the wide bandwidth range, the filter bandwidth is then set such that the corner frequency is just above the highest output frequency needed. The intent here is to achieve an improvement in the jitter performance at the expense of tuning bandwidth. Last, Figure 2 shows the jitter when a 5% band-pass filter is used. The most filtering of wideband noise and spurious is obtained in this case and thus the best jitter performance, but most of the tuning bandwidth is sacrificed. In clock applications where the frequency remains constant, this drawback is of no concern.

Table 1 shows data for the AD9958 tests. The data confirms that better jitter performance is achieved as the frequency, or slew rate, is increased and as the filtering pass band is decreased.

Jitter ranges from about 4 ps rms for a 38.88 MHz output with a low-pass filter just below Nyquist, to 700 fs rms jitter for a 155 MHz output with a 5% filter. In each case the AD9515 maintains the jitter performance of the signal as its output is divided down. This is a key attribute of the AD9515 and similar products (see Table 4) as it enables, in combination with a DDS, sub-ps jitter performance down to frequencies as low as 19 MHz. Note that this would be difficult to do if a DDS were to attempt to drive a squaring device directly at 19 MHz due to the slew rate effects mentioned previously.

To further confirm the strong dependence on slew rate, additional data is taken with the AD9858 DDS (Table 2), which is capable of delivering 40 mA of output current to a 50 Ω load. This enables an increased output power relative to a 50 Ω load and the associated greater slew rate.

The AD9958 and AD9959 are multichannel DDS devices, and their outputs can be summed together to increase output power.

Table 1. Jitter Response AD9958 and AD9515 vs. Fout, Power, Frequency and Filter BW

Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Divider Output Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9958/AD9515	500	38.88	−3.6	200 LPF	1	38.88	4.1
AD9958/AD9515	500	38.88	−3.6	200 LPF	2	19.44	4.1
AD9958/AD9515	500	38.88	−4.7	47 LPF	1	38.88	2.4
AD9958/AD9515	500	38.88	−4.7	47 LPF	2	19.44	2.4
AD9958/AD9515	500	38.88	−3.3	5% BPF	1	38.88	1.5
AD9958/AD9515	500	38.88	−3.3	5% BPF	2	19.44	1.5
AD9958/AD9515	500	77.76	−3.8	200 LPF	1	77.76	2.5
AD9958/AD9515	500	77.76	−3.8	200 LPF	2, 4	38.88, 19.44	2.5
AD9958/AD9515	500	77.76	−4.9	85 LPF	1	77.76	1.5
AD9958/AD9515	500	77.76	−4.9	85 LPF	2, 4	38.88, 19.44	1.5
AD9958/AD9515	500	77.76	−3.8	5% BPF	1	77.76	1.1
AD9958/AD9515	500	77.76	−3.8	5% BPF	2, 4	38.88, 19.44	1.1
AD9958/AD9515	500	155.52	−5.5	200 LPF	2	77.76	1.5
AD9958/AD9515	500	155.52	−5.5	200 LPF	4, 8	38.88, 19.44	1.5
AD9958/AD9515	500	155.52	−5.6	5% BPF	2	77.76	0.68
AD9958/AD9515	500	155.52	−5.6	5% BPF	4, 8	38.88, 19.44	0.68

Table 2 shows the AD9858 with a 5% band-pass filter, a 225 MHz low-pass filter, and various levels of DDS output power. As expected, better jitter is achieved as power is increased and bandwidth reduced. With a 5% band-pass filter, the majority of spurs from the DAC are attenuated. The jitter in this case is much more dependent on noise coupling between the DAC output and limiter input; this is proven by the strong correlation between jitter improvement and increased slew rate.

This data also indicates that better jitter performance is attained with the AD9858 relative to the AD9958 for similar levels of power and bandwidth. There are differences in spurious performance of DDSs that result in varying levels of jitter performance. When selecting a DDS for a clocking application, generally the device with best SFDR provides the best jitter performance. The AD9858 is also sampling at a much higher rate than the AD9958, so the images of the fundamental and lower order harmonics are further into the stop band of the reconstruction filter's frequency response.

Getting the required stop-band attenuation, as well as overall performance from the DAC reconstruction filters is nontrivial. Filter component parasitics and PCB board layout effects can impact the idealized filter response characteristics. Impaired stop-band attenuation and the resulting out-of-band noise feed-through result in degraded jitter performance.

Table 2. Jitter Response AD9858 and AD9515 vs. Fout, Power, Frequency and Filter BW

Product	DDS Sample Rate (MHz)	DDS Output Frequency (MHz)	DDS Output Power (dBm)	DDS Reconstruction Filter (MHz)	AD9515 Output Divider Setting	AD9515 Output Frequency (MHz)	Jitter (rms) (ps)
AD9858/AD9515	1000	155.52	+7.7	225 LPF	2	77.76	0.56
AD9858/AD9515	1000	155.52	+7.7	225 LPF	4,8	38.88, 19.44	0.56
AD9858/AD9515	1000	155.52	+7.7	5% BPF	2	77.76	0.33
AD9858/AD9515	1000	155.52	+7.7	5% BPF	4, 8	38.88, 19.44	0.33
AD9858/AD9515	1000	155.52	+2.6	225 LPF	2	77.76	0.63
AD9858/AD9515	1000	155.52	+2.6	225 LPF	4, 8	38.88, 19.44	0.63
AD9858/AD9515	1000	155.52	+1.1	5% BPF	2	77.76	0.42
AD9858/AD9515	1000	155.52	+1.1	5% BPF	4, 8	38.88, 19.44	0.42
AD9858/AD9515	1000	155.52	−3.2	225 LPF	2	77.76	0.73
AD9858/AD9515	1000	155.52	−3.2	225 LPF	4, 8	38.88, 19.44	0.73
AD9858/AD9515	1000	155.52	−4.6	5% BPF	2	77.76	0.64
AD9858/AD9515	1000	155.52	−4.6	5% BPF	4, 8	38.88, 19.44	0.64

TERMINOLOGY

Time Jitter

For the purposes of this application note the term jitter refers to time jitter. Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings is seen to vary. In a square wave, the time jitter is seen as a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) which corresponds to the area under a normal probability density function spanning one standard deviation around the mean.

DDS

For the purpose of this application note the term, DDS denotes the combination of a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC).

Table 3. ADI High Frequency DDS Product Portfolio

DDS Product Selection	Max Sample Rate (MHz)	Frequency Tuning Resolution (Bits)	DAC Full Scale Current (mA)	DAC Resolution (Bits)	Number of Output Channels
AD9858	1000	32	40	10	1
AD9958	500	32	10	10	2
AD9959	500	32	10	10	4
AD9956	400	48	15	14	2
AD9540	400	48	15	10	2
AD9859	400	32	15	10	1
AD9951	400	32	15	14	1
AD9952	400	32	15	14	1
AD9953	400	32	15	14	1
AD9954	400	32	15	14	1
AD9852	300	48	20	12	1
AD9854	300	48	20	12	2
AD9851	180	32	20	10	1
AD9850	125	32	20	10	1
AD9830	50	32	20	10	1

Table 4. ADI Clock Distribution Product Portfolio

Divider Product Selection	Max Input Frequency (MHz)	Max Output Frequency (MHz)	Integer Divide Ratio	Number of Output Channels	Output Levels (Vary per Channel)
AD9515	0 to 1600	0 to 1600	1 to 32	2	LVDS/CMOS/LVPECL
AD9514	0 to 1600	0 to 1600	1 to 32	3	LVDS/CMOS/LVPECL
AD9513	0 to 1600	0 to 800	1 to 32	3	LVDS/CMOS
AD9512	0 to 1600	0 to 1200	1 to 32	5	LVDS/CMOS/LVPECL
AD9511	0 to 1600	0 to 1200	1 to 32	5	LVDS/CMOS/LVPECL
AD9510	0 to 1600	0 to 1200	1 to 32	8	LVDS/CMOS/LVPECL

NOTES

NOTES

AN05758-0-2/06(0)