DATA SHEET

MOS INTEGRATED CIRCUIT

μPD16309

64bit DC-PDP COLUMN DRIVER ICs

DESCRIPTION

The uPD16309 is a Column driver utilized high voltage CMOS process for DC plasma display panel. It consists of a 64bit bi-directional shift-register, 64bit transparent latch and high voltage P channel MOS FETs (Open Drain Output).
It operates 5V (CMOS input level) and drives High Voltage of 200V. (Open drain output)

FEATURES

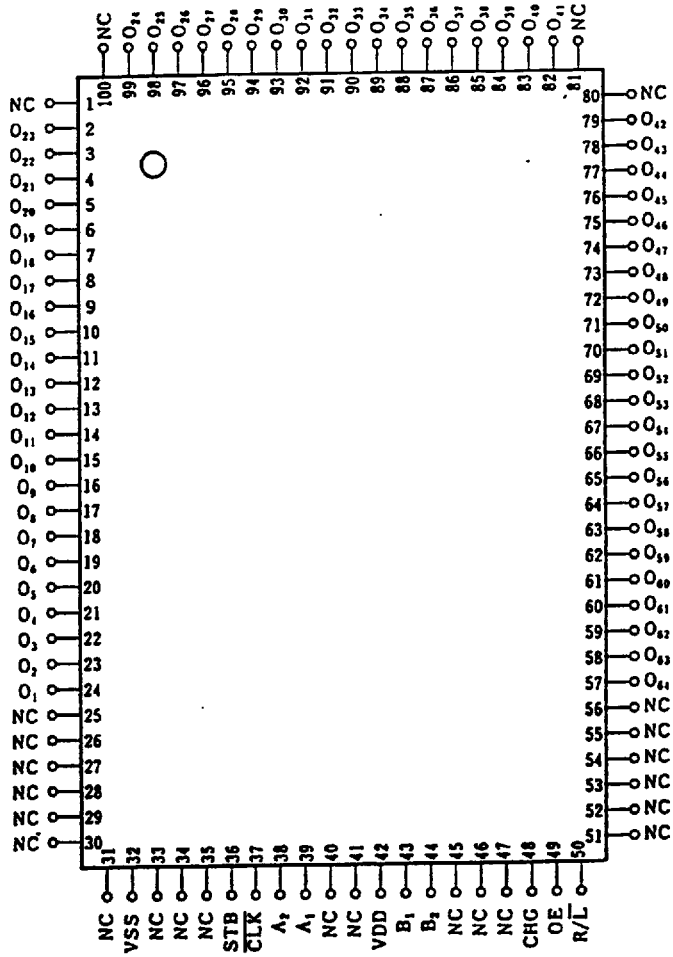
- High Voltage Pch MOS FETs + CMOS structure
- 200V High Voltage Source Driver
- High Speed Data Transferring Rate (f_{max}=10MHz)
- 64bit Bi-directional Shift-register
- Low Power Consumption (I_{DD}=1mA max. Ta=-40 to +85°C)
- Wide Operating Temperature (-40 to +85°C)

ORDER INFORMATION

Part No.	Package	Quarity Level
uPD16309GF-3BA	100pin Plastic QFP (3 sided, 14 x 20)	Standard

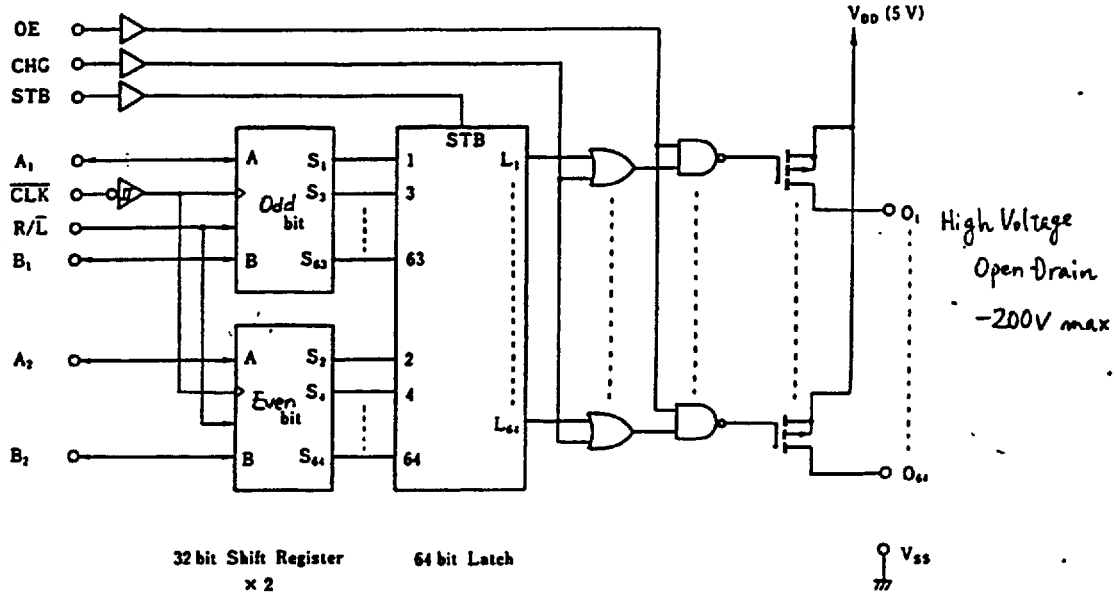
D1

PIN CONNECTION DIAGRAM (Top View)



Please open the No. 40 pin because of connecting lead frame.

BLOCK DIAGRAM



D2

PIN CONFIGURATION

SYMBOL	PIN NAME	PIN No.	EXPLANATION
CLK	Shift Clock Input	37	Data is read and shifted while CLK is going high level to Low level.
STB	Latch Strobe Input	36	When STB is high level, Data of shift register are read to Latch circuit.
A_1 A_2	Right Data Input/Output	39 38	Data Input / Output Terminals R/L=H ; $A_1 \rightarrow O_1 \rightarrow O_3 \cdots O_{61} \rightarrow O_{63} \rightarrow B_1$; $A_2 \rightarrow O_2 \rightarrow O_4 \cdots O_{62} \rightarrow O_{64} \rightarrow B_2$ R/L=L ; $B_1 \rightarrow O_{63} \rightarrow O_{61} \cdots O_3 \rightarrow O_1 \rightarrow A_1$; $B_2 \rightarrow O_{64} \rightarrow O_{62} \cdots O_4 \rightarrow O_2 \rightarrow A_2$
B_1 B_2	Left Data Output/Input	43 44	
R/L	Shift Direction Control Input	50	
O_1-O_{64}	Driver Outputs	2-24, 57-79, 82-99	High Voltage Outputs -200V, -3mA max
OE	Output Enabel Input	49	OE=H; O_1-O_{64} are output data. OE=L; O_1-O_{64} are High Impedance. (Driver OFF)
CHG	Output Charge Input	48	While CHG is high level, All drivers are turned on.
V_{DD}	Power Supply	42	4.5V - 5.5V
V_{SS}	Ground	32	Connect to system ground.
NC	Non Connect	1, 25-31, 33-35 40, 41, 45-47 51-56, 80, 81, 100	Please open the No. 40 pin.

TRUTH TABLE1 (SHIFT-REGISTER)

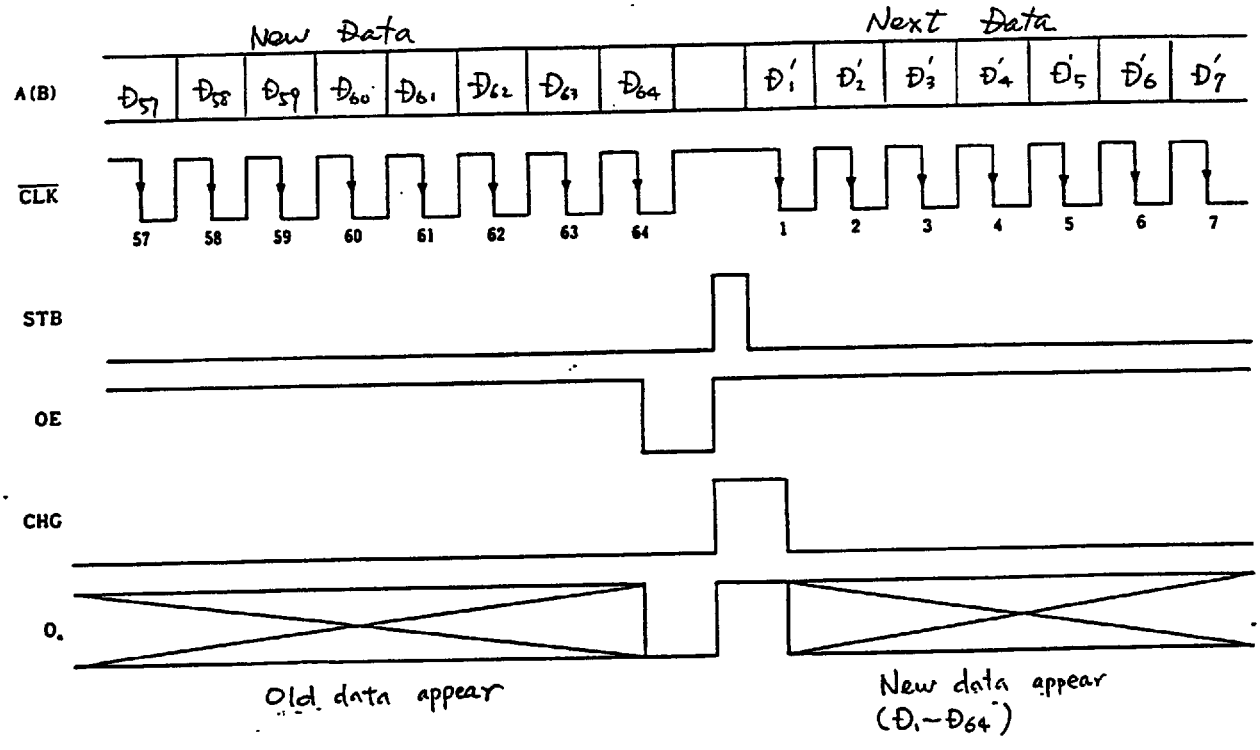
INPUT		INPUT/OUTPUT		SHIFT-REGISTER STATUS
R/L	CLK	A	B	
H	↓	IN	OUT	RIGHT SHIFT (1 → 64)
H	↑			No CHANGE
L	↓	OUT	IN	LEFT SHIFT (64 → 1)
L	↑			No CHANGE

TRUTH TABLE2 (DRIVER)

DATA	STB	CHG	OE	DRIVER OUTPUTS
×	×	×	L	Z (All drivers are turned off.)
×	×	H	H	H (All drivers are turned on)
L	H	L	H	Z (A driver is turned on)
H	H	L	L	H (A driver is turned off)
×	L	L	H	Outputs are continued the status when STB is high level.

"DATA" is the data in shift-register.

TIMING CHART (Using Only one μPD16309)



ABSOLUTE MAXIMUM RATINGS (Ta=25℃, V_{SS}=0V)

Power Supply Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to VDD+0.5	V
Logic Output Voltage	V_{O1}	−0.5 to VDD+0.5	V
Driver Output Voltage	V_{O2}	−200 to VDD+0.5	V
Driver Current	I_{O2}	−3	mA
Power Dissipation/Package	P_D	1000*	mW
Operating Temperature	$T_{opt.}$	−40 to +85	℃
Storage Temperature	$T_{stg.}$	−65 to 150	℃

* For Ta above 25℃, derate linearly at the rate of -8mW/℃.

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
High Level Input Voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	0		0.2V_{DD}	V	
Driver Output Voltage	V_{O2}	-180		V_{DD}	V	
Driver Output Current	I_{O2}			-1.2	mA	

ELECTRICAL CHARACTERISTICS (T_a=-40 to +85℃, V_{DD}=4.5 to 5.5V, V_{SS}=0V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Output Voltage	V_{OH1}	0.9V_{DD}			V	Logic Output, I_{OH1}=-1mA
Low Level Output Voltage	V_{OL1}			0.1V_{DD}	V	Logic Output, I_{OL1}=1mA
High Level Output Voltage	V_{OH2}		V_{DD}-0.8	V_{DD}-2	V	O_1-O_{64}, I_{OH2}=-1.2mA
Output Leakage Current	I_{TL}			±10	μA	O_1-O_{64} (Each Output) V_{O2}=-18OV, OE=0V
Input Current	I_I			±1	μA	V_I=V_{DD} or V_{SS}
High Level Input Voltage	V_{IH}	0.7V_{DD}			V	
Low Level Input Voltage	V_{IL}			0.2V_{DD}	V	
Quiescent Supply Current	I_{DD}			100	μA	Ta=25℃
				1.0	mA	Ta=-40 to +85℃

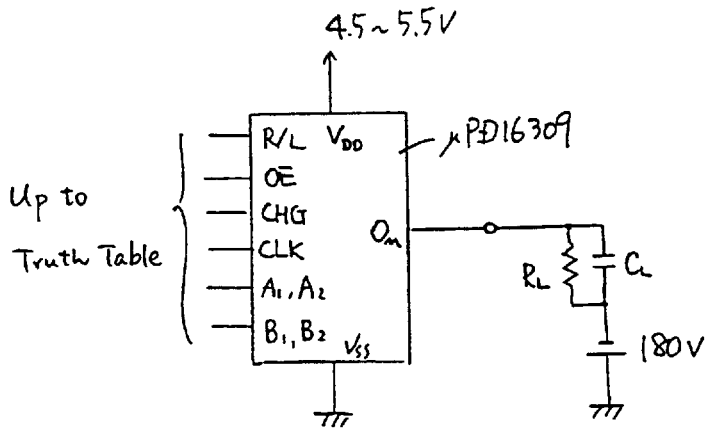
SWITCHING CHARACTERISITICS (T_a=-40 to +85°C, V_{DD}=4.5 to 5.5V, $V_{O2<L>}$=-18OV, C_L=15pF, R_L=91kΩ)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Propagation Delay Time	t_{PHL1}		50	100	ns	CLK to A/B (Serial Output)
	t_{PLH1}		50	100	ns	
	t_{PHZ2}		0.4	2.0	us	CLK to O_1-O_{64}
	t_{PZH2}		0.1	0.8	us	
	t_{PHZ3}		0.4	2.0	us	STB to O_1-O_{64}
	t_{PZH3}		0.1	0.75	us	
	t_{PHZ4}		0.4	2.0	us	CHG to O_1-O_{64}
	t_{PZH4}		0.1	0.7	us	
	t_{PHZ5}		0.4	2.0	us	OE to O_1-O_{64}
	t_{PZH5}		0.1	0.6	us	
Output Rise Time	t_{TZH}		0.3	2.0	us	O_1-O_{64}
Output Fall Time	t_{THZ}		7	20	us	
Maximum Clock Frequency	f_{max}	10			MHz	Duty Cycle=50%
Input Capacitance	C_I		10	15	pF	Ta=25°C

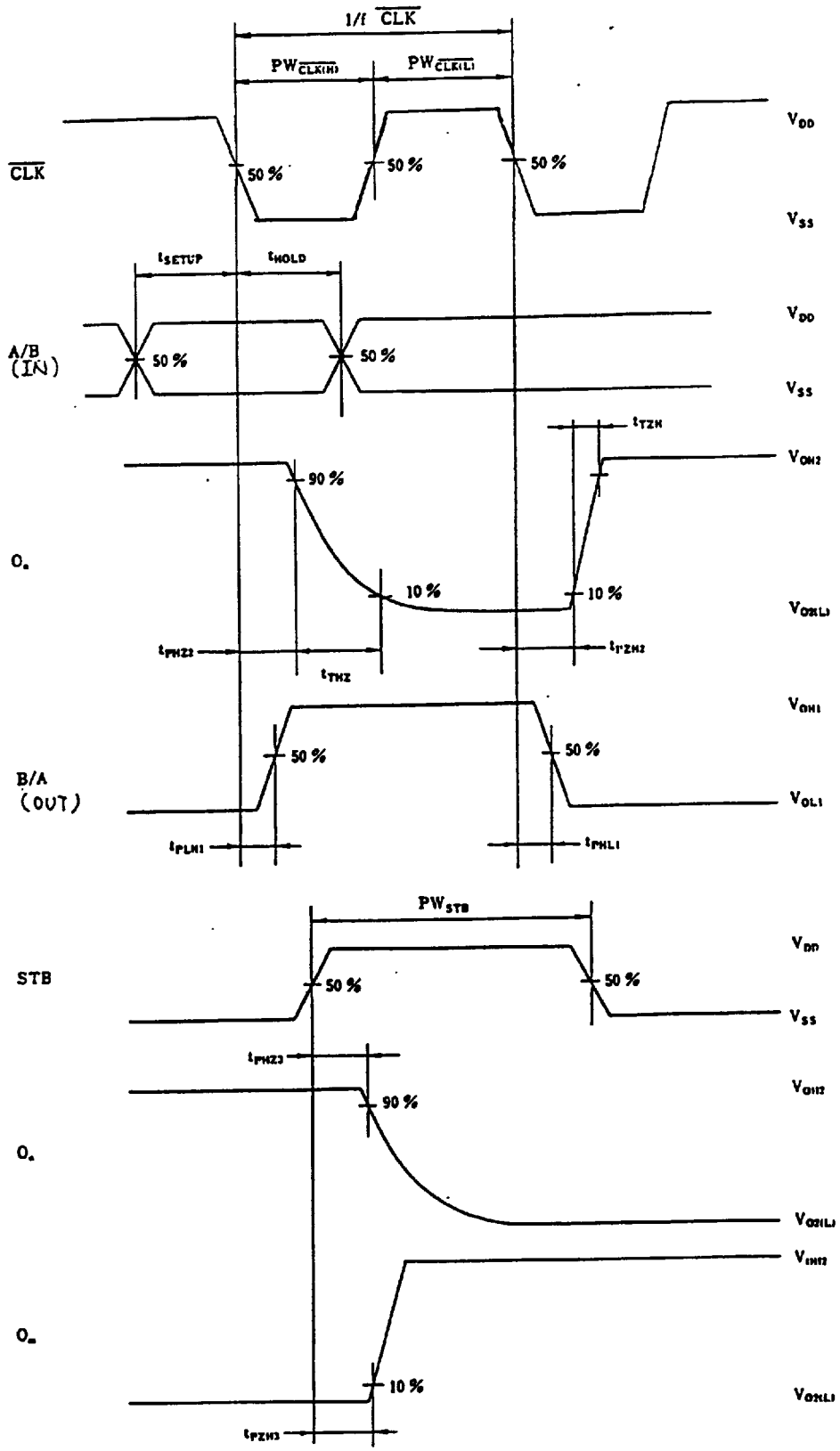
TIMING REQUIREMENT CONDITION (Ta=-40 to +85°C, VDD=4.5 to 5.5V)

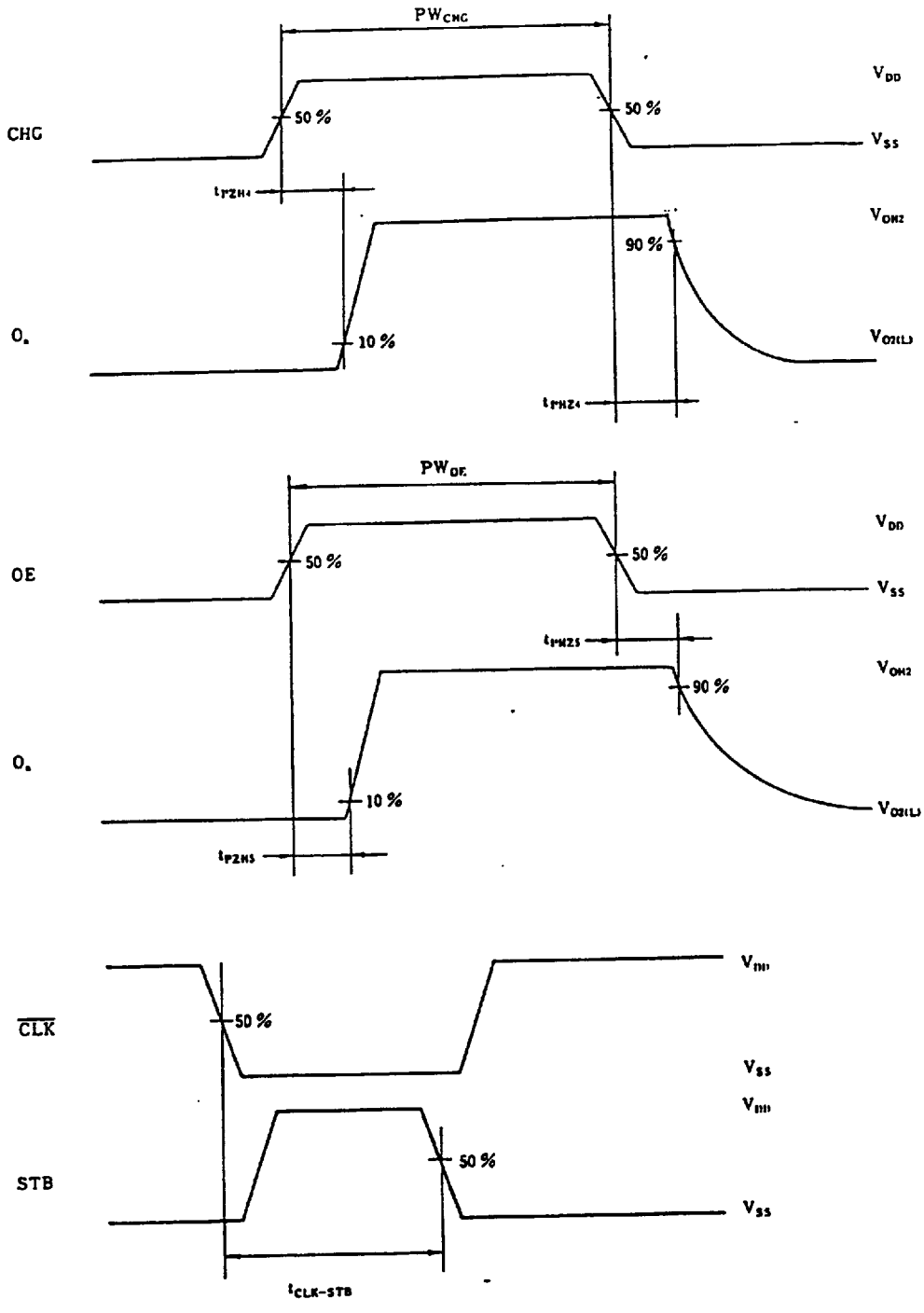
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock Pulse Width	PW_{CLK}	50			ns	
OE Pulse Width	PW_{OE}	2.0			us	
STB Pulse Width	PW_{STB}	50			ns	
CHG Pulse Width	PW_{CHG}	2.0			us	
Data Set Up Time	t_{SETUP}	20			ns	
Data Hold Time	t_{HOLD}	10			ns	
Clock to Strobe Time	$t_{CLK-STB}$	100			ns	

SWITCHING TEST CIRCUIT



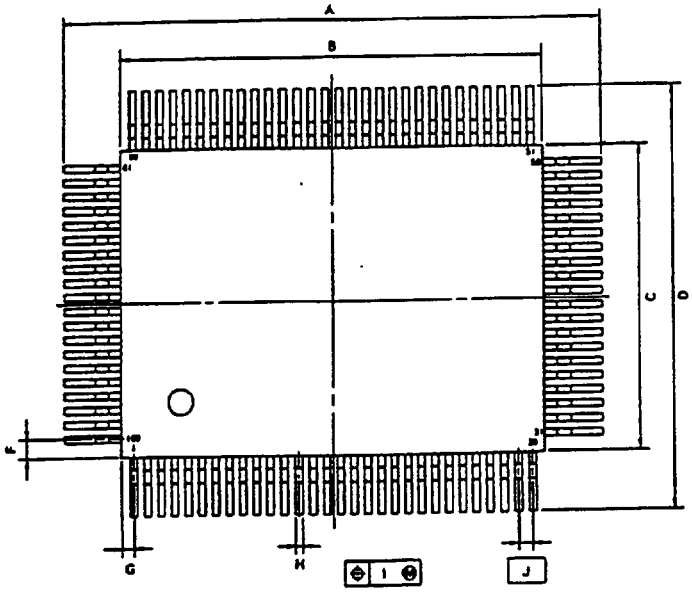
SWITCHING CHARACTERISTICS WAVEFORM



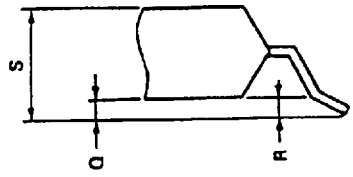


PACKAGE DIMENSIONS

100 Pin Plastic QFP (14 x 20) (unit: mm)



detail of lead end



P100GF-65-3BA-1

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.6^{\pm 0.4}$	$0.929^{\pm 0.016}$
B	$20.0^{\pm 0.2}$	$0.795^{+0.008}_{-0.009}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.008}_{-0.009}$
D	$17.6^{\pm 0.4}$	$0.693^{\pm 0.016}$
F	0.8	0.031
G	0.6	0.024
H	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.