

# CCD area image sensor S9979



## TDI operation / large active area CCD

S9979 is a FFT-CCD area image sensor specifically designed for low-light-level detection in scientific applications. In particular, this image sensor is ideally suited for extremely low-light-level detection in such fields as spectroscopy and astronomy. By operating this image sensor in MPP mode, the dark current can be exceedingly reduced. Moreover, use of the low-noise readout amplifier enables low-light-level detection and long integration time, thus achieving a wide dynamic range. S9979 has an effective pixel size of  $48 \times 48 \mu\text{m}$  and is available in active area of  $73.728 \text{ (H)} \times 6.144 \text{ (V)}$  mm.

### Features

- TDI (Time Delay Integration) operation
- $1536 \text{ (H)} \times 128 \text{ (V)}$  pixel format
- Pixel size:  $48 \times 48 \mu\text{m}$
- 100 % fill factor
- Wide dynamic range: 20000
- Low dark signal:  $2 \text{ ke}^-/\text{pixel/s}$  Typ. (MPP mode)
- Low readout noise:  $60 \text{ e}^- \text{rms}$  Typ.
- MPP operation

### Applications

- Industrial inspection
- Low-light-level detection

### ■ Specification

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm(V)]
S9979	Non-cooled	$1536 \times 128$	$1536 \times 128$	$73.728 \times 6.144$

### ■ General ratings

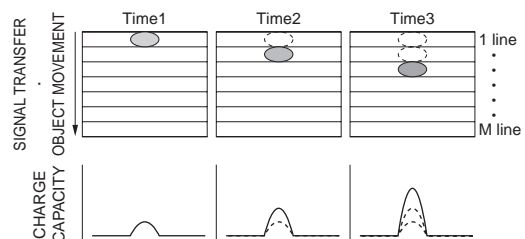
Parameter	Specification
CCD structure	Full frame transfer or TDI
Fill factor	100 %
Number of active pixels	$1536 \text{ (H)} \times 128 \text{ (V)}$
Pixel size	$48 \text{ (H)} \times 48 \text{ (V)} \mu\text{m}$
CCD active area	$73.728 \text{ (H)} \times 6.144 \text{ (V)} \text{ mm}$
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	Two-stage MOSFET source follower with load resistance
Package	28-pin ceramic package
Window *1	Quartz window (standard) Temporarily attached window is available

\*1: Temporary window type (ex. S9979N) and UV coat type (ex. S9979UV) are available upon request.  
Temporary window is fixed by tape to protect the CCD chip and wire bonding.

### What is TDI operation

In FFT-CCD, TDI operation performs continuous imaging of a fast-moving object, by transferring the signals at the same rate as the speed of the moving object. TDI operation allows acquiring continuous, clear images with high S/N and no frame breaks. Since signals of all pixels in each row are accumulated, sensitivity variations can be drastically improved compared to two-dimensional operation.

### ● Signal integration by TDI operation



KMPDC0139EA

**■ Absolute maximum ratings (Ta=25 °C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-30	-	+30	°C
Storage temperature	Tstg	-30	-	+70	°C
OD voltage	VOD	-0.5	-	+20	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
IGV voltage	VIGV	-15	-	+15	V
IGH voltage	VIGH	-15	-	+15	V
SG voltage	VSG	-15	-	+15	V
OG voltage	VOG	-15	-	+15	V
RG voltage	VRG	-15	-	+15	V
TG voltage	VTG	-15	-	+15	V
Vertical clock voltage	VP1AV, VP2AV VP1BV, VP2BV	-15	-	+15	V
Horizontal clock voltage	VP1AH, VP2AH VP1BH, VP2BH	-15	-	+15	V

**■ Operating conditions (MPP mode, Ta=25 °C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	12	15	-	V	
Reset drain voltage	VRD	12	13	14	V	
Output gate voltage	VOG	-0.5	2	5	V	
Output transistor ground voltage	VSSA	-	0	-	V	
Substrate voltage	VSSD	-5	0	-	V	
Test point	Vertical input source	VISV	-	VRD	-	
	Vertical input gate	VIGV	-8	0	-	
	Horizontal input gate	VIGH	-8	0	-	
Vertical shift register clock voltage	High	VP1AVH, VP2AVH VP1BVH, VP2BVH	0	3	6	V
	Low	VP1AVL, VP2AVL VP1BVL, VP2BVL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1AHH, VP2AHH VP1BHH, VP2BHH	0	3	6	V
	Low	VP1AHL, VP2AHL VP1BHL, VP2BHL	-9	-8	-7	
Summing gate voltage	High	VSGH	0	3	6	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	0	3	6	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	0	3	6	V
	Low	VTGL	-9	-8	-7	

**■ Electrical characteristics (Ta=25 °C)**

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc		-	2	4	MHz
Reset clock frequency	frg		-	2	4	MHz
Vertical shift register capacitance	CP1AV, CP2AV CP1BV, CP2BV		-	15000	-	pF
Horizontal shift register capacitance	CP1AH, CP2AH CP1BH, CP2BH		-	500	-	pF
Summing gate capacitance	CSG		-	15	-	pF
Reset gate capacitance	CRG		-	10	-	pF
Transfer gate capacitance	CTG		-	500	-	pF
Transfer efficiency	CTE	*2	0.99995	0.99999	-	
DC output level	Vout	*3	5	8	11	V
Output impedance	Zo	*3	-	500	-	Ω
Power dissipation	P	*3, *4	-	60	-	mW

\*2: Measured at half of the full well capacity. CTE is defined per pixel.

\*3: VOD=15 V

\*4: Power dissipation of the on-chip amplifier-

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat		-	Fw × Sv	-	V
Full well capacity	Vertical	Fw		600	1200	-	ke <sup>-</sup>
	Horizontal			600	1200	-	
	Summing			600	1200	-	
CCD node sensitivity		Sv	*5	0.45	0.6	-	μV/e <sup>-</sup>
Dark current (MPP mode)		DS	*6	-	2	8	ke <sup>-</sup> /pixel/s
Readout noise		Nr	*7	-	60	120	e <sup>-</sup> rms
Dynamic range		DR	*8	5000	20000	-	
Photo response non-uniformity		PRNU	*9	-	±3	±10	%
Spectral response range		λ		-	400 to 1100	-	nm
Blemish	Point defects *10	White spots		-	-	0	-
		Black spots		-	-	0	
	Cluster defects		*11	-	-	0	
	Column defects		*12	-	-	0	

\*5: VOD=15 V.

\*6: Dark current doubles for every 5 to 7 °C.

\*7: -40 °C, operating frequency is 2 MHz.

\*8: Dynamic range = Full well capacity / Readout noise

\*9: Measured at the half of the full well capacity

$$PRNU (\%) = \text{Noise} / \text{Signal} \times 100$$

Noise: Fixed pattern noise (peak to peak)

\*10: White spots > 20 times of Max. dark signal (8 ke<sup>-</sup>/pixel/s).

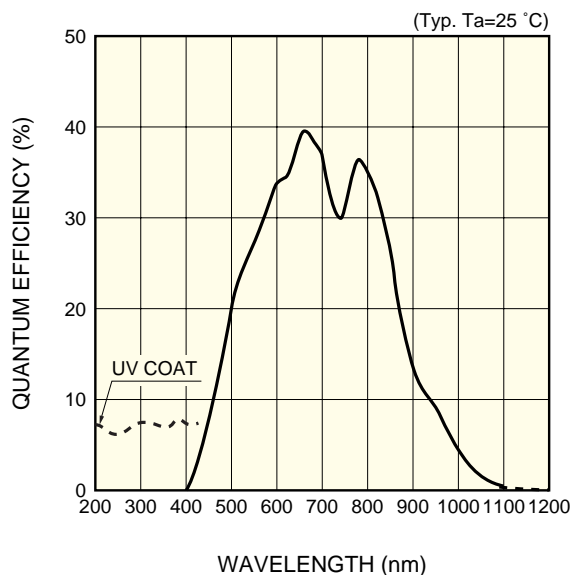
Black spots

Pixels whose sensitivity is lower than one-half of the average pixel output (Measured with uniform light producing one-half of the saturation charge)

\*11: 2 to 9 contiguous defective pixels.

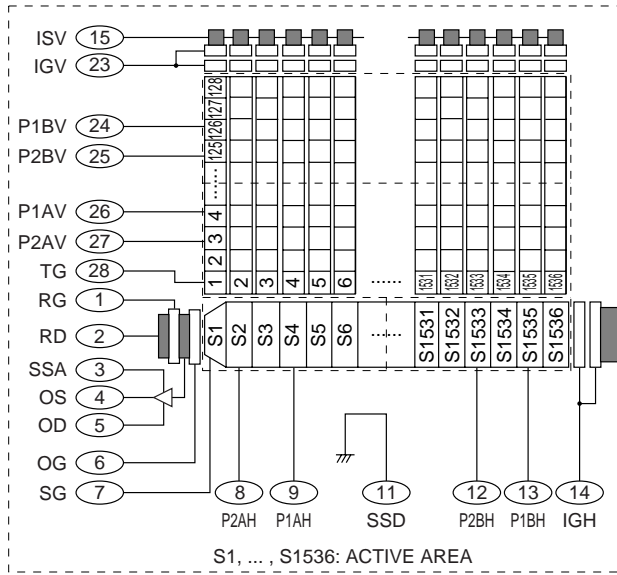
\*12: 10 or more contiguous defective pixels.

■ Spectral response (without window)



KMPD80244EB

■ Device structure



KMPDC0234EA

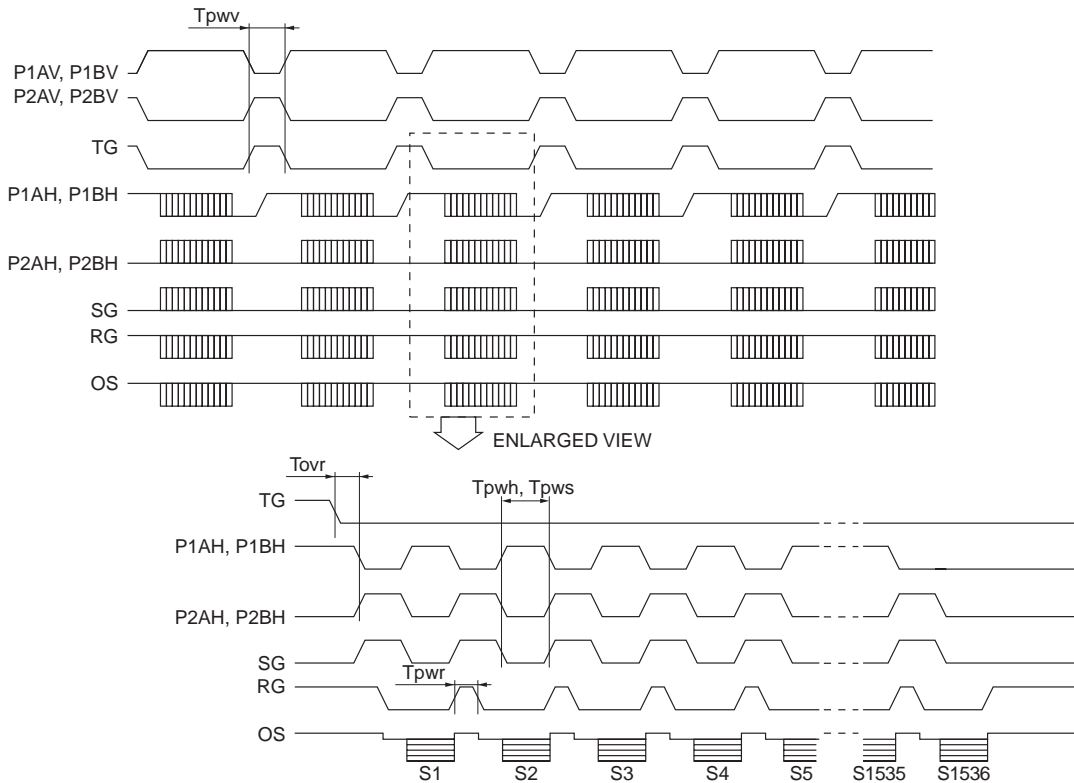
■ Pixel format

← Left Horizontal Direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
0	0	0	1536	0	0	0

Top ← Vertical direction → Bottom		
Isolation	Effective	Isolation
0	128	0

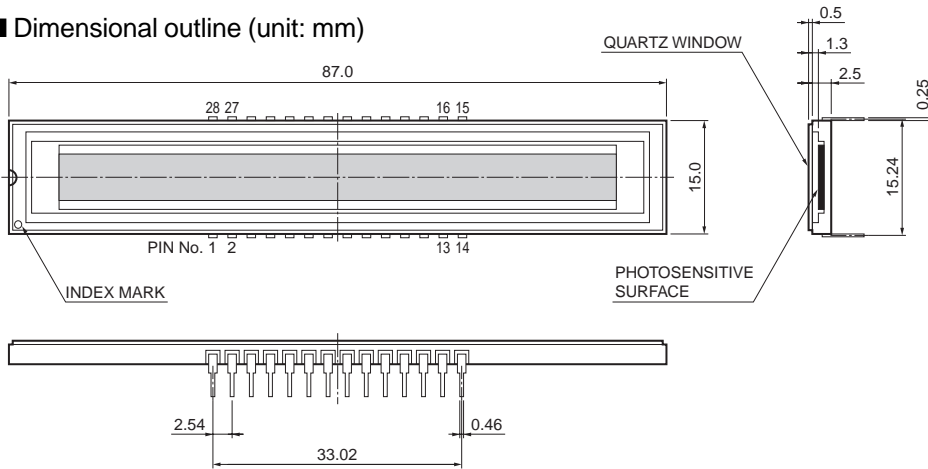
■ Timing chart (TDI operation)



KMPDC0142EB



■ Dimensional outline (unit: mm)



KMPDA0203EA

■ Pin connections

Pin No.	Symbol	Description	Remark
1	RG	Reset gate	
2	RD	Reset drain	
3	SSA	Analog ground	
4	OS	Output transistor source	
5	OD	Output transistor drain	
6	OG	Output gate	
7	SG	Summing gate	
8	P2AH	CCD horizontal register clock A-2	
9	P1AH	CCD horizontal register clock A-1	
10	NC		
11	SSD	Digital ground	
12	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
13	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
14	IGH	Test point (Horizontal input gate)	
15	ISV	Test point (Vertical input source)	Shorted to RD
16 to 22	NC		
23	IGV	Test point (Vertical input gate)	
24	P1BV	CCD vertical register clock B-1	Same timing as P1AV
25	P2BV	CCD vertical register clock B-2	Same timing as P2AV
26	P1AV	CCD vertical register clock A-1	
27	P2AV	CCD vertical register clock A-2	
28	TG	Transfer gate	

■ Precautions for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

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HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184, www.hamamatsu.com

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741

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