



## RB-TA2021

# CLASS-T DIGITAL AUDIO AMPLIFIER 6 CHANNEL TA2021 REFERENCE DESIGN

Technical Information - Board Rev. 1.7

Revision 1.0 – December 2002

### GENERAL DESCRIPTION

The RB TA2021 Version 1.7 is a 6 channel, 20W per channel audio amplifier designed to provide a simple and straightforward environment for the evaluation of the TA2021 amplifier. For additional documentation on the TA2021, see the TA2021 Data Sheet ([www.tripath.com](http://www.tripath.com)).

### APPLICATIONS

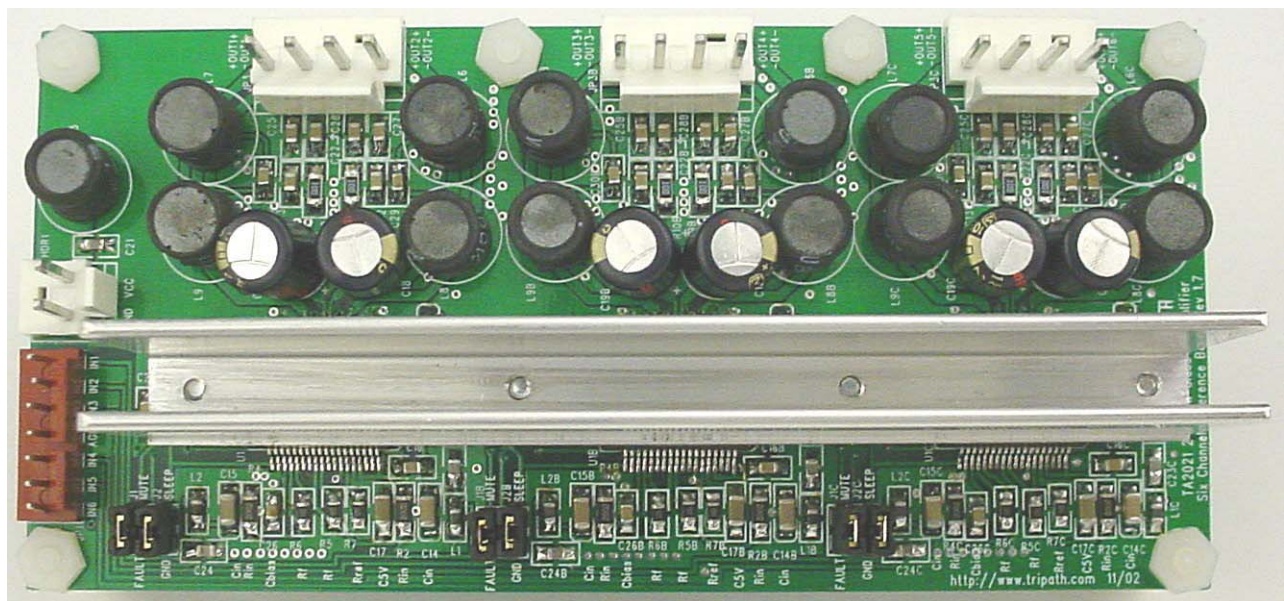
- DVD Receivers
- Mini/Micro Component Systems
- Computer / PC Multimedia
- Cable Set-Top Products
- Televisions

### BENEFITS

- Integrated solution with internal FETs
- Improved efficiency over Class-AB amps
- Simplifies thermal management
- Signal Quality equal to linear amplifiers

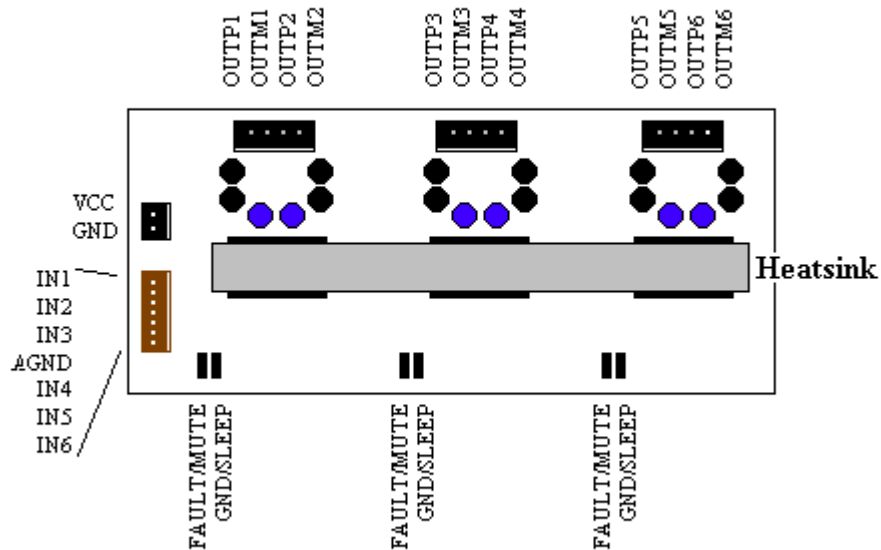
### FEATURES

- High Power: 6 X 20W @ 4Ω
- Single Supply Operation
- Low Noise Floor: 120uV A-weighted
- Low Distortion: 0.05% THD+N @ 10W 4Ω
- High Efficiency:
  - 81% for 4Ω loads
- Dynamic Range = 100dB
- Mute and Sleep inputs
- Over-Current Protection
- Over and Under Voltage Protection
- Over Temperature Protection



## OPERATING INSTRUCTIONS

### EVALUATION BOARD DIAGRAM



### POWER SUPPLIES

The TA2020 requires a +13.5V power supply to operate. Power to the board is provided via HDR1, a 2 pin 0.156" spaced header. The minimum operating voltage is 8.5V and the maximum operating voltage is 14.6V. Under and over-voltage protection circuits will cause the amplifier to mute if these conditions are not followed.

Header Label	Description
VCC	Positive of the 13.5V Power supply
GND	Negative (GND) of 13.5V Power Supply

**Warning: Do not exceed Maximum Operating Supply Voltage of 14.6V**

### OUTPUT

The output connections, JP3, JP3B and JP3C, are 4-Pin 0.156" spaced headers. The female terminal housing for this header is Molex 09-50-8041. The outputs of the TA2021 are differential (bridged). Therefore, each channel requires two wires to connect a speaker, neither of which is ground.

JP3 pin #	Connection
1	OUTP2 (ch1)
2	OUTM2 (ch1)
3	OUTM1 (ch2)
4	OUTP1 (ch2)

JP3B pin #	Connection
1	OUTP2 (ch3)
2	OUTM2 (ch3)
3	OUTM1 (ch4)
4	OUTP1 (ch4)

JP3C pin #	Connection
1	OUTP2 (ch5)
2	OUTM2 (ch5)
3	OUTM1 (ch6)
4	OUTP1 (ch6)

## INPUT

The input connection, JP1, is a 7-Pin 0.100" spaced header. The female terminal housing for this header is Molex 22-01-2077. The six inputs share a common ground referenced to AGND.

JP1 Connector Pin#	Connection
Pin1	IN1
Pin2	IN2
Pin3	IN3
Pin4	AGND
Pin5	IN4
Pin6	IN5
Pin7	IN6

## JUMPER SETTINGS (MUTE and SLEEP)

There are three 2-pin headers for the MUTE control of the TA2021s. If the jumpers are removed, the channels will be muted. If the jumpers are in place, the channels will be muted if the FAULT pin outputs a logic high. A logic high on the FAULT pin indicates an over-current, over-temperature, over-voltage or under-voltage condition.

There are three 2-pin headers for the SLEEP control of the TA2021s. If the jumpers are removed, the channels will be in sleep mode. If the jumpers are in place, the channels will operate properly.

*Note: All jumpers should be in place for normal amplifier operation.*

## GAIN SETTING

The gain of each channel of the TA2021 is set to 12V/V. It may be adjusted by the ratio of two external resistors, RI and RF, and is defined by the following formula:  $V_0/V_I = 12 \cdot (R_F/R_I)$ . VI is the input signal level and VO is the differential output signal level (see the top level schematic for more details).

## Performing Measurements on the TA2021

The TA2021 operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum in nature and typically varies between 100kHz and 1MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal, but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the TA2021 amplifier switching pattern will degrade the measurement by including out of band (audio) energy.

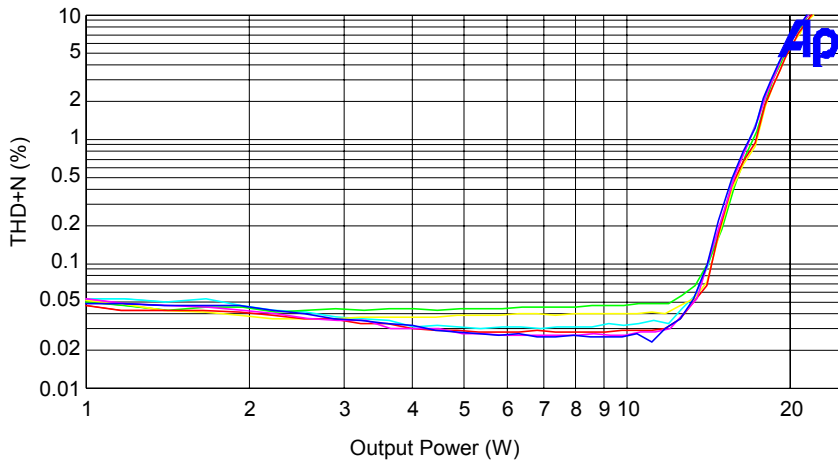
One feature of the TA2021 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TA2021 has a simple two-pole output filter with excellent performance in listening tests.

(See Application Note 4 for additional information on bench testing)

**Characteristic Curves**

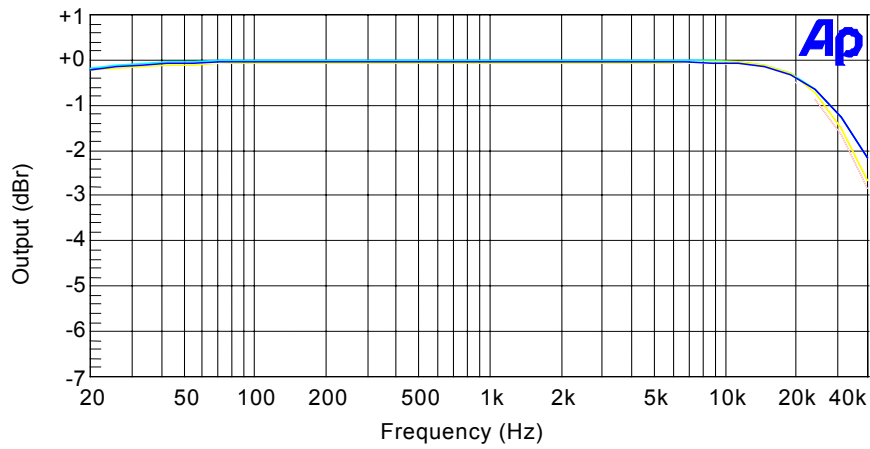
**THD+N vs Output Power**

(VCC=13.5V, 4ohm load)



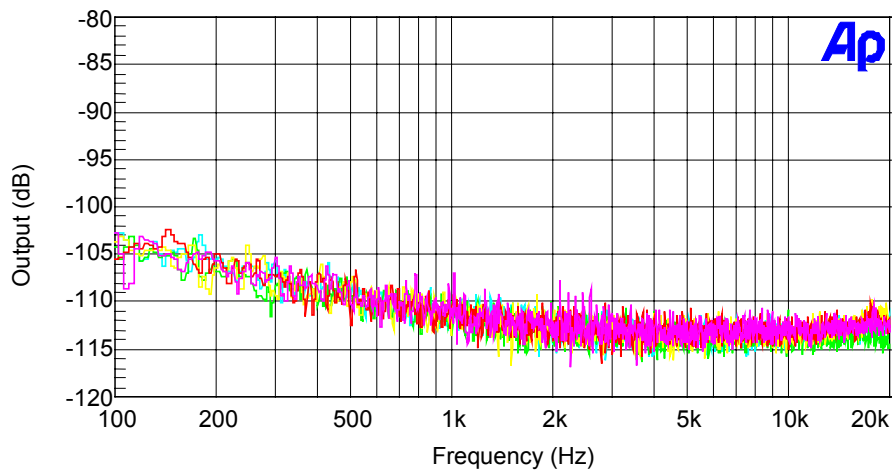
**Output Frequency Response**

(VCC = 13.5V, with a 1W reference output, 4ohm load)



**Noise Floor**

VCC=13.5V, 4 ohm load



## Layout Considerations

It is critical to have a good printed circuit board layout to prevent potentially damaging voltage stress as well as maximize audio performance. When designing a layout for two or more devices as opposed to a single TA2021, there are additional requirements to be considered. The following are layout recommendations to achieve the best performance and reliability for multiple device designs. The layout recommendations are listed in order of importance. The reference designators are for U1 of the schematic. The same rules apply for components around U1B and U1C.

1. All decoupling capacitors should be as close to each device as possible. This includes C6, C7, C18, C19, C26 and C17.
2. Utilize ground and power planes whenever possible.
3. Separation of analog and digital ground planes will optimize audio performance; they should be joined in one place only to avoid ground loops.
4. D5, D6, D7 and D8 should be located as close to the device as possible. These fast recovery diodes minimize output undershoot during high current events such as shorts to ground.
5. R5 and R6 should be located as close to the device as possible. These are the feedback resistors for the input-inverting amplifiers.
6. Ensure that the ground connection between the BIASCAP capacitor (C26) and the signal ground input is strong. If there is any noise voltage between these two points, the signal to noise ratio will be degraded.
7. R7 should be close to pin 6 (REF) and the ground side should be connected directly to pin 5 (AGND1).

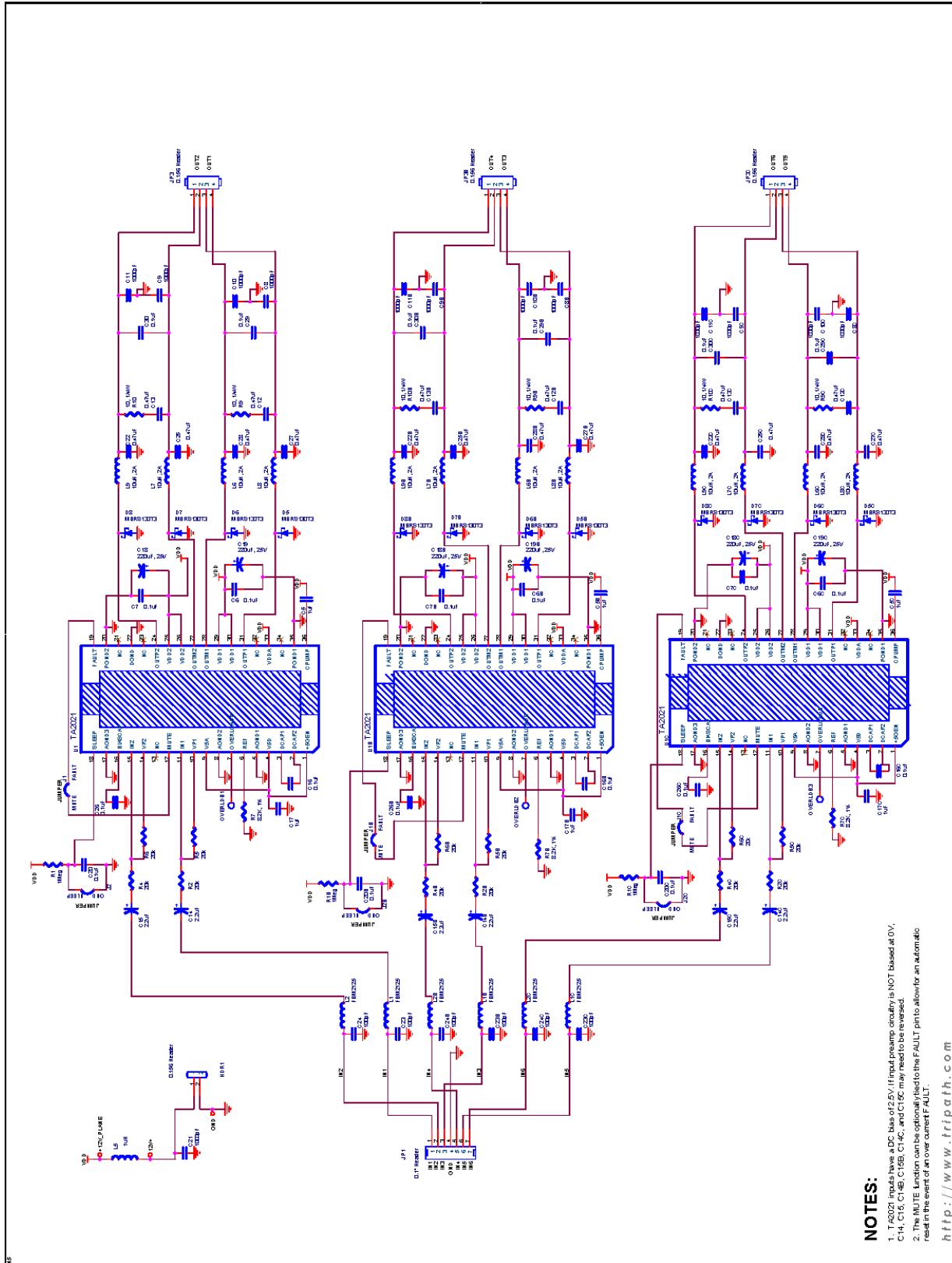
## Contact Information

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# Evaluation Board Schematic



**NOTES:**

1. TA2021 has a VCC bias of 0.5V. If input ground circuitry is NOT biased at 0V, C14, C15, C16, C18, C19, and C20 may need to be reversed.
2. The MUTE function can be optionally tied to the FAULT pin to allow for an automatic read in the event of an over current FAULT.

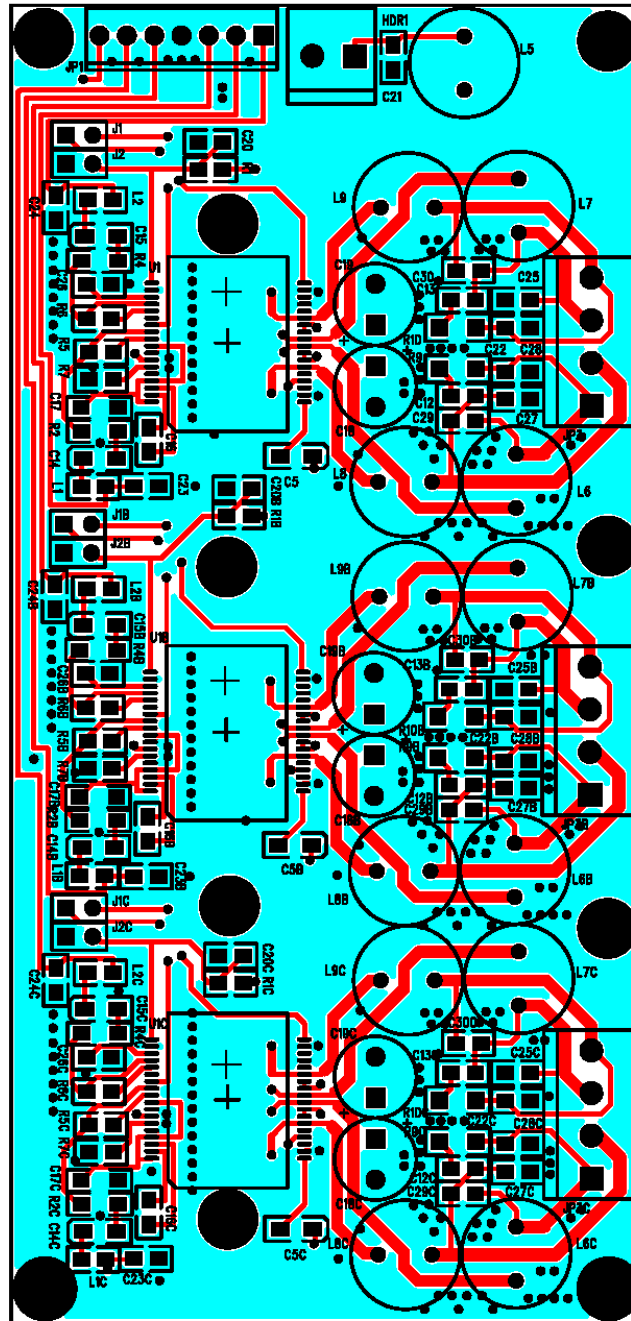
<http://www.tripath.com>

# Evaluation Board Bill of Materials

TA2021 6 channel, TA2021 Reference design  
 Bill of Materials  
 Revised: October 17, 2002  
 Revision: 1.0

Item	Qty	Reference	Part	Type	Footprint	Rating	Manufacturer	Manufacturer P/N	Digikey P/N	Digikey Price	Total Price
1	6	C3C,C3B,C5,C17C,C17B,C17	Capacitor	1uF CERAMIC X7R	805	16V	Yageo America	1206R105K7BB0D	311-1181-1-ND	\$ 0.09800	
2	21	C6C,C6B,C6,C7C,C7B,C7, C16C,C16B,C16,C20C,C20B, C20,C26C,C26B,C26C29C, C29B,C29C30C,C30B,C30	Capacitor	0.1uF CERAMIC X7R	805	50V	Yageo America	08052R104K9BB0D	311-1140-2-ND	\$ 0.01950	
3	13	C8C,C8B,C8,C9C,C9B,C9, C10C,C10B,C10,C11C,C11B, C11,C21	Capacitor	1000uF CERAMIC NPO	805		BC Components	0805N10J1500NT	BC1279CT-ND	\$ 0.03640	
4	18	C12C,C12B,C12,C13C,C13B, C13,C22C,C22B,C22,C25C, C25B,C25C27C,C27B,C27, C28C,C28B,C28	Capacitor	0.47uF CERAMIC X7R	805	16V	Panasonic ECG	ECJ-2YB1C474K	PCC1818CT-ND	\$ 0.10500	
5	6	C14C,C14B,C14,C15C,C15B, C15	Capacitor	2.2uF CERAMIC X5R		10V	Panasonic ECG	ECJ-3YB1A225K	PCC1868CT-ND	\$ 0.10050	
6	6	C18C,C18B,C18,C19C,C19B, C19	Capacitor	220uF Electrolytic		25V	Panasonic ECG	EEU-FC1E221	P10271-ND	\$ 0.12400	
7	6	C23C,C23B,C23,C24C,C24B, C24	Capacitor	100uF Ceramic NPO	805		BC Components	0805N10J1500NT	BC1268TR-ND	\$ 0.01125	
8	12	D5C,D5B,D5,D6C,D6B,D6, D7C,D7B,D7,D8C,D8B,D8	Diode Schottky	MBR5130T3	SMB	30V, 1A	International Rectifier	MBR5130TR	MBR5130CT-ND	\$ 0.13400	
9	1	HDR1	Connector	0.156" Header			Molex	26-60-4020	WM4620-ND	\$ 0.16998	
10	1	JP1	Connector	0.1" Header			Molex	22-23-2071	WM4205-ND	\$ 0.23850	
11	3	JP3C,JP3B,JP3	Connector	0.156" Header			Molex	26-60-4040	WM4622-ND	\$ 0.09868	
12	3	J1C,J1B,J12C,J2B,J2	Connector	0.1" Header 2-pin			3M	929834-02-36	(36-pin strips)	\$ 0.04550	
13	6	L1C,L1B,L1,L2C,L2B,L2	Ferrite Bead	FBM2125	805	4A, 100MHZ	Panasonic ECG	EXC-ML20A390U	P10191CT-ND	\$ 0.10050	
14	1	L5	Inductor	1uH							
15	12	L6C,L6B,L6,L7C,L7B,L7, L8C,L8B,L8,L9C,L8B,L9	Inductor	10uH, 2A			Toko America	822MY-100K (8RH92)	TK4467-ND	\$ 0.49000	
16	3	R1C,R1B,R1	Resistor	1Meg	805		Open		311-1.00MCCT-ND	\$ 0.02126	
17	6	R2C,R2B,R2,R4C,R4B,R4	Resistor	20k	1206		Open		311-20.0KFCCT-ND	\$ 0.02842	
18	6	R5C,R5B,R5,R6C,R6B,R6	Resistor	20k	805		Open		311-40.2KCCT-ND	\$ 0.02126	
19	3	R7C,R7B,R7	Resistor	8.2K, 1%	805		Open		311-8.20KCCT-ND	\$ 0.02126	
20	6	R9C,R9B,R9,R10C,R10B,R10	Resistor	10	1206	1/8W	Open		P10ETR-ND	\$ 0.00770	
21	3	U1C,U1B,U1	Resistor	TA2021	36P SSOP		Tripath Technology	TA2021			
22		4-40 Standoffs	Male/Female Nylon Threaded Standoff	0.25" x 0.75"			Keystone Electronics	4804	4804K-ND	\$ 0.13738	
23		4-40 Nuts	4-40 Nylon Nuts for Standoffs				Building Fasteners	NY HN 440	H616-ND	\$ 0.08400	
24		HeadSink								\$ 10.00000	

### Evaluation Board Layout (Top-Layer Composite)

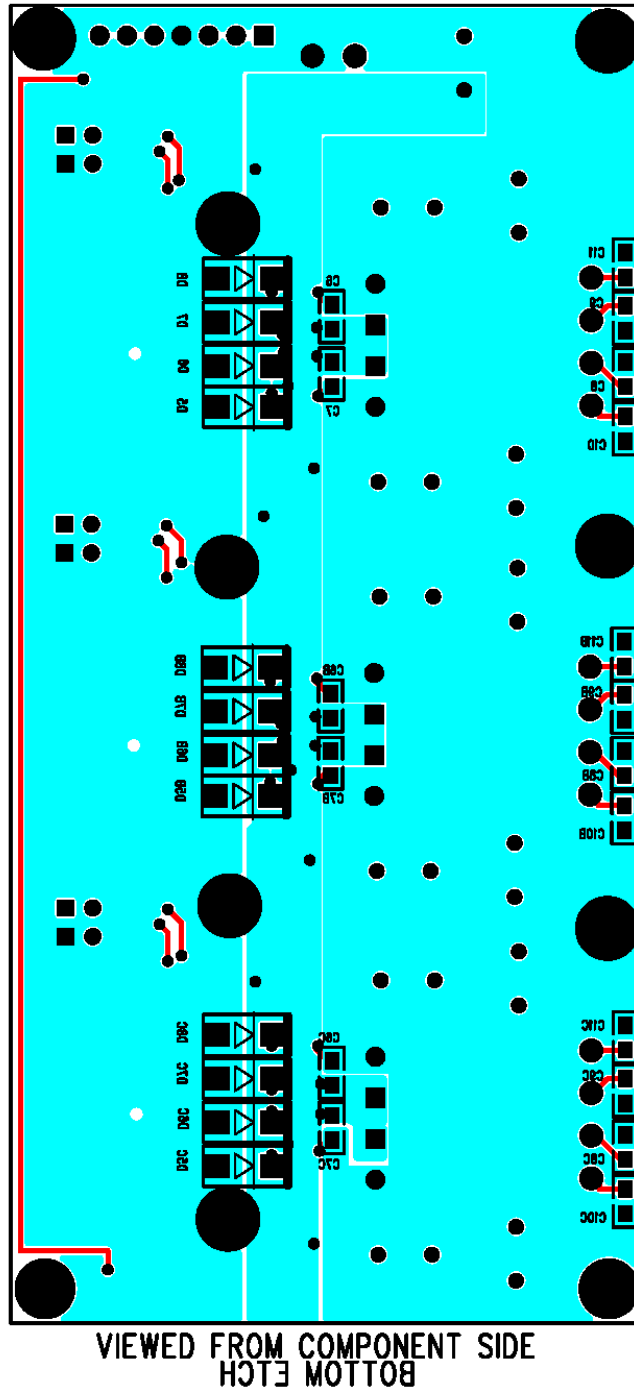


VIEWED FROM COMPONENT SIDE  
TOP ETCH

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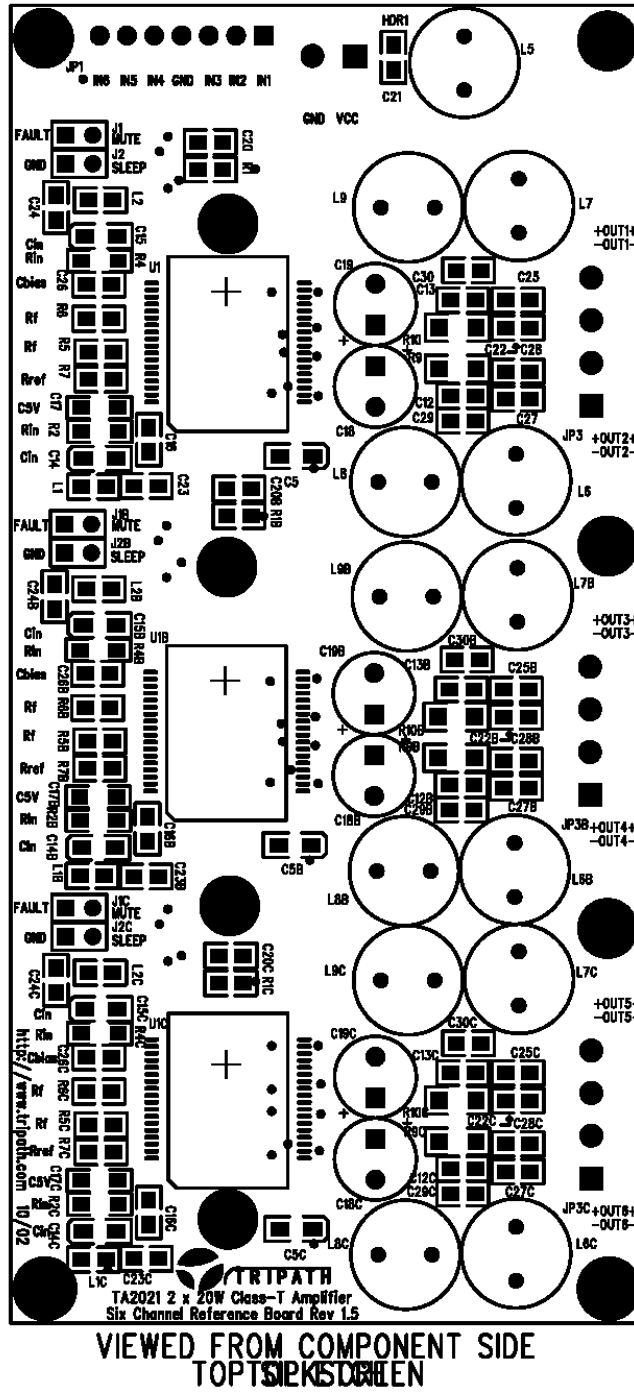


### Evaluation Board Layout (Bottom-Layer Composite)



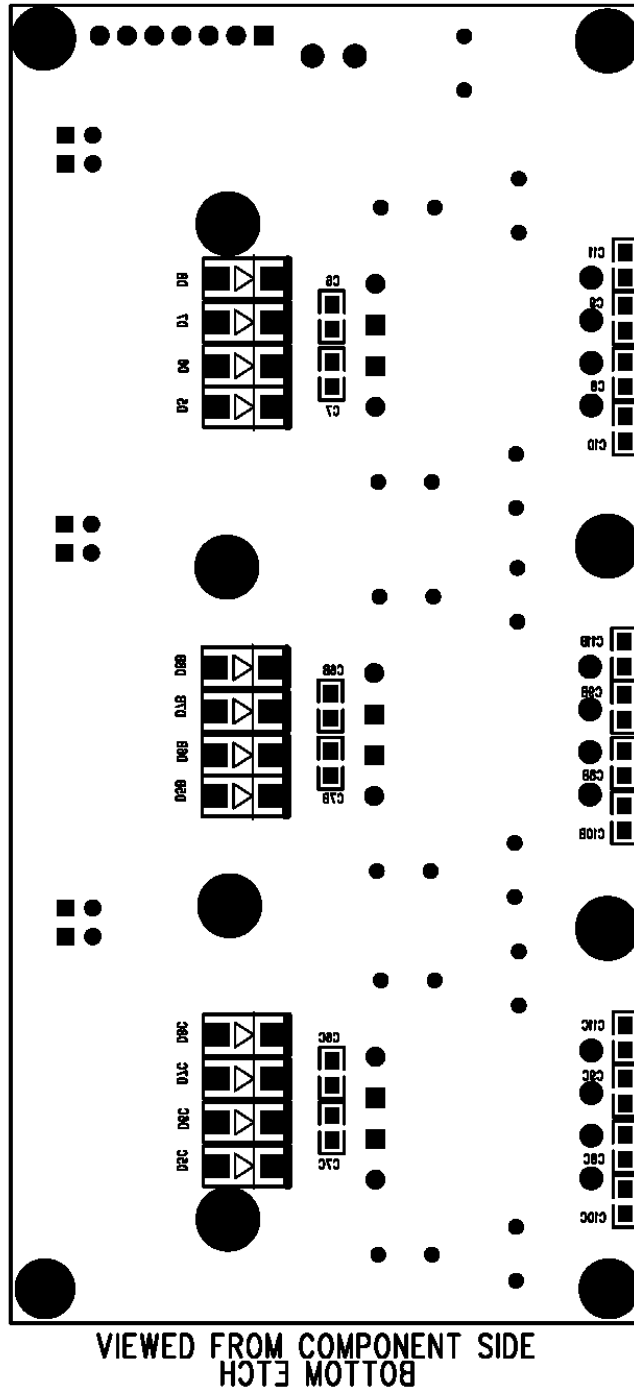
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Evaluation Board Layout (Top-Layer Silkscreen)



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**Evaluation Board Layout (Bottom-Layer Silkscreen)**



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