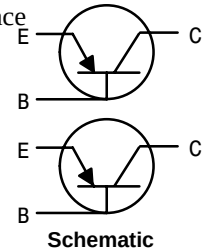
MMDJ3P03BJT

ON Semiconductor Preferred Device

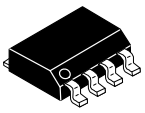
Plastic Power Transistors
SO–8 for Surface Mount Applications

DUAL BIPOLAR
POWER TRANSISTOR
PNP SILICON
30 VOLTS
3 AMPERES

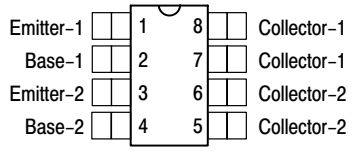
- Collector –Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain —
  h_{FE} = 125 (Min) @ I_C = 0.8 Adc
  = 90 (Min) @ I_C = 3.0 Adc
- Low Collector –Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.24 Vdc (Max) @ I_C = 1.2 Adc
  = 0.55 Vdc (Max) @ I_C = 3.0 Adc
- Miniature SO–8 Surface Mount Package – Saves Board Space



Schematic



CASE 751–07, Style 16
(SO–8)



Top View
Pinout

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	45	Vdc
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Emitter–Base Voltage	V_{EB}	±6.0	Vdc
Collector Current — Continuous — Peak	I_C	3.0 5.0	Adc
Base Current — Continuous	I_B	1.0	Adc
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Ambient on 1″ sq. (645 sq. mm) Collector pad on FR–4 board material with one die operating. Thermal Resistance – Junction to Ambient on 0.012″ sq. (7.6 sq. mm) Collector pad on FR–4 board material with one die operating.	$R_{\theta JA}$	 100 185	°C/W
Total Power Dissipation @ T_A = 25°C mounted on 1″ sq. (645 sq. mm) Collector pad on FR–4 board material with one die operating. Derate above 25°C	P_D	 1.25 10	 Watts mW/°C
Maximum Temperature for Soldering	T_L	260	°C

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	—	—	Vdc
Emitter–Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω)	I_{CER}	—	—	20	μAdc
(V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)		—	—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS(1)					
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc)	$V_{CE(sat)}$	—	0.15	0.21	Vdc
(I_C = 1.2 Adc, I_B = 20 mAdc)		—	—	0.24	
(I_C = 3.0 Adc, I_B = 0.3 Adc)		—	—	0.55	
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	—	—	1.25	Vdc
Base–Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	125	260	—	—
(I_C = 1.2 Adc, V_{CE} = 1.0 Vdc)		110	—	—	
(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)		90	—	—	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	—	100	150	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	—	135	—	pF
Current–Gain — Bandwidth Product(2) (I_C = 500 mA, V_{CE} = 10 V, F_{test} = 1.0 MHz)	f_T	—	110	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{FE}| \bullet f_{test}$

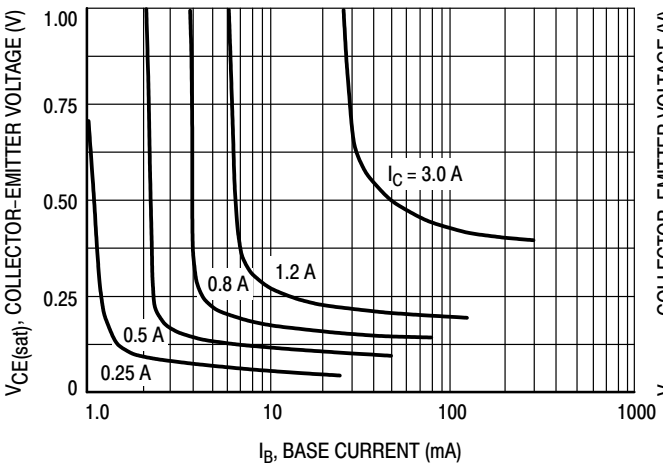


Figure 1. Collector Saturation Region

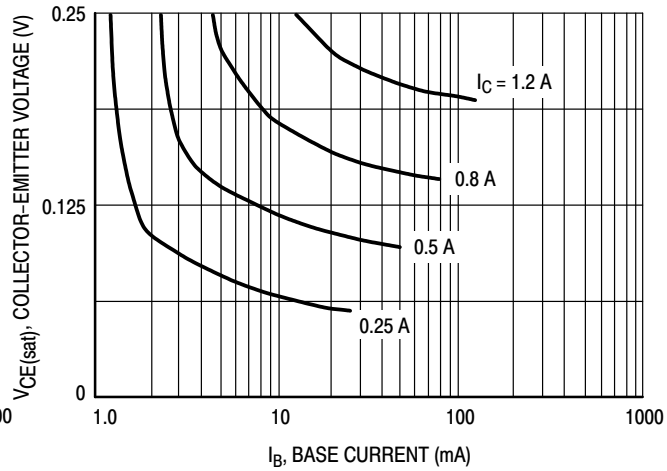


Figure 2. Collector Saturation Region

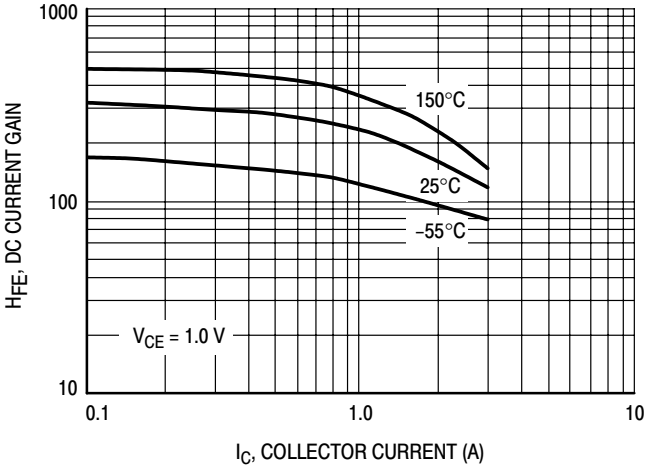


Figure 3. DC Current Gain

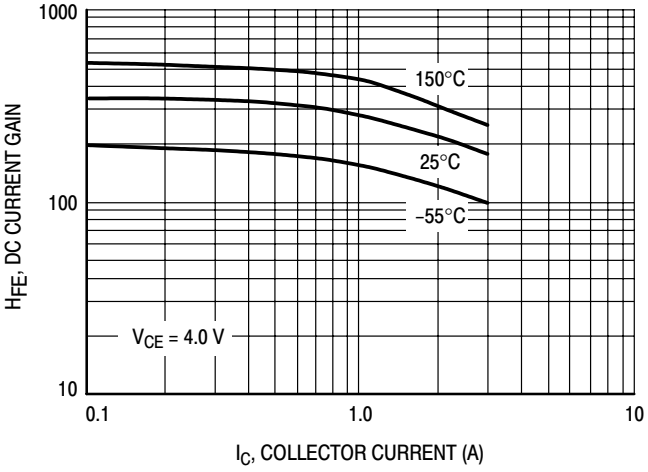


Figure 4. DC Current Gain

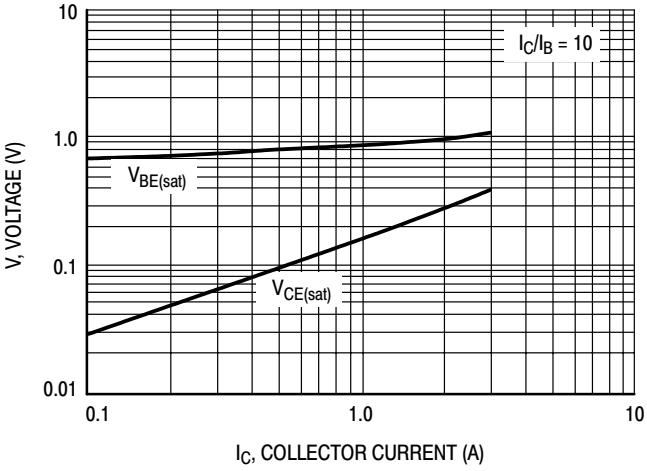


Figure 5. “On” Voltages

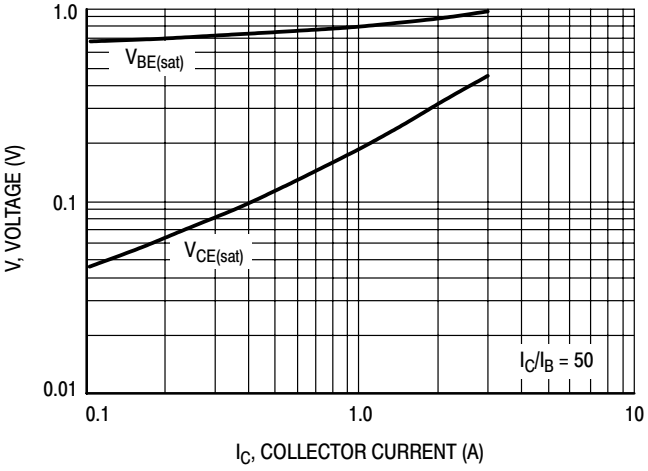


Figure 6. “On” Voltages

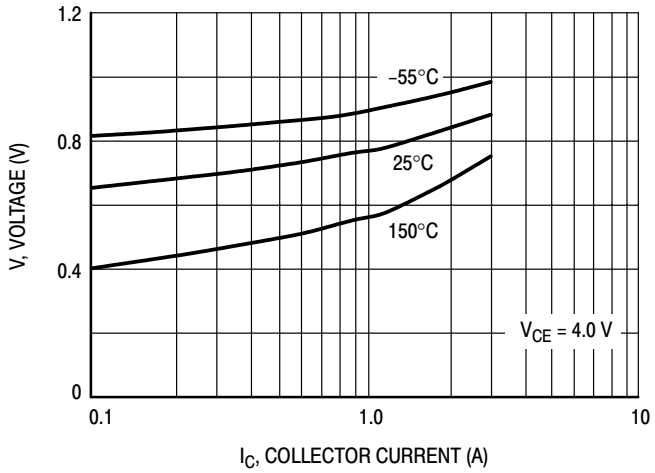


Figure 7. $V_{BE(on)}$ Voltage

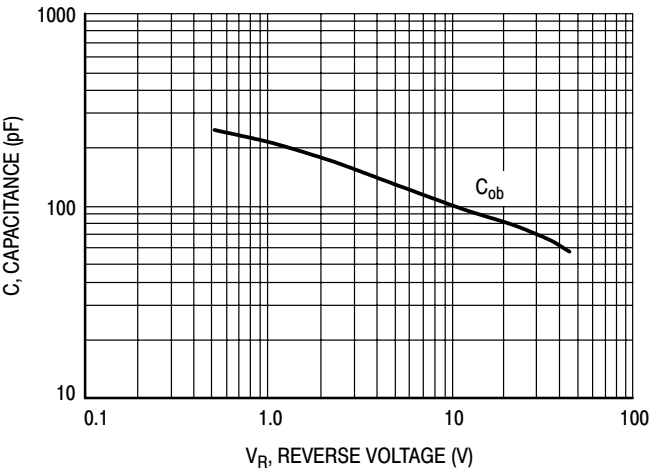


Figure 8. Output Capacitance

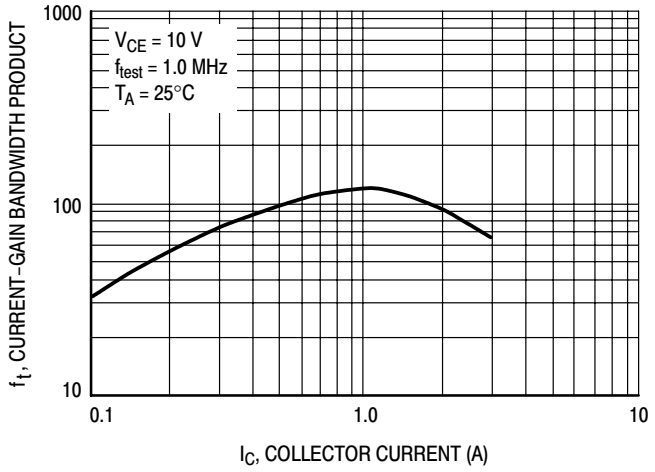


Figure 9. Current−Gain Bandwidth Product

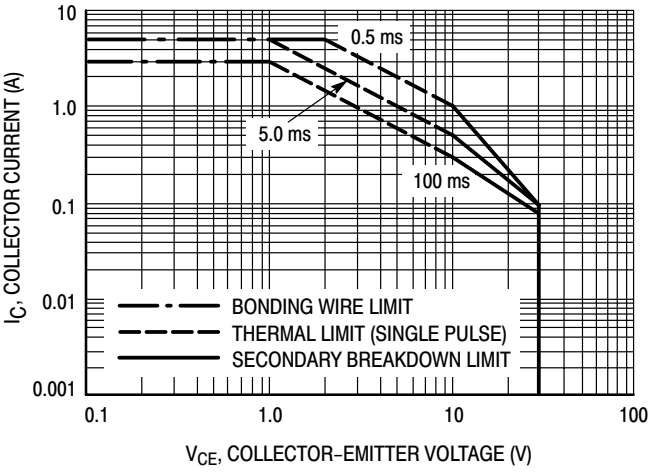


Figure 10. Active Region Safe Operating Area

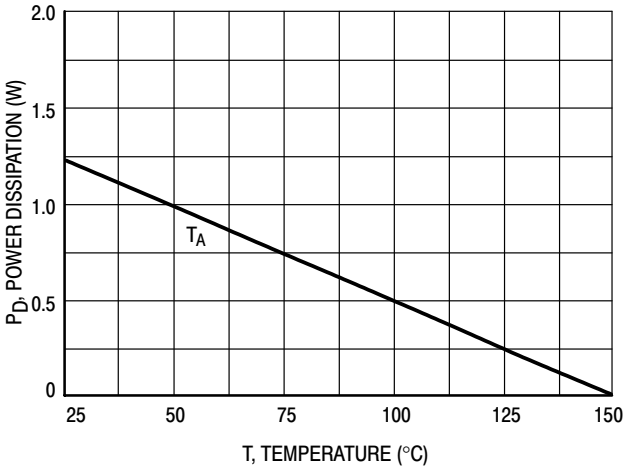


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

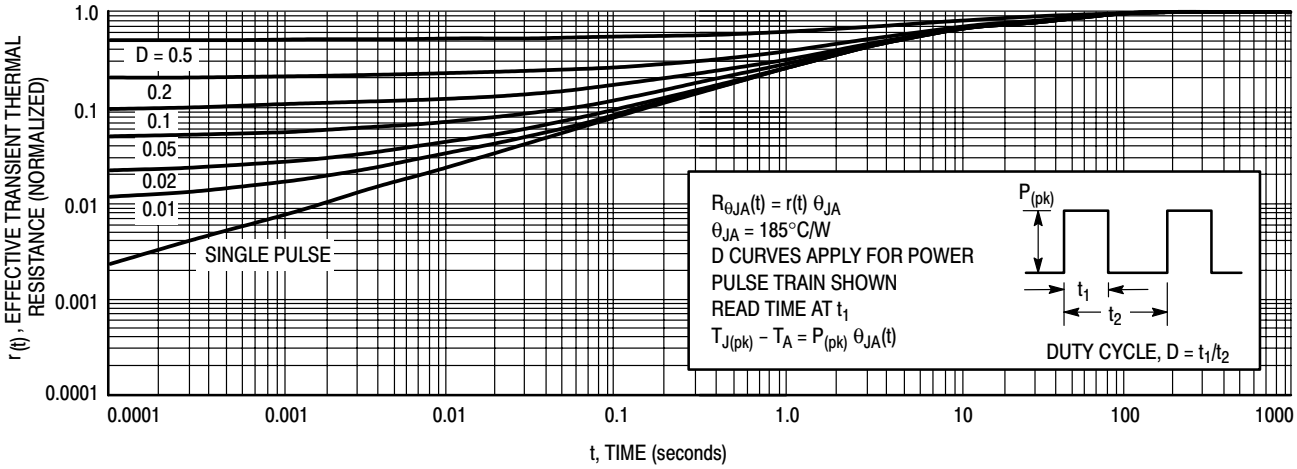
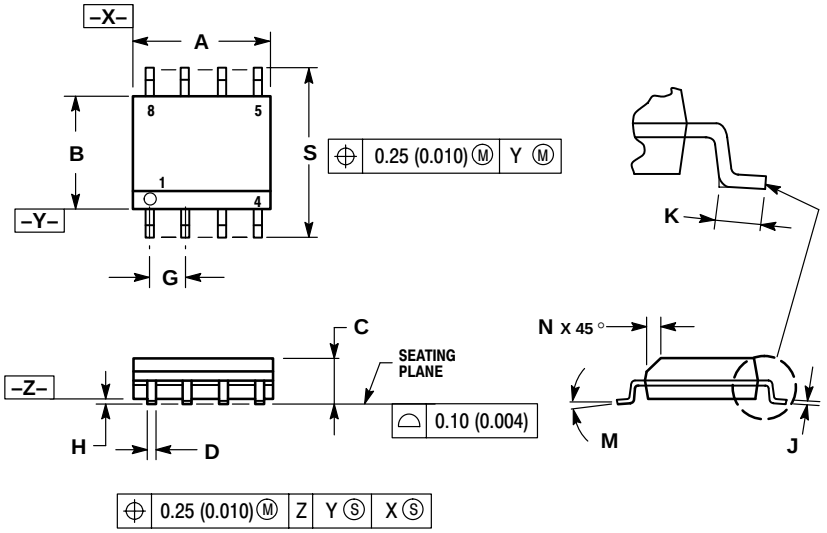


Figure 12. Thermal Response

PACKAGE DIMENSIONS

SOIC–8 NB
CASE 751–07
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

Notes

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