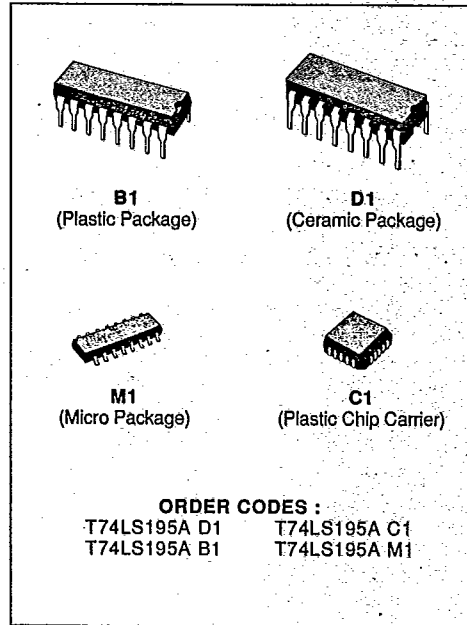


**UNIVERSAL 4-BIT SHIFT REGISTER**

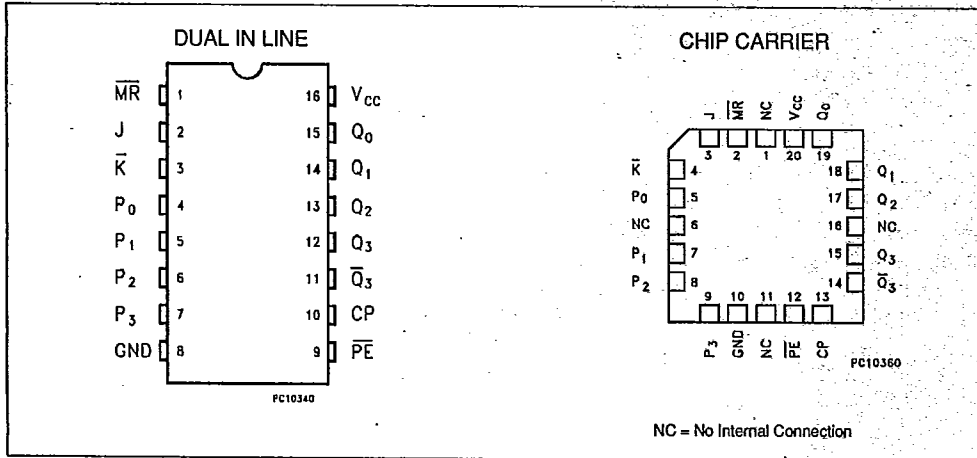
- TYPICAL SHIFT REGISTER FREQUENCY OF 40 MHz
- ASYNCHRONOUS MASTER RESET
- J, K INPUT TO FIRST STAGE
- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

**DESCRIPTION**

The T74LS194A is a High Speed Bidirectional Universal Shift Register. As a high speed multifunctional building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data register transfers.



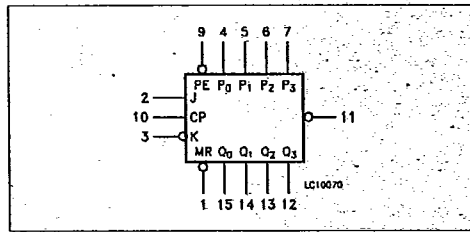
**PIN CONNECTION (top view)**



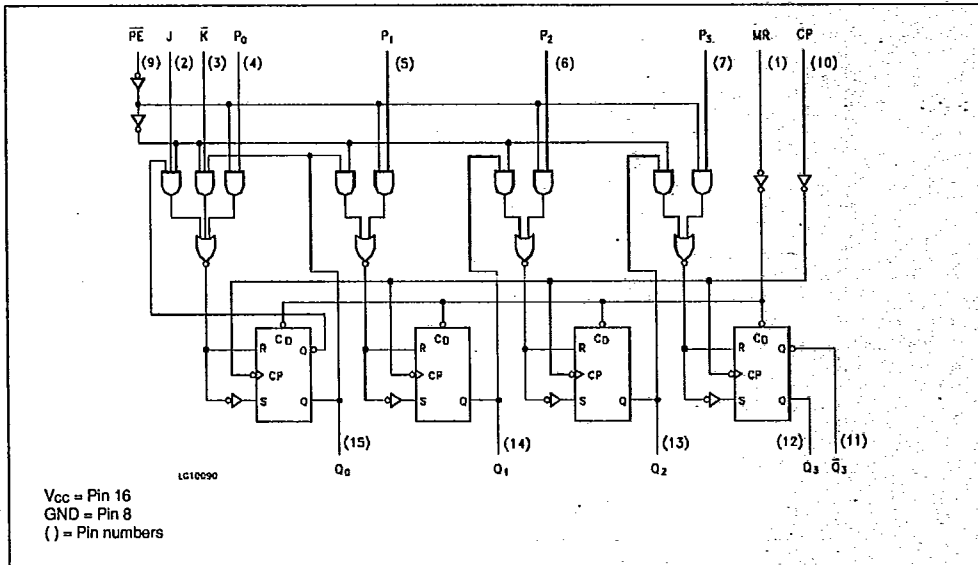
PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
$P_0$ - $P_3$	Parallel Data Inputs
J	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
CP	Clock (Active HIGH Going Edge) Input
MR	Master Reset (Active LOW) Input
$Q_0$ - $Q_3$	Parallel Outputs
$\overline{Q_3}$	Complementary Last Stage Output

LOGIC SYMBOL



LOGIC DIAGRAM



TRUTH TABLE

OPERATING	INPUTS					OUTPUTS				
	MR	$\overline{PE}$	J	$\overline{K}$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$	$\overline{Q_3}$
Asynchronous Reset	L	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	h	h	h	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub>
Shift, Reset First Stage	H	h	l	l	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub>
Shift, Toggle First Stage	H	h	h	l	X	q <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub>
Shift, Retain First Stage	H	h	l	h	X	q <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>2</sub>
Parallel Load	H	l	X	X	p <sub>n</sub>	p <sub>0</sub>	p <sub>1</sub>	p <sub>2</sub>	p <sub>3</sub>	p <sub>3</sub>

L = LOW Voltage Level  
H = HIGH Voltage Level  
X = Don't Care  
l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition  
h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition  
P<sub>n</sub> (q<sub>n</sub>) = Lower case letters indicate the state of the reference input (or output) one set-up time prior to the LOW to HIGH clock transition.

## FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS195A Shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The LS195A has not two primary modes of operation, shift right ( $Q_0 \rightarrow Q_1$ ) and parallel load which are controlled by the state of the Parallel Enable (PE) input. When the PE input is HIGH, serial data enters the first flip-flop  $Q_0$  via the J and K inputs and is shifted one bit in the direction  $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$  following each LOW to HIGH clock transition. The J  $\bar{K}$  inputs provide the flexibility of the J K type input for special applications, are the simple D type input

for general applications by tying the two pins together. When the PE input is LOW, the LS195A appears as four common clocked D flip-flop. The data on the parallel inputs  $P_0, P_1, P_2, P_3$  is transferred to the respective  $Q_0, Q_1, Q_2, Q_3$  outputs to the  $P_{n-1}$  inputs and holding the PE input LOW. All serial and parallel data transfers are synchronous, occurring after each LOW to HIGH clock transition. Since the LS195A utilizes edge-triggering, there is no restriction on the activity of the J, K,  $P_n$  and PE inputs for logic operation - except for the set-up and release time requirements.

A LOW on the asynchronous Master Reset ( $\bar{MR}$ ) input sets all Q outputs LOW, independent for any other input condition.

## ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	- 0.5 to 7	V
$V_i$	Input Voltage, Applied to Input	- 0.5 to 15	V
$V_o$	Output Voltage, Applied to Output	- 0.5 to 10	V
$I_i$	Input Current, Into Inputs	- 30 to 5	mA
$I_o$	Output Current, Into Outputs	30	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS195AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)	Unit
		Min.	Typ. (*)	Max.		
V <sub>IH</sub>	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Input	V
V <sub>IL</sub>	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Input	V
V <sub>CD</sub>	Input Clamp Diode Voltage		- 0.65	- 1.5	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	V
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.4		V <sub>CC</sub> = MIN, I <sub>OH</sub> = - 400 µA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	V
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	I <sub>OL</sub> = 12 mA	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
			0.35	0.5	I <sub>OL</sub> = 24 mA	
I <sub>IH</sub>	Input HIGH Current			20 0.1	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	µA mA
I <sub>IL</sub>	Input LOW Current			- 0.4	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	mA
I <sub>OS</sub>	Output Short Circuit Current (note 2)	- 20		- 100	V <sub>CC</sub> = MAX, V <sub>OUT</sub> = 0 V	mA
I <sub>CC</sub>	Power Supply Current		14	21	V <sub>CC</sub> = MAX	mA

Notes : 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

2. Not more than one output should be shorted at a time.

(\*) Typical values are at V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = 25 °C.

AC CHARACTERISTICS: T<sub>A</sub> = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f <sub>MAX</sub>	Shift Frequency	30	40		Figures 1	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Outputs		14 17	22 26	Figures 1	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Propagation Delay, MR to Outputs		19	30	Figures 3	

AC SET-UP REQUIREMENTS: T<sub>A</sub> = 25 °C

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t <sub>wCP</sub>	Clock Pulse Width	16	17		Figure 1	ns
t <sub>s</sub> (Data)	Set-Up Time Data to Clock	15	11		Figure 2	ns
t <sub>h</sub> (Data)	Hold Time Data to Clock	0				ns
t <sub>s</sub> (S)	Set-Up Time PE Control to Clock	25	18		Figure 4	ns
t <sub>h</sub> (S)	Hold Time PE Control to Clock	0				ns
t <sub>w</sub> (MR)	Master Reset Pulse Width	12	8		Figure 3	ns
t <sub>rec</sub> (MR)	Recovery Time Mater Reset to Clock	25	6			ns
t <sub>release</sub>	PE			10		ns

DEFINITION OF TERMS: 42E D 7929237 0033492 T SGTH

**SET-UP TIME ( $t_s$ ):** is defined as the minimum time required for the correct logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

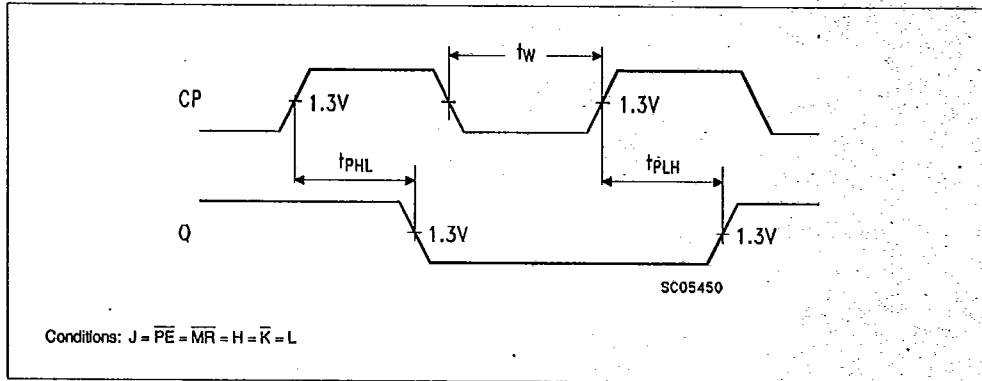
**HOLD TIME ( $t_h$ ):** is defined as the minimum time following the clock transition from LOW to HIGH at which the logic level must be maintained at the input

in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

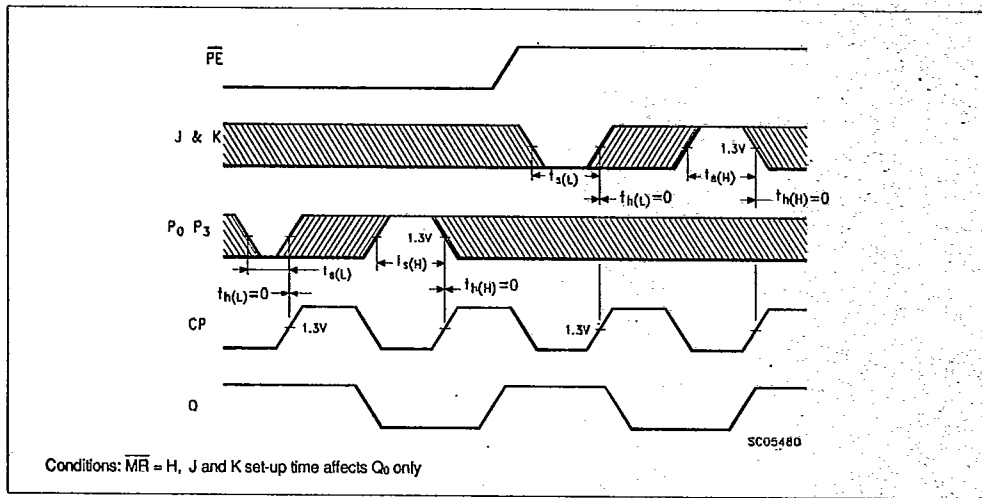
**RECOVERY TIME ( $t_{rec}$ ):** is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

**AC WAVEFORMS**

**Figure 1: Clock to Output Delays and Clock Pulse Width**



**Figure 2: Set-up ( $t_s$ ) and Hold ( $t_h$ ) Time for Serial Data (J & K) and Parallel Data ( $P_0, P_1, P_2, P_3$ )**



The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3: Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

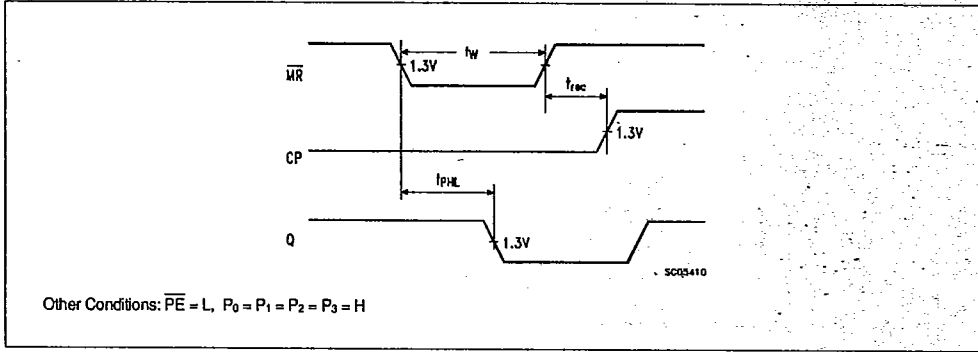
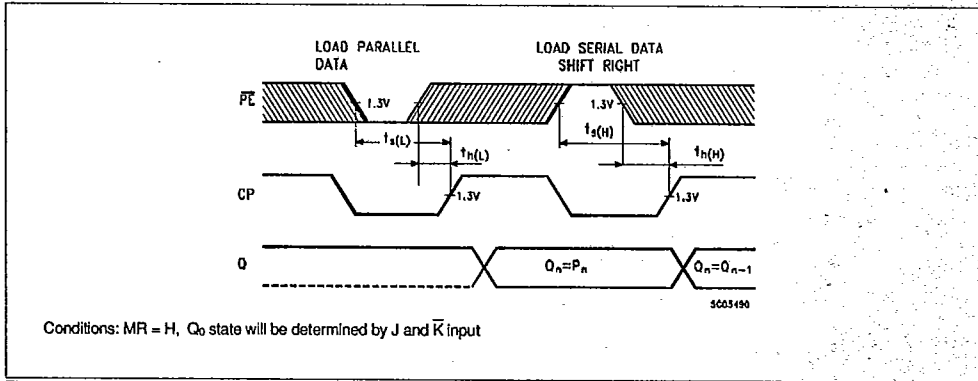


Figure 4: Set-up ( $t_s$ ) and Hold ( $t_h$ ) Time for  $\overline{PE}$  Input



The shaded areas indicate when the input is permitted to change for predictable output performance.