Advanced LCD Controller AL310 Data Sheets

Amendments

99.10.04 Preliminary version

02.12.17 Preliminary version A0.1:
(1) Updated from Preliminary version A0.1

03.05.23 Version B1.0:
(1) Updated from Preliminary version A0.2
(2) Add Register Description

THE INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WIHOUT NOTICE.

Contents:

1. General Description

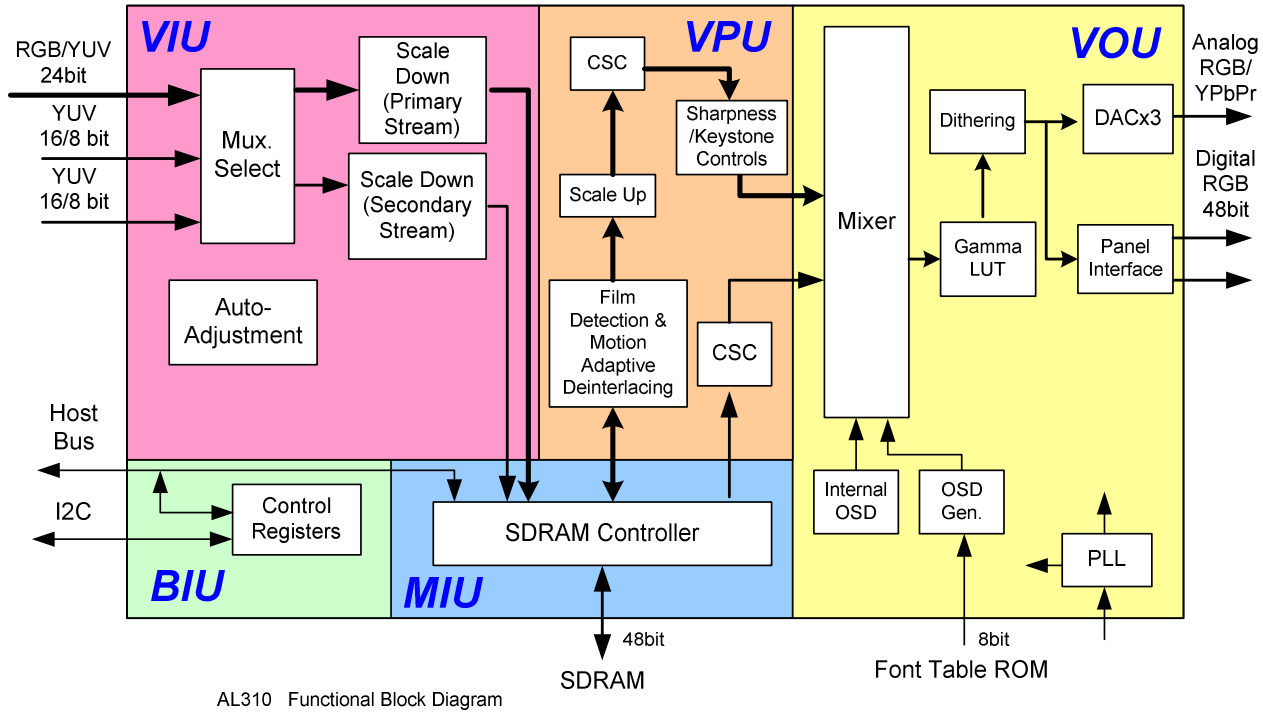
AL310 is a highly integration LCD Controller which supports Triple-Port input with multiple graphics/video formats capable and mixing captured frames output with scaling, overlaying and alpha blending effects…etc. It can be used for most video conversion and processing applications.

AL310 is equipped with a high-quality scaling engine that automatically maintains full screen output display, regardless of the resolution of the incoming signals. Applying AverLogic's proprietary scaling algorithm, the primary input graphics/video can be scaled up and scaled down independently in horizontal & vertical directions. It also provides film detection, advanced de-interlacing, filtering, and scaling which's able to convert and process the interlaced video to be displayed on progressive panels.

The On Screen Display (OSD) window provides overlay of a control menu, text, or caption on the output display. It's built-in OSD generator with 2K Bytes programmable RAM fonts and supports optional external OSD ROM.

AL310 is built-in 3-channel DAC for non-interlaced analog output and 48bit digital output. It's housed with 308-pin PBGA.

2. Function Block Diagram



AL310 Functional Block Diagram

3. Features

3.1 General Features

- Support Triple Digital RGB/YUV inputs and Non-interlaced RGB/YPbPr Analog and Digital outputs
- Triple Input ports for PIP overlaying (Video over Graphics or Video over Video)
- Film Detection with Inverse 3:2/2:2 Pull Down
- Advanced Motion Adaptive Deinterlacing
- AverLogic's Proprietary Scaling Algorithm for Scaling Up and Down
- Direct Video Memory Access for Graphic Data Processing
- Built-in 2K Bytes OSD RAM and support External OSD Font ROM
- Available in 308-pin PBGA
- 2.5V Core and 3.3V I/O power supplies with 5V input tolerant

3.2 Feature Description:

- Input Interface
  - Input resolution up to 1280x1024 @60Hz
  - Simultaneous Primary and Secondary input for PIP overlaying
  - Input resolution support: VGA up to SXGA(RGB), SDTV, EDTV and HDTV
  - Video interface ITU-R 656-8bit & 601-16bit, YUV422 supported

- Output Interface
  - Output resolution up to 1280x1024 @60Hz
  - Analog non-interlaced RGB/YPbPr and Digital RGB 48bit outputs supported

- SDRAM Interface
  - Support maximum 48bit bus width SDRAM interface, two or three of SDRAM configuration up to 125 MHz supported

- Deinterlacing and Scan Rate Conversion
  - DeInterlacing for Interlaced Video Input
  - Advanced Motion Adaptive Deinterlacing
  - Film Mode Detection with Inverse 3:2 & 2:2 pull down
  - Frame Rate Conversion(FRC) from 50Hz up to 120Hz

- Scaling Engine and Video Processing
  - Independent Scale Up and Down in both Horizontal and Vertical direction
  - Keystone Correction for Front-Projection Systems
  - Sharpness Control
  - Built-in LUT for Gamma Correction and Color Adjustment
  - Dithering Logic for Color Depth Enhancement

- Overlaying and Alpha Blending for PIP function
  - Two input source overlaying for PIP display with Alpha Blending/Transparency effect

- I2C or Parallel Port Registers Access
  - Registers can be accessed by serial I2C port or 8 bit parallel port for high speed registers data update

- On Screen Display (OSD)
  - 2k Bytes Internal OSD RAM for fine bitmaps and text font
  - Dual internal OSD windows support with Alpha Blending/Transparency effect
  - Support up to 64k Bytes External ROM for font and bitmap data
  - In ROM mode, 1.5k Bytes OSD RAM for Context RAM, 0.5k Bytes for Pre-fetch RAM
  - Pre-fetch RAM supports different speed types of Font ROMs (EE-PROM, PROM or Mask-ROM)

- Other Features
  - Primary input stream VBI pass through support
  - Automatic screen positioning and phase adjustment support for LCD output display
  - Frame capture Mirroring support in Horizontal or Vertical direction
  - NTSC/PAL Video Input Auto-Detection support
  - Power Saving support
  - Slave mode support

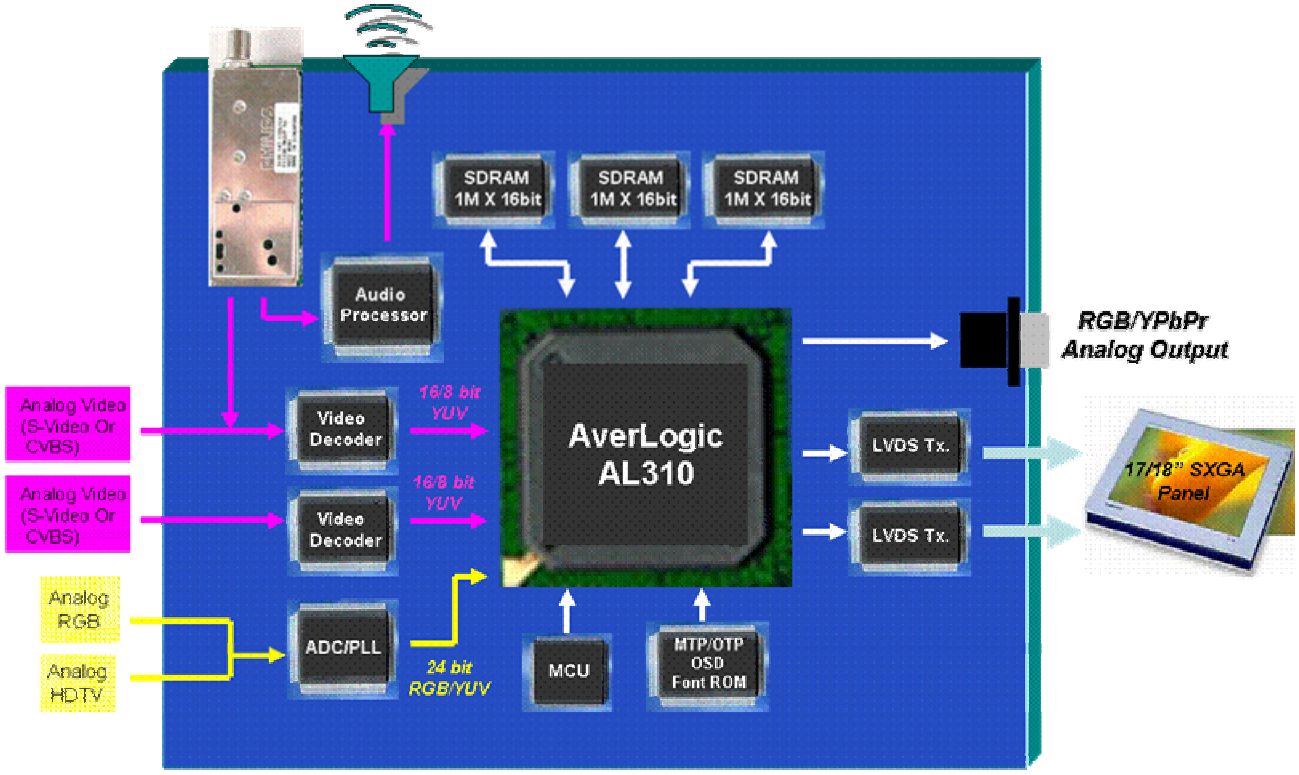
- Operating Power
  - 2.5V core and 3.3V I/O power supplies with 5V input tolerant

- Package
  - 308-pin PBGA

4 Applications

- PIP LCD TV & LCD Monitor with Video Input
- PIP PDP/Front Projection/Rear Projection/Progressive Scan TVs
- PIP HDTV/DTV Video Enhancer & Advanced TV Tuner Box
- Other PIP Flat Panel Displays

5 Application Example (Advanced LCD TV with PIP Function)



6 Pin-Out Diagram

PBGA-308 Package:

Coordinate	1	2	3	4	5	6	7	8	9	10
A	MXOUT	HOST_WRB	RA14	RA13	RA12	RA10	RA8	RA7	RA6	RA4
B	MXIN	HOST_DB7	RA15	VOUT46	VOUT45	RA11	RA9	VOUT40	RA5	RA3
C	VIN0	VIN33	RSTB	IREQ	VOUT44	VOUT43	VOUT37	VOUT35	VOUT34	VOUT36
D	VIN37	VIN35	P2VSS25	VOUT47	VOUT41	VOUT42	VOUT39	I2C_EN	VOUT38	VOUT32
E	VIN38	VIN36	VIN34	P1AVSS25					VDD25	VDD25
F	VIN3	VIN2	VIN1	P2VDD25						
G	VIN41	VIN40	VIN39	P2AVDD25						
H	VIN42	VIN5	VIN4	P2AVSS25				VDD33	VDD33	VSS33
J	VIN8	VIN43	VIN7	VIN6	VIN32			VDD33	VSS25	VSS25
K	VIN10	VIN45	VIN9	VIN44	P1AVDD25			VDD33	VSS25	VSS25
L	VIN46	VIN11	VIN12	VIN47	P1VDD25			VDD33	VSS25	VSS25
M	VIN13	VIN48	VIN14	VIN15	PSVDD25			VDD33	VSS25	VSS25
N	VIN49	PCCLK	PCHS	PCHREF				VDD33	VDD33	VSS33
P	VIN50	PCVS	VIN51	VIN16						
R	VIN52	VIN17	VIN19	VIN53						
T	VIN18	VIN20	VIN22	VIN54					VDD25	VDD25
U	VIN21	VIN55	GPO1	GPO0	HOST_DB3	V2HREF	HOST_DENB	MDATA4	MDATA0	DQML
V	VIN23	VIN25	VIN26	VIN28	VIN30	HOST_DB4	HOST_DB6	V2CLK	HOST_MEMB	MDATA2
W	VIN24	HOST_DB0	VIN27	VIN29	VIN31	HOST_DB5	V1VS	V2HS	MDATA1	MDATA3
Y	GPO2	HOST_DB1	HOST_DB2	V1CLK	V1HREF	V1HS	HOST_RDB	V2VS	HOST_RDYB	DQMH
Coordinate	1	2	3	4	5	6	7	8	9	10

11	12	13	14	15	16	17	18	19	20	Coordinate
RA2	RA1	RDATA7	RDATA5	RDATA3	RDATA1	SCLK	VOUT28	VOUT27	VOUT24	A
RA0	RDATA6	RDATA4	RDATA2	RDATA0	PHS	PVS	VOUT26	VOUT22	VOUT21	B
VOUT33	VOUT31	VOUT29	OXIN1	DSCLK	VOUT25	VOUT23	VOUT3	VOUT6	VOUT0	C
OXIN2	PDSDEN	VOUT30	VOUT1	VOUT2	VOUT7	VOUT4	VOUT5	VOUT15	VOUT14	D
VDD25	VDD25					VOUT13	VOUT19	VOUT10	VOUT16	E
						VOUT11	VOUT17	VOUT18	VOUT8	F
						AVSS25	VOUT20	VOUT9	VREFOUT	G
VSS33	VSS33	AVDD33				DVSS25	VOUT12	COMP	VREFIN	H
AVSS33R	AVDD33R	AVDD33B			AVSS33B	RSET	IOG	IOB	IOR	J
VSS25	VSS25	VSS33			AVSS33	MDATA36	MDATA35	MDATA34	MDATA33	K
VSS25	VSS25	VSS33			AVDD33G	MADDR7	MADDR8	MADDR11	MDATA32	L
VSS25	VSS25	VSS33			AVSS33G	AVDD25	MADDR4	MADDR9	MADDR10	M
VSS33	VSS33	VSS33				DVDD25	MADDR1	MADDR5	MADDR6	N
						VDD25	MADDR0	MADDR2	MADDR3	P
						VDD25	MDATA30	MDATA31	PMXIN	R
VDD25	VDD25					MDATA28	MDATA29	MDATA27	MDATA26	T
MDATA10	MDATA42	MDATA44	WEB	MDATA14	MDATA15	MDATA21	MDATA41	MDATA39	MDATA25	U
MDATA6	MDATA9	MDATA45	MDATA40	MDATA12	MDATA38	MDATA37	MDATA43	MDATA20	MDATA24	V
CSB	MDATA46	MDATA47	MDATA11	RASB	BA1	MDATA19	MDATA18	MDATA17	MDATA23	W
MDATA5	CLKE	MDATA7	MDATA8	CLK	CASB	BA0	MDATA13	MDATA16	MDATA22	Y
11	12	13	14	15	16	17	18	19	20	Coordinate

: Input Interface
: OSD ROM Interface
: DAC Output Interface
: Panel Interface
: SDRAM Interface
: HOST Interface
: PLL Interface
: Digital Power 2.5V
: Digital Ground 2.5V
: Digital Power 3.3V
: Digital Ground 3.3V

7 Pin Definition and Description

7.1 Input Format Table of AL310:

VIN No.	55~48	47~40	39~32	31~24	23~16	15~8	7~0
PC(V0)					R/Cr	G/Y Y	B/Cb CbCr YCbCr
V1		Cr	Y Y	Cb CbCr YCbCr			
V2	Y YCbCr	CbCr					

7.2 The pin-out definitions are described as follows:

Pin Name	Pin Number	I/O type	Description
Input Interface			
VIN[55:48]	U2,T4,R4,R1,P3,P1, N1,M2	I	***For V2:*** YUV 4:2:2(16bit) : Y[7:0] Input Data YUV 4:2:2 (8 bit) : YCbCr[7:0] Input Data
VIN[47:40]	L4,L1,K2,K4,J2,H1, G1,G2	I	***For V1:*** YUV 4:4:4 : Cr[7:0] Input Data ***For V2:*** YUV 4:2:2(16bit) : CbCr[7:0] Input Data
VIN[39:32]	G3,E1,D1,E2,D2,E3, C2,J5	I	***For V1:*** YUV 4:4:4 : Y[7:0] Input Data YUV 4:2:2(16bit) : Y[7:0] Input Data
VIN[31:24]	W5,V5,W4,V4,W3, V3,V2,W1	I	***For V1:*** YUV 4:4:4 : Cb[7:0] Input Data YUV 4:2:2(16bit) : CbCr[7:0] Input Data YUV 4:2:2 (8 bit) : YCbCr[7:0] Input Data
VIN[23:16]	V1,T3,U1,T2,R3,T1, R2,P4	I	***For PC*** RGB : RED[7:0] Input Data

Pin Name	Pin Number	I/O type	Description
			For V0: YUV 4:4:4 : Cr[7:0] Input Data
VIN[15:8]	M4,M3,M1,L3,L2,K1 ,K3,J1	I	***For PC*** RGB : GREEN[7:0] Input Data ***For V0:*** YUV 4:4:4 : Y[7:0] Input Data YUV 4:2:2(16bit) : Y[7:0] Input Data
VIN[7:0]	J3,J4,H2,H3,F1,F2, F3,C1	I	***For PC*** RGB : BLUE[7:0] Input Data ***For V0:*** YUV 4:4:4 : Cb[7:0] Input Data YUV 4:2:2(16bit) : CbCr[7:0] Input Data YUV 4:2:2 (8 bit) : YCbCr[7:0] Input Data
PCCLK	N2	I	Reference Clock of PC or Video Port 0
PCHREFF	N4	I	HDE Input of PC or Video Port 0
PCHS	N3	I	HSYNC Input of PC or Video Port 0
PCVS	P2	I	VSYNC Input of PC or Video Port 0
V1CLK	Y4	I	Reference Clock of Video Port 1
V1HREFF	Y5	I	HDE Input of Video Port 1
V1HS	Y6	I	HSYNC Input of Video Port 1
V1VS	W7	I	VSYNC Input of Video Port 1
V2CLK	V8	I	Reference Clock of Video Port 2
V2HREFF	U6	I	HDE Input of Video Port 2
V2HS	W8	I	HSYNC Input of Video Port 2
V2VS	Y8	I	VSYNC Input of Video Port 2
OSD ROM Interface			
RDATA[7:0]	A13,B12,A14,B13, A15,B14,A16,B15,	I	ROM Data Bus Bit 7-0
RA[15:0]	B3,A3,A4,A5,B6,A6, B7,A7,A8,A9,B9,A10 ,B10,A11,A12,B11	O	ROM Address Bus Bit 15-0
DAC Output Interface			

Pin Name	Pin Number	I/O type	Description
AVDD33	H13	AP	3.3v Analog Power for DAC
AVSS33	K16	AG	Analog GND for DAC
AVDD25	M17	AP	2.5V Analog Power for DAC
AVSS25	G17	AG	Analog GND for DAC
AVDD33R	J12	AP	3.3 V Analog Power for Channel R
AVSS33R	J11	AG	Analog GND for Channel R
AVDD33G	L16	AP	3.3 V Analog Power for Channel G
AVSS33G	M16	AG	Analog GND for Channel G
AVDD33B	J13	AP	3.3 V Analog Power for Channel B
AVSS33B	J16	AG	Analog GND for Channel B
DVDD25	N17	DP	2.5V Digital Power for DAC
DVSS25	H17	DG	Digital GND for DAC
IOR	J20	O	Channel R Current Output
IOG	J18	O	Channel G Current Output
IOB	J19	O	Channel B Current Output
RSET	J17	I	Full-Scale Adjust Resister
COMP	H19	I	Compensation Pin
VREFIN	H20	I	Voltage Reference Input
VREFOUT	G20	O	Voltage Reference Output
Panel Interface			
VOUT[47:40]	D4,B4,B5,C5,C6,D6, D5,B8	O	Digital Output Interface RED[7:0] Even
VOUT[39:32]	D7,D9,C7,C10,C8, C9,C11,D10	O	Digital Output Interface GREEN[7:0] Even
VOUT[31:24]	C12,D13,C13,A18, A19,B18,C16,A20	O	Digital Output Interface BLUE[7:0] Even
VOUT[23:16]	C17,B19,B20,G18, E18,F19,F18,E20	O	Digital Output Interface RED[7:0] Odd
VOUT[15:8]	D19,D20,E17,H18, F17,E19,G19,F20,	O	Digital Output Interface GREEN[7:0] Odd
VOUT[7:0]	D16,C19,D18,D17, C18,D15,D14,C20	O	Digital Output Interface BLUE[7:0] Odd

Pin Name	Pin Number	I/O type	Description
SCLK	A17	O	Display Pixel Clock
DSCLK	C15	O	Display Pixel Clock Divided by 2
PDSDEN	D12	O	Display Data Enable
PHS	B16	I/O	Display HSYNC output / input for Slave Mode
PVS	B17	I/O	Display VSYNC output / input for Slave Mode
OXIN1	C14	I	Reference Clock 1 for Display Device
OXIN2	D11	I	Reference Clock 2 for Display Device
SDRAM Interface			
MDATA[47:0]	W13,W12,V13,U13, V18,U12,U18,V14, U19,V16,V17,K17, K18,K19,K20,L20, R19,R18,T18,T17, T19,T20,U20,V20, W20,Y20,U17,V19, W17,W18,W19,Y19, U16,U15,Y18,V15, W14,U11,V12,Y14, Y13,V11,Y11,U8, W10,V10,W9,U9	I/O	SDRAM Data Bus Bit 47-0
MADDR[11:0]	L19,M20,M19,L18, L17,N20,N19,M18, P20,P19,N18,P18	O	SDRAM Address Bit 11-0
PMXIN	R20	I	SDRAM Read Data Input Sampling Clock
BA[1:0]	W16,Y17	O	SDRAM Bank Address Bit 0-1
DQML	U10	O	SDRAM Low Byte Data Mask
DQMH	Y10	O	SDRAM High Byte Data Mask
WEB	U14	O	SDRAM Write Enable
RASB	W15	O	SDRAM Row Address Strobe
CASB	Y16	O	SDRAM Column Address Strobe
CLK	Y15	O	SDRAM reference Clock
CLKE	Y15	O	SDRAM Clock Enable

Pin Name	Pin Number	I/O type	Description
CSB	W11	O	SDRAM Chip Select
Host Interface			
RSTB	C3	I	Reset
HOST_DB[7:0]	B2,V7,W6,V6,U5,Y3,Y2,W2	I/O	Host Data Bus Bit 7-0 of Parallel Port
HOST_WRB	A2	I	Reference Clock of Parallel Port
HOST_RDB	Y7	I	Read/Write Strobe of Parallel Port
HOST_DENB	U7	I	Data Cycle of parallel Port
HOST_MEMB	V9	I	Memory Access Cycle of Parallel Port
HOST_RDYB	Y9	O	Read Data Ready Output of Parallel Port
IREQ	C4	O	Interrupt Output of Parallel Port
GPO0	U4	O	General Output Port 0
GPO1	U3	O	General Output Port 1
GPO2	Y1	O	General Output Port 2
I2C_EN	D8	I	I2C Enable
PLL Interface			
MXIN	B1	I	Crystal Input (14.31818MHz)
MXOUT	A1	O	Crystal Output
P1VDD25	L5	DP	2.5V Pad Ring Power for PLL1
P1VSS25	M5	DG	Pad Ring GND for PLL1
P1AVDD25	K5	AP	Analog Power for PLL1
P1AVSS25	E4	AG	Analog GND for PLL1
P2VDD25	F4	DP	2.5V Pad Ring Power for PLL2
P2VSS25	D3	DG	Pad Ring GND for PLL2
P2AVDD25	G4	AP	Analog Power for PLL2
P2AVSS25	H4	AG	Analog GND for PLL2
DIGITAL POWER / GROUND			
VDD25	E9,E10,E11,E12,P17,R17,T9,T10,T11,T12	DP	Digital Power 2.5V
VSS25	J9,J10,K9,K10,K11,K12,L9,L10,L11,L12	DG	Digital Ground 2.5V

Pin Name	Pin Number	I/O type	Description
	,M9,M10,M11,M12		
VDD33	H8,H9,J8,K8,L8,M8, N8,N9	DP	Digital Power 3.3V
VSS33	H10,H11,H12,K13, L13,M13,N10,N11, N12,N13	DG	Digital Ground 3.3V

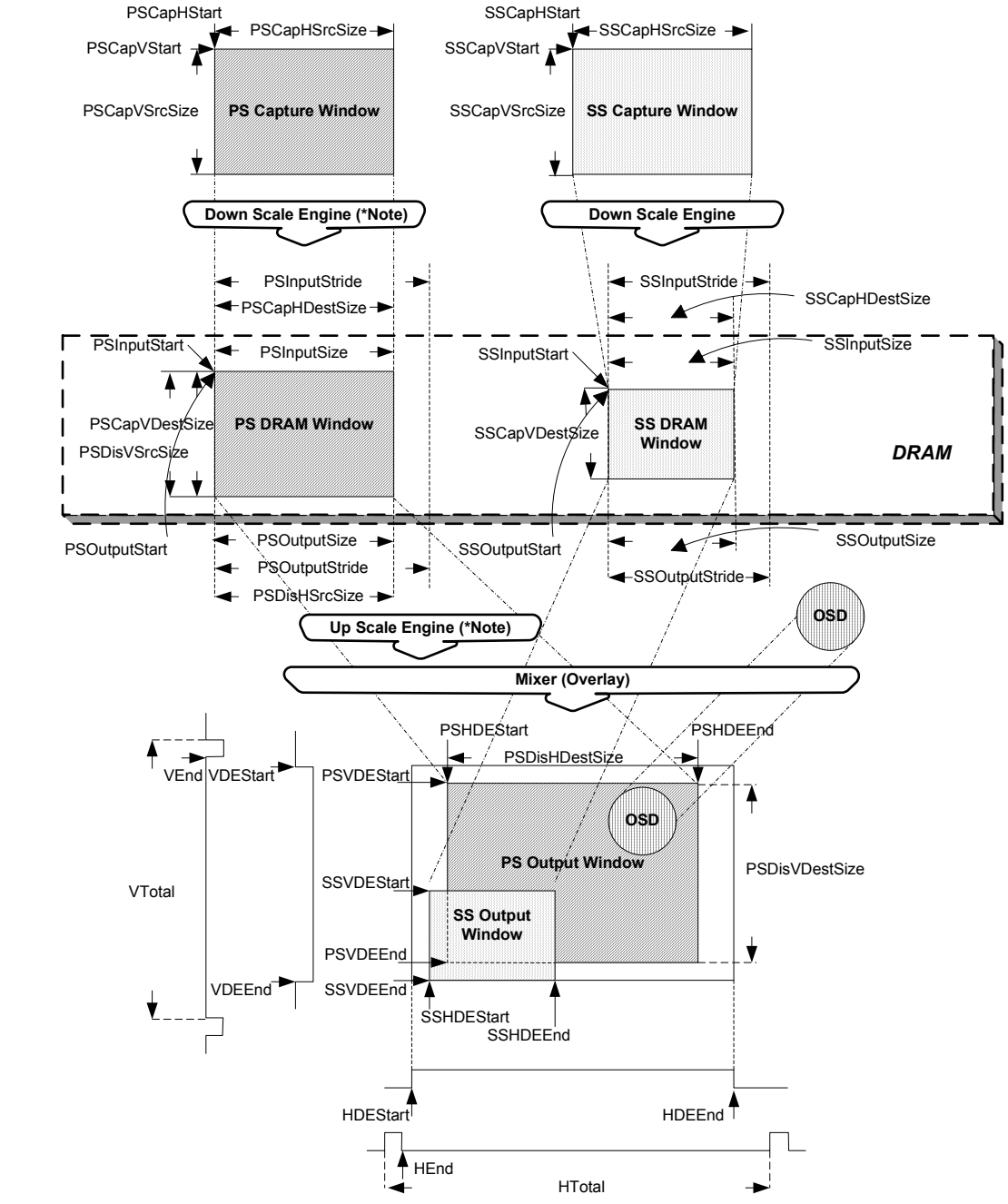
Note: For I/O type, “I”, “O”, “AP”, “AG”, “DP”, and “DG” stand for “Input”, “Output”, “Analog Power”, “Analog Ground”, “Digital Power”, and “Digital Ground” respectively.

8 General Function Description

8.1 Function Blocks

AL310 provide a fully programmable structure allowing video stream process more flexible. The AL310 data process is executed by parsing in the modules such as capture, down scale, memory, up scale and mixer. In each module, data will be manipulated corresponding to the setting of registers. Due to the lack of the number of registers, some registers require banking to other page for access. There are 4 group registers, base control registers, capture control registers, memory control registers and display control registers. The value of base register 0eh determines which group of registers is taken effect. If register 0eh is programmed to value 00, the group of base control registers is chosen; and the register 0eh with value 01 is for capture register group, value 02 is for memory register group and value 03 is for display register group. The register 0eh must be set to corresponding value before that group of register can be accessed.

Register	Group ID	Group register Description		Symbol	Example
0Eh	<1:0>	00	Access only base control registers	BAS#	BAS#16
		01	Access capture and base control registers	CAP#	CAP#20
		10	Access memory and base control registers	MEM#	MEM#20
		11	Access display and base control registers	DIS#	DSP#20



* Note: Primary Stream process supports Down Scale or Up Scale, it can't do both at the same time

Primary Stream and Secondary Stream processing parse and defined registers

8.2 VIU (Video Input Unit)

AL310 supports triple input ports for PIP overlaying. Main-channel accepts RGB/YUV 24/16/8bit and Sub-channel accepts 16/8bit YUV 4:2:2 video data stream with ITU-R-656/601 standards. Applying AverLogic Proprietary Scaling algorithm, the video stream can be scaled down to accommodate required output resolutions with high quality scaling effect. The high quality scaling engine also ensures full screen output display.

For PC Graphics input, AL310 provides Auto-adjustment function to adjust Phase, and Position automatically.

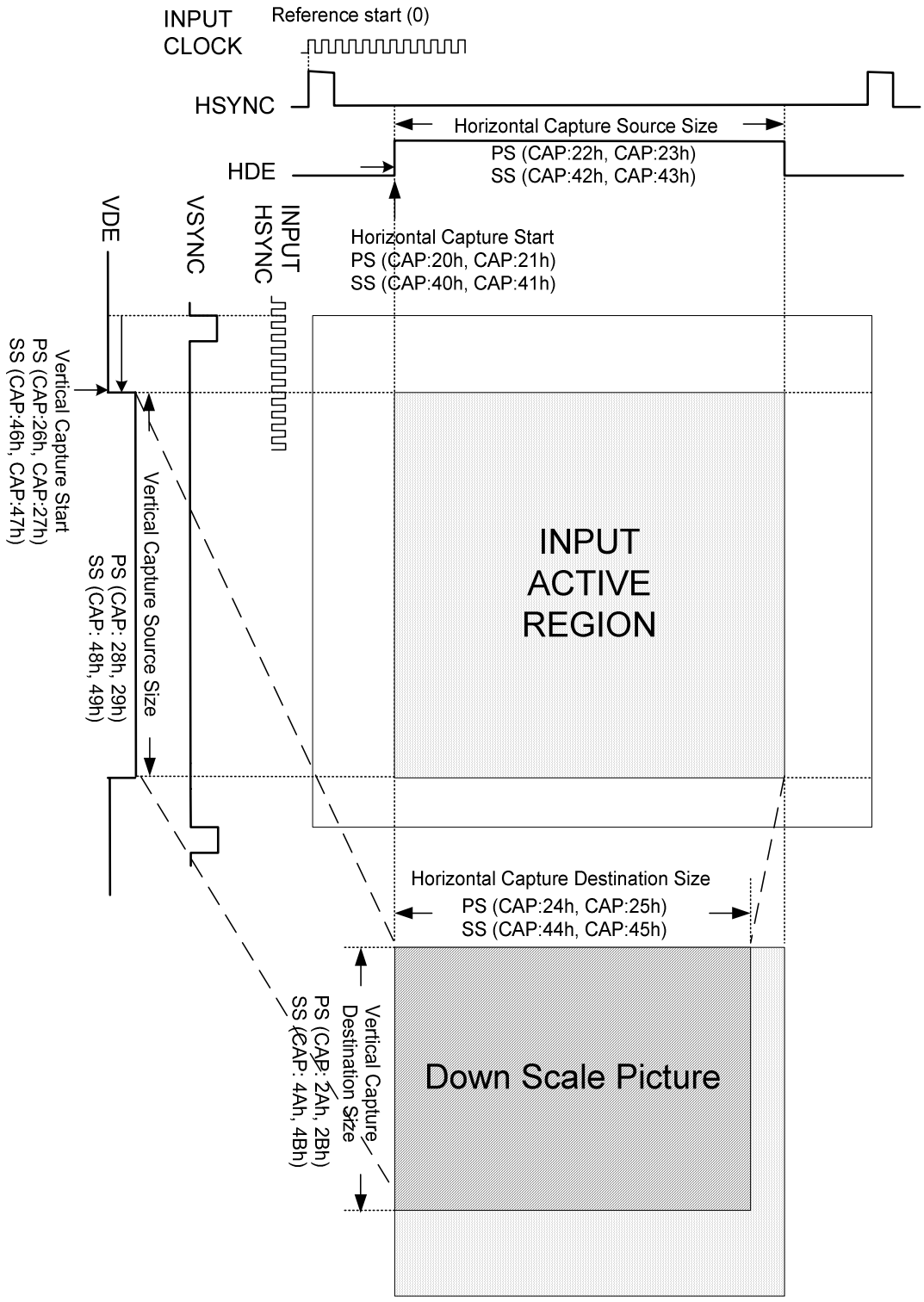
8.2.1 Input Data Format

The AL310 is an integrated video processor that automatically detects and converts multiple graphics & video formats. The AL310 recognized the input data streams as primary and secondary. The Index and Base registers provide user an expansion of the control registers, which implements easy control of the input and the desired output format. The Base registers control the input type and target format.

The AL310 accepts four data formats: 24bit RGB, 8-bit ITU-R BT.656 (CCIR656), 16-bit CCIR601 422 and 24-bit CCIR601 444 data. The clock and sync signal pins separate for RGB or YUV while the YUV data share the same pins as RGB data. For detailed applications, please refer to AL310 Application Notes.

8.2.2 Video Capture and Down Scale Engine

The AL310 has a high-quality scaling engine performing proprietary scaling operations independently in both Horizontal and Vertical direction with 4-line, high precision interpolation.



AL310 Input/Capture timing and Down Scale

8.2.3 Automatic Positioning Registers

The AL310 can detect and report input capture timing for Auto-adjustment function. It detects the starting and ending positions of active video in both direction (Horizontal and Vertical) and ensures the output fit properly into the display region. The data threshold value defines the sensibility of valid data. The capture data will be sampled and qualified base upon the value of data threshold, so that it can determine the starting point and ending point of an active line or an active frame.

8.2.4 PLL Programming for Memory and Display Clock

AL310 embedded 2 independent 200MHz PLL-Based Clock Generator. One is used to generate SDRAM clock (CLK, pin Y15), the other is for output clock (SCLK, pin A17). They are all reference input clock from XIN (generally 14.318MHZ).

There are 3 operation modes in defined in PLL register: Power Down Mode, Bypass Mode and Normal Mode. Power Down Mode forces FOUT to low and PLL in low power consumption state (<10uW). Bypass Mode provides FOUT with the same frequency as FIN. Normal Mode synthesizes FOUT by programming suitable divider values. It needs a Tready time (Pull_in Time + Locking Time) for PLL to re-lock the FIN clock when PLL wakes up from Power Mode to Normal Mode. In general, it should be reserved a Tread time for re-locking when PLL is changed to Normal Mode from Power Mode or Bypass Mode, or when any divider setting is changed.

8.3 MIU (Memory Interface Unit)

MIU supports SDRAM 48/32bit bus width interface. AL310 supports various SDRAM configurations, such as 1Mx16, 2ea or 3ea. It uses sequential Burst mode to control SDRAM memory that operates at minimum 100MHz of clock frequency. For detail operation of SDRAM, please reference memory specifications.

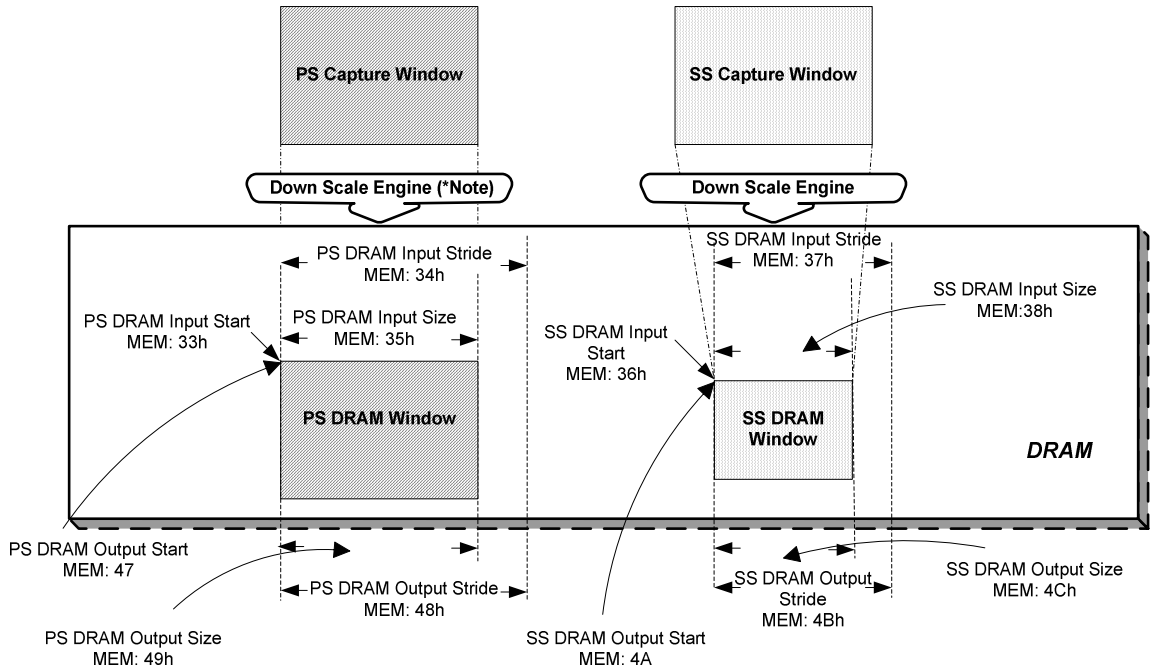
8.3.1 DRAM Bandwidth Consideration

The AL310 uses external DRAMS for the purpose of frame rate conversion between the input video and the output video device. The frame rate conversion for video is done by

double buffering. However, for graphics, double buffering is disabled for most of the time less motion happens in graphics.

8.3.2 DRAM Input/Output Windows

The proceeding diagrams will describe the DRAM input control.



Primary Stream and Secondary Stream memory managing

The DRAM input data size depends on the horizontal capture destination size.

After the input data size has been defined, the memory address of input data can be determined by the register DRAM input stride. The DRAM input stride can be programmed to provide extra memory space for input data.

8.4 VPU (Video Processing Unit)

AL310 identifies video input sources including Progressive Film (24/25 fames/sec) and Interlaced Video (50/60 fields/sec) and selects appropriate de-interlacing algorithm for video enhancement. VPU supports Film Detection with Inverse 3:2 or 2:2 Pull Down and AverLogic Proprietary Deinterlacing. When AL310 detects the video source as Film, then progressive scan frames will be reassembled and output twice input rate such as 50/60 frame/sec. Otherwise, it will be taken as Interlaced Video Source, and processed by using Deinterlacing to reduce video artifacts. The scaling engine offers Scale-Up effect by applying AverLogic's proprietary scaling algorithm. It supports independent Scale-Up in both Horizontal and Vertical direction with 4-line, high precision interpolation. The Sharpness Control provides good effect for image enhancement. It also provides Keystone function for Projector application.

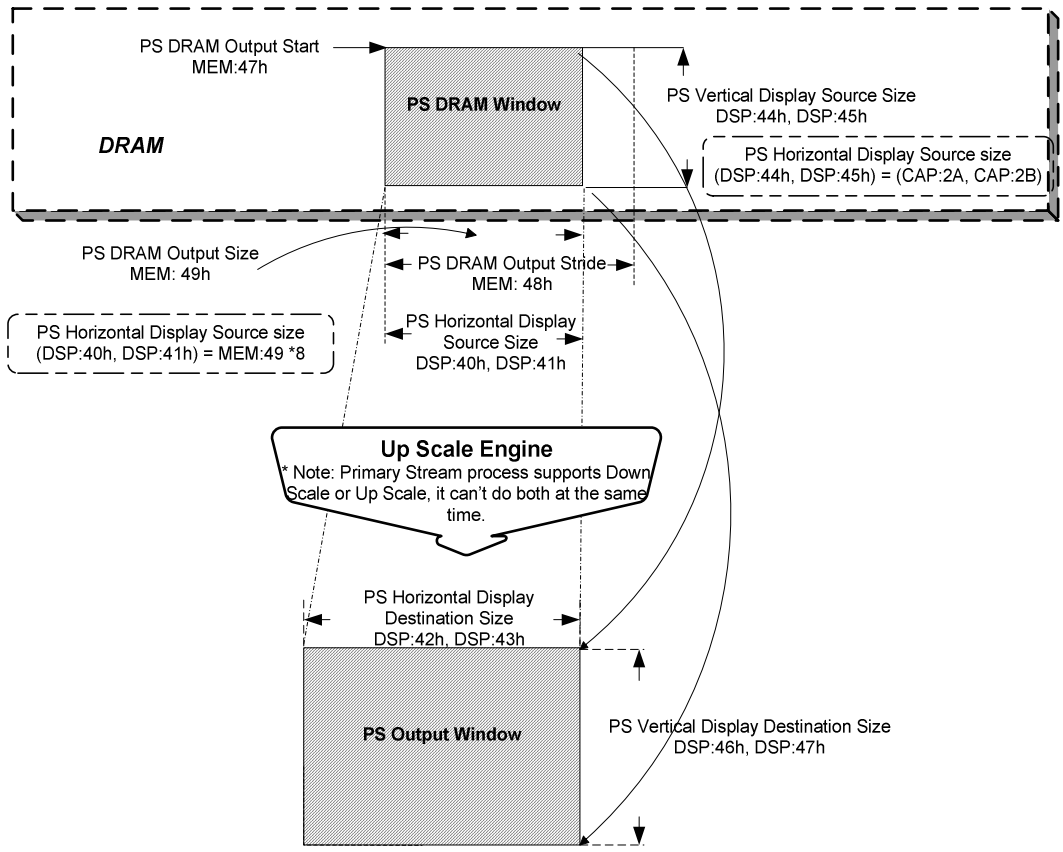
8.4.1 Video De-Interlaced with Film Detection and Motion Adaptive

Video Processing unit equips a high quality deinterlacing algorithm to optimize the output progressive scan frame by recovering film sequence and compensating motion effect during the deinterlacing process. The motion estimation can evaluate both Y/C data or Y data by setting register. In Motion Adaptive process, the sensitivity of the data estimation can be adjusted by register for Luma and Chroma threshold. In film video, such as DVD movie, some duplicate fields are inserted into the interlaced video stream. Original film sequence detection and recovery can produce a smooth progressive scan frame transition after deinterlaced.

8.4.2 Up Scale Engine

The Up Scale Engine can scale up Primary Stream to higher resolution in high quality for output display. The AL310 adapts FIR scaling engine that can do horizontal and vertical up scale independently. The primary stream picture can be either down scale to smaller size of picture or up scale to larger size of picture from original capture (input) picture for output, but it can not do both up and down scale process at the same time. Consider to capture full picture of input data if the output resolution of primary stream picture is going to be enlarged.

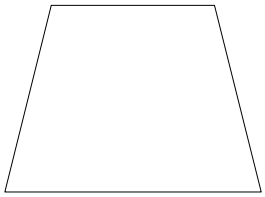
Following block diagram illustrates the define registers of source primary stream window and destination up scale window.



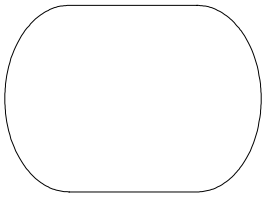
Primary Stream Up scale block diagram and defined registers

8.4.3 Keystone Up Scale Engine

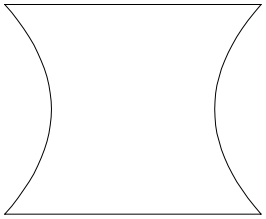
The AL310 can scale up the image in dynamic ratio which is good for projector image correction. The projected images from the projector sometimes show as Figure due to the misalignment or cheap optics. The AL310 can up scale picture in dynamic ratios which are loaded from pre-stored at internal FIFO buffers. The keystone is designed to compensate the distortions, such as figures following.



distortion 1



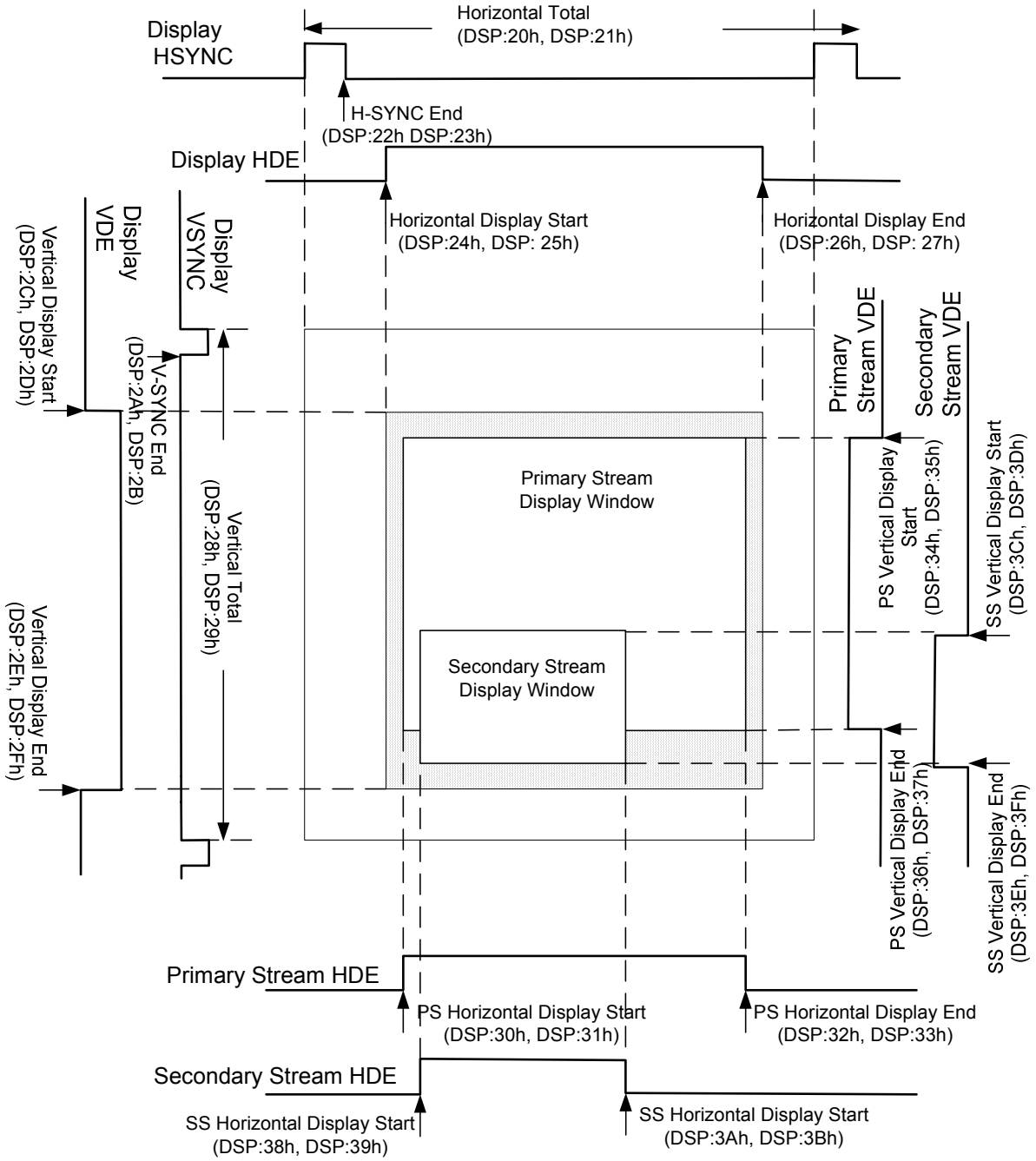
distortion 2



distortion 3

8.5 VOU (Video Output Unit)

Two independent On-Screen-Display (OSD) windows provide overlay for a control menu, text, or caption on the output display. The AL310's OSD is very flexible in the way that the font, size, and display location are all programmable. The internal 2K byte SRAM provides storage for the OSD information. The OSD can be operated with only this internal SRAM or with an external ROM to store font tables or even larger bitmaps. Built-in 8bit Programmable Gamma Look-Up Table for each input color channel for Gamma Correction. It may be used for RGB Contrast, Brightness and Color Temperature adjustments. Dithering is performed to retain color resolution for LCD panels that support 18-bit color depths. AL310 provides Digital video output interface that can be directly connected to 24bit TFT LCD Panel or DVI/LVDS Transmitters. It also provides Analog video output which can support SXGA resolution.



AL310 Output timing and display windows

8.5.1 PIP Overlaying

In the primary stream, select either PS image or PS background color to show on the PS

display region. In proportion to the SS image or SS background color show on the SS display region. On the overlay area of PS & SS is a blending region. If PS and SS don't fill up the display screen, the desktop color is showed on other areas. The Figure 3 Display Screen shows the location of different combination from input image or internal color generator.

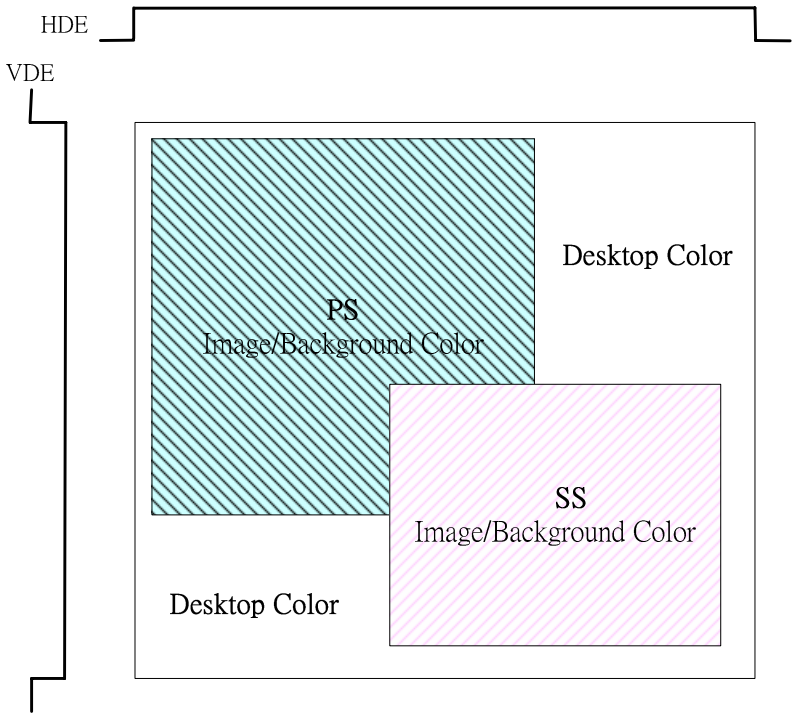


Figure 3 Display Screen

8.5.2 OSD

Two independent On-Screen-Display (OSD) windows provide overlay for a control menu, text, or caption on the output display. The AL310's OSD is very flexible in the way that the font, size, and display location are all programmable. The internal 2K byte SRAM provides storage for the OSD information. The OSD can be operated with only this internal SRAM or with an external ROM to store font tables or even larger bitmaps.

Regarding the detailed usage, please refer to AL310's OSD Application Note.

8.5.3 LUT (Look up table for Gamma Correction and Color Enhancement)

Because of the different characteristics of TV's and PC monitors, direct color space conversion from TV to PC may not show the same color that the human eye sees from the original video on the TV. The contrast may not be sufficient, and the hue may not be accurate, so to resolve these issues the AL310 has a gamma correction internal LUT implemented.

The AL310 provides programmable registers for implementing the LUT. The directly converted colors are sent to the LUT that then sends out the mapped, corrected colors.

The user can program the LUT based on his/her own experiments on specific types of monitors. The typical input-output mapping curve is usually somewhat like the following:

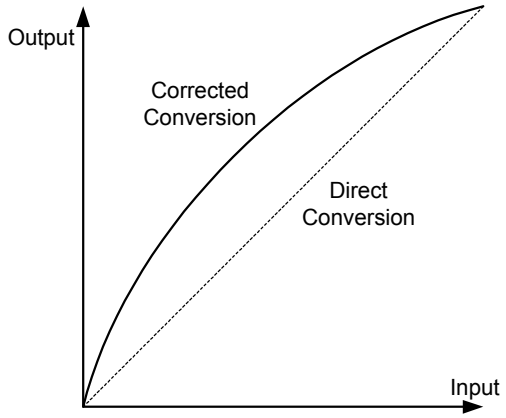


Figure 11 LUT Mapping

8.5.4 Dithering

The AverLogic offers dithering technique that simulates display of colors that are not in the current color space of a particular image. The Dithering logic provides additional color depth enhancement to retain color resolution for LCD panels that support 18-bit color depth.

8.5.5 Dual Output

The AL310 supports both digital and analog output interfaces that provide flexible output mode selections according to different user desire.

8.6 BIU (Bus Interface Unit)

It supports I^2C serial and parallel port programming interfaces. I^2C serial interface requires two wires to access while the parallel port interface needs 11 wires. The communication speed of proprietary parallel interface is much faster than I^2C serial interface.

Regarding to the detailed usage, please refer to AL310's General Application Note.

9 Register Definition & Description

Registers are provided to setup AL310. These registers can be programmed via host interface. The host interface protocol is illustrated in “Host Interface” paragraph. The application notes will describe more detailed settings about these registers. Upon request, AverLogic will provide the sample code or tool of host interface control software.

9.1 Register Set

Register Name	Address	R/W	Default	Function
Base Control Group Registers				
COMPANYID	00h	R	46h	Company ID
INTRMASK	02h	R/W	00h	Interrupt Mask
INTRSTATUS	03h	R/W	00h	Interrupt Vector and Mode
CAPCTRL	06h	R/W	00h	Capture Data Control
DISCTRL1	07h	R/W	00h	Display Data Control 1
DISCTRL2	08h	R/W	00h	Display Data Control 2
POLARITYCTRL	09h	R/W	00h	Display Polarity Control
OTIMECTRL	0Ah	R/W	00h	Display Timing Control
GROUPACCESS	0Eh	R/W	00h	Group Access ID
BOARDCFG	10h	R/W	00h	Board Configuration
INSRCFORMAT	11h	R/W	00h	Input Video Source Format
INPUTCTRL	12h	R/W	00h	Input Control
HREFDLY	13h	R/W	00h	Horizontal Reference Delay
PSSSCTRL	14h	R/W	00h	PS and SS control
SSCTRL	15h	R/W	00h	SS input control
PSCTRL	16h	R/W	00h	PS input control
MEMACCR	17h	R/W	00h	Memory Access Control
INVMSB	18h	R/W	00h	Inverted MSB of PS & SS
PLLSETR	1Bh	R/W	00h	PLL Setting for Memory and Display
MPLLNF	1Ch	R/W	00h	LSB of NF Value for Memory PLL
MPLLNRO	1Dh	R/W	00h	MSB of NF/NR/NO Value for Memory PLL
OPLLNF	1Eh	R/W	00h	LSB of NF Value for Display PLL
OPLLNRO	1Fh	R/W	00h	MSB of NF/NR/NO Value for Display PLL
Capture Control Group Registers*(Accessible when BAS#0E = 01h)*				

Register Name	Address	R/W	Default	Function
PS Timing				
CAPPSHSTART	21h & 20h	R/W	00h	PS Horizontal Capture Start
CAPPSHSRCSIZE	23h & 22h	R/W	00h	PS Horizontal Capture Source Size
CAPPSHDESTSIZE	25h & 24h	R/W	00h	PS Horizontal Capture Destination Size
CAPPSVSTART	27h & 26h	R/W	00h	PS Vertical Capture Start
CAPPSVSRCSIZE	29h & 28h	R/W	00h	PS Vertical Capture Source Size
CAPPSVDESTSIZE	2Bh & 2Ah	R/W	00h	PS Vertical Capture Destination Size
PSINTERLACECTRL	2Eh	R/W	00h	PS Interlace Control
PSHDNRATIO	31h & 30h	R/W	00h	PS Horizontal Scale Down Ratio
PSVDNRATIO	33h & 32h	R/W	00h	PS Vertical Scale Down Ratio
VBI Input Timing				
VBIVSTART	34h	R/W	00h	VBI Vertical Capture Start
VBIVEND	35h	R/W	00h	VBI Vertical Capture End
VBIHSTART	36h	R/W	00h	VBI Horizontal Capture Start
VBIHSIZE	37h	R/W	00h	VBI Horizontal Capture Size
ITU-656 Detection				
PS656HSTART	38h	R/W	20h	PS ITU656 data Horizontal sync start
PS656HEND	39h	R/W	A0h	PS ITU656 data Horizontal sync end
PS656VSTART	3Ah	R/W	02h	PS ITU656 data Vertical sync start
PS656VEND	3Bh	R/W	04h	PS ITU656 data Vertical sync end
SS656HSTART	3Ch	R/W	20h	SS ITU656 data Horizontal sync start
SS656HEND	3Dh	R/W	A0h	SS ITU656 data Horizontal sync end
SS656VSTART	3Eh	R/W	02h	SS ITU656 data Vertical sync start
SS656VEND	3Fh	R/W	04h	SS ITU656 data Vertical sync end
SS Input Timing				
CAPSSHSTART	41h & 40h	R/W	00h	SS Horizontal Capture Start
CAPSSHSRCSIZE	43h & 42h	R/W	00h	SS Horizontal Capture Source Size
CAPSSHDESTSIZE	45h & 44h	R/W	00h	SS Horizontal Capture Destination Size
CAPSSVSTART	47h & 46h	R/W	00h	SS Vertical Capture Start
CAPSSVSRCSIZE	49h & 48h	R/W	00h	SS Vertical Capture Source Size
CAPSSVDESTSIZE	4Bh & 4Ah	R/W	00h	SS Vertical Capture Destination Size
SSINTERLACECTRL	4Eh	R/W	00h	SS Interface Control

Register Name	Address	R/W	Default	Function
SSDOWNHFILTER	4Fh	R/W	00h	SS Scale Down Horizontal filter taps
Position Detection				
POSDATATH	51h	R/W	00h	Data Threshold for Position Detection
POSHDESTART	5Bh & 5Ah	R		Horizontal Active Start
POSHDEEND	5Dh & 5Ch	R		Horizontal Active End
POSVDESTART	5Fh & 5Eh	R		Vertical Active Start
POSVDEEND	61h & 60h	R		Vertical Active End
Mode Detection				
CAPPSHTOTALCNT	63h & 62h	R		PS Horizontal Total Counter
CAPPSVTOTALCNT	65h & 64h	R		PS Vertical Total Counter
CAPSSHTOTALCNT	67h & 66h	R		SS Horizontal Total Counter
CAPSSVTOTALCNT	69h & 68h	R		SS Vertical Total Counter
PSDBUFFLAGNUML	70h	R/W	00h	PS Double Buffer Flag Number LSB
SSDBUFFLAGNUML	71h	R/W	00h	SS Double Buffer Flag Number LSB
DBUFFLAGNUMH	72h	R/W	00h	PS & SS Double Buffer Flag Number MSB
TUNEPCCLK	73h	R/W	00h	Tune Input PC Clock Timing
TUNEV1CLK	74h	R/W	00h	Tune Input V1 Clock Timing
TUNEV2CLK	75h	R/W	00h	Tune Input V2 Clock Timing
Memory Control Group Registers*(Accessible when reg.0Eh = 02h)*				
DRAM Control				
DRAMACCESSCTRL	20h	R/W	00h	DRAM Access control
DRAMWRITE	21h	R/W	00h	DRAM Write
FIFOCONTROL	22h	R/W	00h	SS FIFO Control
FIFOCONTROL	23h	R/W	00h	PS Input FIFO Control
DRAMMINREFRESH	28h	R/W	00h	DRAM Minimum Refresh
DRAMCTRL	2Ah & 29h	R/W	00h	DRAM Control Register
DRAMRADDR	2Dh ~ 2Bh	R/W	00h	DRAM Read Address
SKIPMODE	32h	R/W	10h	Skip Mode
DRAM Input Control				
DRAMPSISTART	33h	R/W	10h	PS DRAM Input Start
DRAMPSISTRIDE	34h	R/W	00h	PS DRAM Input Stride
DRAMPSISIZE	35h	R/W	00h	PS DRAM Input Size

Register Name	Address	R/W	Default	Function
DRAMSSISTART	36h	R/W	00h	SS DRAM Input Start
DRAMSSISTRIDE	37h	R/W	00h	SS DRAM Input Stride
DRAMSSISIZE	38h	R/W	00h	SS DRAM Input Size
DRAM Window Copy Control				
WCSRCSTART	3Bh ~ 39h	R/W	00h	Window Copy Source Start
GSDRAMINPUTSTRIDE	3Ch	R/W	00h	Window Copy Source Stride
GSDRAMINPUTSIZE	3Dh	R/W	00h	Window Copy HSize
WCSTRIDE	3Eh	R/W	00h	Direct Write Stride
WCDESTSTART	41h ~ 3Fh	R/W	00h	Window Copy Destination Start
DASTART	44h ~ 42h	R/W	00h	Direct Read/Write Address
WCSIZE	45h	R/W	00h	Window Copy Size
WCLINETOTAL	46h	R/W	00h	Window Copy Line Total
DRAM Output Window Control				
DRAMPSOSTART	47h	R/W	00h	PS DRAM Output Start
DRAMPSOSTRIDE	48h	R/W	00h	PS DRAM Output Stride
DRAMPSOSIZE	49h	R/W	00h	PS DRAM Output Size
DRAMSSOSTART	4Ah	R/W	00h	SS DRAM Output Start
DRAMSSOSTRIDE	4Bh	R/W	00h	SS DRAM Output Stride
DRAMSSOSIZE	4Ch	R/W	00h	SS DRAM Output Size
VBISTART	4Fh ~ 4Dh	R/W	00h	VBI Starting Address
FRONTM	50h	R/W	00h	
TUNEMCLK	51h	R/W	00h	Tune Memory Write Clock Timing
TUNEPMCLK	52h	R/W	00h	Tune Memory Read Clock Timing
DRAM Data Port				
READSTATUS	60h	R		Read Status
BYTE0	61h	R/W	00h	Byte 0
BYTE1	62h	R/W	00h	Byte 1
BYTE2	63h	R/W	00h	Byte 2
BYTE3	64h	R/W	00h	Byte 3
BYTE4	65h	R/W	00h	Byte 4
BYTE5	66h	R/W	00h	Byte 5
Display Control Group Registers *(Accessible when reg.0Eh = 03h)*				

Register Name	Address	R/W	Default	Function
Display Timing				
DISHTOTAL	21h ~ 20h	R/W	00h	Display Horizontal Total
DISHSEND	23h & 22h	R/W	00h	Display Horizontal Sync
DISHDESTART	25h & 24h	R/W	00h	Horizontal Display Start
DISHDEEND	27h & 26h	R/W	00h	Horizontal Display End
DISVTOTAL	29h & 28h	R/W	00h	Display Vertical Total
DISVSEND	2Bh & 2Ah	R/W	00h	Display Vertical Sync
DISVDESTART	2Dh & 2Ch	R/W	00h	Vertical Display Start
DISVDEEND	2Fh & 2Eh	R/W	00h	Vertical Display End
Window Output Timing				
DISPSHDESTART	31h & 30h	R/W	00h	PS Horizontal Display Start
DISPSHDEEND	33h & 32h	R/W	00h	PS Horizontal Display End
DISPSVDESTART	35h & 34h	R/W	00h	PS Vertical Display Start
DISPSVDEEND	37h & 36h	R/W	00h	PS Vertical Display End
DISSSHDESTART	39h & 38h	R/W	00h	SS Horizontal Display Start
DISSSHDEEND	3Bh & 3Ah	R/W	00h	SS Horizontal Display End
DISSSVDESTART	3Dh & 3Ch	R/W	00h	SS Vertical Display Start
DISSSVDEEND	3Fh & 3Eh	R/W	00h	SS Vertical Display End
Zoom In Control Registers				
DISPSHSRCSIZE	41h & 40h	R/W	00h	PS Horizontal Display Source Size
DISPSHDESTSIZE	43h & 42h	R/W	00h	PS Horizontal Display Destination Size
DISPSVSRCSIZE	45h & 44h	R/W	00h	PS Vertical Display Source Size
DISPSVDESTSIZE	47h & 46h	R/W	00h	PS Vertical Display Destination Size
PSZOOMFCTRL	48h	R/W	00h	PS Zoom In Filter Control
PSHUPRATIO	4Bh & 4Ah	R/W	00h	PS Horizontal Scale Up Ratio
DELTAHUPRATIO	4Bh & 4Ah	R/W	00h	Delta PS Horizontal Scale Up Ratio *Note: This definition is valid when DIS#CB<4> ='1' and used in Keystone*
PSVUPRATIO	4Dh & 4Ch	R/W	00h	PS Vertical Scale Up Ratio
PSHPHASE	4Fh & 4Eh	R/W	00h	PS Horizontal Scale Up Initial Phase
PSVPHASE	51h & 50h	R/W	00h	PS Vertical Scale Up Initial Phase
OUTPUTMODE	54h	R/W	00h	Output Mode

Register Name	Address	R/W	Default	Function
LUTINDEX	55h	R/W	00h	LUT Write Index
LUTRED	5Ch	R/W	00h	LUT Red Color LSB
LUTGREEN	5Dh	R/W	00h	LUT Green Color LSB
LUTBLUE	5Eh	R/W	00h	LUT Blue Color LSB
LUTCOLOR	5Fh	R/W	00h	LUT Color MSB and Read/Write Trigger
PATTERNGEN	56h	R/W	00h	Pattern Generator and GPO
OSD Color Registers				
OSDRAMWADDR	59h & 58h	R/W	00h	OSD Write Address
OSDRAMWDATA	5Ah	W	00h	OSD Write Data Port
COLOR0RED	60h	R/W	00h	Color 0 Red
COLOR0GREEN	61h	R/W	00h	Color 0 Green
COLOR0RED	62h	R/W	00h	Color 0 Blue
COLOR1RED	63h	R/W	00h	Color 1 Red
COLOR1GREEN	64h	R/W	00h	Color 1 Green
COLOR1BLUE	65h	R/W	00h	Color 1 Blue
COLOR2RED	66h	R/W	00h	Color 2 Red
COLOR2GREEN	67h	R/W	00h	Color 2 Green
COLOR2BLUE	68h	R/W	00h	Color 2 Blue
COLOR3RED	69h	R/W	00h	Color 3 Red
COLOR3GREEN	6Ah	R/W	00h	Color 3 Green
COLOR3BLUE	6Bh	R/W	00h	Color 3 Blue
COLOR4RED	6Ch	R/W	00h	Color 4 Red
COLOR0GREEN	6Dh	R/W	00h	Color 4 Green
COLOR4BLUE	6Eh	R/W	00h	Color 4 Blue
COLOR5RED	6Fh	R/W	00h	Color 5 Red
COLOR5GREEN	70h	R/W	00h	Color 5 Green
COLOR5BLUE	71h	R/W	00h	Color 5 Blue
COLOR6RED	72h	R/W	00h	Color 6 Red
COLOR6GREEN	73h	R/W	00h	Color 6 Green
COLOR6BLUE	74h	R/W	00h	Color 6 Blue
COLOR7RED	75h	R/W	00h	Color 7 Red
COLOR7GREEN	76h	R/W	00h	Color 7 Green

Register Name	Address	R/W	Default	Function
COLOR7BLUE	77h	R/W	00h	Color 7 Blue
OSD Control Registers				
OSDCOLORSEL	78h	R/W	00h	OSD Color Select
BLINKTIME	79h	R/W	00h	OSD Blink Timer
OSDMODE	80h	R/W	00h	OSD Modes
FOREOP	81h	R/W	00h	Logic Operation 1
FOREOP	83h	R/W	00h	Logic Operation 2
FADEALPHA	82h	R/W	00h	Fading Alpha Value
OSD1 Registers				
OSDCONTROL1	84h	R/W	00h	OSD1 Control
ROMSTARTADDR1	85h	R/W	00h	OSD1 ROM Start Address
FONTADDRUNIT1	86h	R/W	00h	OSD1 Font Address Unit
OSDHSTART1	90h	R/W	00h	OSD1 Horizontal Start
OSDVSTART1	91h	R/W	00h	OSD1 Vertical Start
RAMADDRST1	92h	R/W	00h	OSD1 RAM Start Address
RAMSTRIDE1	8Bh & 93h	R/W	00h	OSD1 RAM Horizontal Stride
BMAPHSIZE1	95h & 94h	R/W	00h	OSD1 Bitmap Horizontal Size
BMAPHTOTAL1	97h & 96h	R/W	00h	OSD1 Bitmap Horizontal Total Pixels
BMAPVSIZE1	99h & 98h	R/W	00h	OSD1 Bitmap Vertical Size
BMAPVTOTAL1	9Bh & 9Ah	R/W	00h	OSD1 Bitmap Vertical total Lines
ICONHTOTAL1	9Ch	R/W	00h	OSD1 Icon Horizontal Total
ICONVTOTAL1	9Dh	R/W	00h	OSD1 Icon Vertical Total
FONTLINESIZE1	AEh	R/W	00h	OSD1 Font Line Size
OSD2 Registers				
OSDCONTROL2	88h	R/W	00h	OSD2 Control
ROMSTARTADDR2	89h	R/W	00h	OSD2 ROM Start Address
FONTADDRUNIT2	8Ah	R/W	00h	OSD2 Font Address Unit
OSDHSTART2	A0h	R/W	00h	OSD2 Horizontal Start
OSDVSTART1	A1h	R/W	00h	OSD2 Vertical Start
RAMADDRST2	A2h	R/W	00h	OSD2 RAM Start Address
RAMSTRIDE2	8Ch & A3h	R/W	00h	OSD2 RAM Horizontal Stride
BMAPHSIZE2	A5h & A4h	R/W	00h	OSD2 Bitmap Horizontal Size

Register Name	Address	R/W	Default	Function
BMAPHTOTAL2	A7h & A6h	R/W	00h	OSD2 Bitmap Horizontal Total Pixels
BMAPVSIZE2	A9h & A8h	R/W	00h	OSD2 Bitmap Vertical Size
BMAPVTOTAL2L	ABh & AAh	R/W	00h	OSD2 Bitmap Vertical Total Lines
ICONHTOTAL2	ACh	R/W	00h	OSD2 Icon Horizontal Total
ICONVTOTAL2	ADh	R/W	00h	OSD2 Icon Vertical Total
FONTLINESIZE2	AFh	R/W	00h	OSD2 Font Line Size
Alpha Blending Registers				
MIXERCONFIG	B0h	R/W	00h	Mixer Configuration
PSALPHA	B1h	R/W	00h	PS Alpha Value
SSALPHA	B2h	R/W	00h	SS Alpha Value
DESKR	B3h	R/W	00h	Desktop Color Component Red
DESKG	B4h	R/W	00h	Desktop Color Component Green
DESKB	B5h	R/W	00h	Desktop Color Component Blue
PSBACKR	B6h	R/W	00h	PS Background Color Component Red
PSBACKG	B7h	R/W	00h	PS Background Color Component Green
PSBACKB	B8h	R/W	00h	PS Background Color Component Blue
SSBACKR	B9h	R/W	00h	SS Background Color Component Red
SSBACKG	BAh	R/W	00h	SS Background Color Component Green
SSBACKB	BBh	R/W	00h	SS Background Color Component Blue
CHROMAR	BCh	R/W	00h	Chroma Color Component Red
CHROMAG	BDh	R/W	00h	Chroma Color Component Green
CHROMAB	BEh	R/W	00h	Chroma Color Component Blue
Film Detection/ Motion Adaptive Registers				
MOTIONCNTTH	C5h & C4h	R/W	00h	Motion Counter Threshold
LUMATH	C6h	R/W	00h	Lumina(Y) Threshold
CHROMATH	C7h	R/W	00h	Chroma(C) Threshold
MCCTRL	C8h	R/W	00h	De-interlacing Control Register
FILMCTRL	C9h	R/W	00h	Film Detection Control Register
PHASECTRL	CAh	R/W	00h	Phase Detection Control Register
MVCNT	CFh & CEh	R/W	00h	Motion Pixel Numbers
Keystone Registers				
SHPKEYCTRL	CBh	R/W	00h	Sharpness/Keystone Control Register

Register Name	Address	R/W	Default	Function
MVCNTL	C0h	R/W	00h	Keystone Parameters Address LSB
MVCNTH	C1h	R/W	00h	Keystone Parameters Address MSB
Tri-Level Sync Registers				
TRISYNCA	D0h	W	00h	Tri-Level Sync Parameter Period a
TRISYNCB	D1h	W	00h	Tri-Level Sync Parameter Period b
TRISYNCD1	D2h	W	00h	Tri-Level Sync Parameter Delta 1
TRISYNCD2	D3h	W	00h	Tri-Level Sync Parameter Delta 2
TRISYNCBLANK	D4h	W	00h	Tri-Level Sync Parameter Period Blank
TRISYNCLEVEL	D7h	W	00h	Tri-Level Sync Level
SS Border Registers				
SSLFSTART	E1h &E0h	W		SS Left Border Start
SSRTSTART	E3h &E2h	W		SS Right Border Start
SSTPSTART	E5h &E4h	W		SS Top Border Start
SSBTSTART	E7h &E6h	W		SS Bottom Border Start
SSBWIDTH	E8h	W		SS Border Width
SSBRED	E9h	W		SS Border Color Red
SSBGREEN	EAh	W		SS Border Color Green
SSBBULE	EBh	W		SS Border Color Blue
Display Parameter Registers				
DISTUNEHS	C2h	R/W		Tune Display Horizontal Sync Phase
DISTUNESCLK	CCh	R/W		Tune Display Pixel Clock Phase
DISTUNEDSCLK	CDh	R/W		Tune Display Pixel Clock by 2 Phase
PHASECTRL	CAh	R/W		Phase Detection Control Register
DISHTOTAL	D8h & D7h	R		Display Horizontal Total
DISVTOTAL	DAh & D9h	R		Display Vertical Total
PHASECNT	DCh & DBh	R		Phase Counter
COLORMANG	F0h	R/W	00h	Enable Brightness/Contrast/Saturation
BRIGHTNESS	F1h	R/W	80h	Brightness Level
CONTRAST	F2h	R/W	40h	Contrast Level
SATURATION	F3h	R/W	40h	Saturation Level

9.2 Register Description

➢ Base Control Group Registers

INDEX (HEX)	Register Name	BITS	Function Description
00	Company ID (R) [COMPANYID]		
	CompanyID	<7:0>	Company ID (46h)
02	Interrupt Mask (R/W) [INTRMASK]		
	DVsyncIntMask	<0>	Display VSYNC interrupt mask
			0 Mask interrupt issued by VSYNC of display
			1 Interrupt issued when display VSYNC is activated
	PSVsyncIntMask	<1>	Capture primary stream VSYNC interrupt mask
			0 Mask interrupt issued by VSYNC of PS
			1 Interrupt issued when VSYNC of PS is activated
	SSVsyncIntMask	<2>	Capture secondary stream VSYNC interrupt mask
			0 Mask interrupt issued by VSYNC of SS
			1 Interrupt issued when VSYNC of SS is activated
	VBlMask	<3>	Display vertical blank interrupt mask
			0 Mask interrupt issued by display vertical blank
			1 Interrupt issued by display vertical blank
	FilmDetMask	<4>	H/W Film detected finished interrupt mask
			0 Mask interrupt issued by film detection
			1 Interrupt issued when HW film detected
	FullDetMask	<5>	FIFO full for directly memory write Interrupt Mask
			0 Mask interrupt issued by FIFO full for directly write to SDRAM
			1 Interrupt issued by FIFO full for directly write to SDRAM
	WCopyEndMask	<6>	Window copy finished interrupt mask
			0 Mask interrupt issued by window copy
			1 Interrupt issued by window copy

FIFOFullMask	<7>	Arbiter FIFO full interrupt mask	
		0	Mask interrupt issued by FIFO index of arbiter
		1	Interrupt issued when FIFO is full

03 Interrupt Vector and Mode (R)(W) [INTRSTATUS]

DVsyncInt (R)	<0>	Display VSYNC interrupt	
PSVsyncInt (R)	<1>	Capture primary stream VSYNC interrupt	
SSVsyncInt (R)	<2>	Capture secondary stream VSYNC interrupt	
VBlInt (R)	<3>	Display vertical blank interrupt	
FilmDet (R)	<4>	H/W Film detected finished interrupt	
FullDet (R)	<5>	FIFO full for directly memory write interrupt	
WCopyEnd (R)	<6>	Window copy finished interrupt	
FIFOFull (R)	<7>	Arbiter FIFO full interrupt	
IntMode(W)	<0>	0	Trigger mode
		1	Level mode
	<1>	0	High active
		1	Low active
	<7:2>	Reserved	

04~05: Reserved

06 Capture Data Control (R/W) [CAPCTRL]

PSVScaleDn	<0>	Primary stream vertical scale down enable	
		0	Disable
		1	Enable
SSVScaleDn	<1>	Secondary stream vertical scale down enable	
		0	Disable
		1	Enable
PSMEM444En	<2>	Primary stream data format stored in frame buffer	
		0	16-bit 4-2-2 format
		1	24-bit 4-4-4 format
SSMEM444En	<3>	Secondary stream data format stored in frame buffer	
		0	16-bit 4-2-2 format
		1	24-bit 4-4-4 format

Reserved	<4>	Tie to 0	
SoGo	<5>	Display timing strboe by PS capture VSYNC	
DRAMBus	<6>	DRAM bus width	
		0	48-bit
		1	32-bit
GO	<7>	Capture timing enable	
		0	Disable
		1	Enable

07 Display Data Control 1 (R/W) [DISCTRL1]

PSDRAMByte	<1:0>	Primary stream data format stored in DRAM	
		00	Reserved
		01	24-bit x 2, RGB888, YCbCr24 or YPbPr24
		10	Reserved
		11	16-bit x 2, RGB565, YCbCr16 or YPbPr16
Reserved	<2>	Reserved	
PSCscEn	<3>	Primary stream data color space conversion	
		0	Disable color space converter
		1	Enable color space converter
SSDRAMByte	<5:4>	Secondary stream data format stored in DRAM	
		00	Reserved
		01	24-bit x 2, RGB888, YCbCr24 or YPbPr24
		10	Reserved
		11	16-bit x 2, RGB565, YCbCr16 or YPbPr16
Reserved	<6>	Reserved	
SSCscEn	<7>	Secondary stream data color space conversion	
		0	Disable color space converter
		1	Enable color space converter

08 Display Data Control 2 (R/W) [DISCTRL2]

PSUVFlip2Path	<0>	PS U/V flip in display data path	
		0	Disable
		1	Enable
PSUVFlip2Mem	<1>	PS U/V flipped in capture data path	

		0	Disable
		1	Enable
	PSRGBEn	<2>	PS input data format, refer to BAS#16<4>
		0	YPbPr input
		1	RGB input
	PSYPbPrEn	<3>	PS color space conversion, refer to BAS#07<3>
		0	YCbCr to RGB conversion
		1	YPbPr to RGB conversion
	SSUVFlip2Path	<4>	SS U/V flip in display path
		0	Disable
		1	Enable
	SSUVFlip2Mem	<5>	SS U/V flipped in capture data path
		0	Disable
		1	Enable
	SSRGBEn	<6>	SS input data format, refer to BAS#15<4>
		0	YPbPr input
		1	RGB input
	SSYPbPrEn	<7>	SS color space conversion, refer to BAS#07<7>
		0	YCbCr to RGB conversion
		1	YPbPr to RGB conversion

09 Display Polarity Control (R/W) [POLARITYCTRL]

	OClkSel	<0>	Output clock source selection as display clock, refer to BAS#09<7>
		0	Select OXIN1 as display clock
		1	Select OXIN2 as display clock
	ControlEn	<1>	Panel output data signals (clock, data, HSYNC, VSYNC and PDE) control enable
		0	Disable output data signals to panel, all output data signals tie to low
		1	Enable panel output data signals
	HSyncPol	<2>	Output horizontal sync polarity
		0	Positive

		1	Negative
	BlankPol	<3>	Output horizontal blank polarity
		0	Positive
		1	Negative
	VSyncPol	<4>	Output vertical sync polarity
		0	Positive
		1	Negative
	InvertOdd	<5>	Invert odd field signal
		0	Positive
		1	Negative
	CSyncOut	<6>	Composite sync out
		0	Separate
		1	Composite
	OPLLSel	<7>	Display reference clock source, refer to BAS#09<0>
		0	From external pin (OXIN1/OXIN2)
		1	From PLL

0A Display Timing Control (R/W) [OTIMECTRL]

	PSWinDisable	<0>	PS window diable
		0	Enable
		1	Disable
	SSWinDisable	<1>	SS window disable
		0	Enable
		1	Disable
	SlaveMode	<2>	Slave mode enable, refer to BAS#0A<3>
		0	Output timing driven by internal registers
		1	Output timing driven by external device(capture or external display device)
	SlaveType	<3>	Slave mode type, refer to BAS#0A<2>
		0	Output timing is driven by capture timing
		1	Output timing is driven by external display device
	CSYNCType	<5:4>	Compsit SYNC type
		00	XOR
		01	AND

		10	NXOR
		11	NAND
	YPbPrAnalogOut	<6>	YPbPr analog output
		0	RGB output
		1	YpbPr output
	YPbPrDigitalOut	<7>	YPbPr digital output
		0	RGB output
		1	YpbPr output

0E Group Access ID (R/W) [GROUPACCESS]

	GroupAccessID	<1:0>	Group register access control
		00	Access only Base control registers
		01	Access Capture and Base control registers
		10	Access Memory and Base control registers
		11	Access Display and Base control registers
	Reserved	<7:2>	Reserved

10 Board Configuration (R/W) [BOARDCFG]

	V1nConfig	<1:0>	Video1 data input pins configuration
		00	VIN pin 24 to pin 47
		01	VIN pin 16 to pin 39
		10	Reserved
		11	Reserved
	Reserved	<7:2>	Reserved

11 Input Video Source Format (R/W) [INSRCFORMAT]

	PCInFormat	<1:0>	Video 0 data input format
		00	24-bit
		01	16-bit
		10	8-bit
		11	Reserved
	V1InFormat	<3:2>	Video 1 data input format
		00	24-bit
		01	16-bit

		10	8-bit
		11	Reserved
	V2InFormat	<5:4>	Video 2 data input format
		00	24-bit
		01	16-bit
		10	8-bit
		11	Reserved
	TriPixPS	<6>	3 pixel per SDRAM cycle for PS
	TriPixSS	<7>	3 pixel per SDRAM cycle for SS

12 Input Control (R/W) [INPUTCTRL]

	Reserved	<2:0>	Tie to “000”
	HsPol	<3>	Enable HS polarity detection
		0	Disable, when turn on auto position function
		1	Enable
	VsPol	<4>	Enable VS polarity detection
		0	Disable, when turn on auto position function
		1	Enable
	Reserved	<7:5>	Reserved

13 Horizontal Reference Delay (R/W) [HREFDLY]

PSHRefDly	<3:0>	Primary stream Capture HRef delay (Unit: psclk)
SSHRefDly	<7:4>	Secondary stream Capture HRef delay (Unit: ssclk)

14 PS & SS control (R/W) [PSSSCTRL]

	PSHScaleDn	<0>	Enable primary stream scale down
	Reserved	<1>	Reserved
	PS656SyncSel	<2>	Primary stream SYNC source when ITU656 input
		0	From external SYNC input pin
		1	From decoded ITU656 data
	PSSoftRef	<3>	Primary stream HREF source
		0	From external HREF input pin
		1	Software programmable
	SSHScaleDn	<4>	Enable secondary stream scale down

Reserved	<5>	Reserved
SS656SyncSel	<6>	Secondary stream SYNC source when ITU656 input
		0 From external SYNC input pin
		1 From decoded ITU656 data
SSSoftRef	<7>	Secondary stream HREF source
		0 From external HREF input pin
		1 Software programmable

15 SS Input control (R/W) [SSCTRL]

SSSrcSel	<1:0>	Select secondary stream input source / Position detection source
		00 Video 0 (PC)
		01 Video 1 (V1)
		10 Video 2 (V2)
		11 Reserved
SSInvOddField	<2>	Invert internal detected secondary stream odd field signal
Reserved	<3>	Reserved
SS444En	<4>	Input secondary stream data format, refer to BAS#08<4>
		0 RGB/YPbPr input format
		1 YCbCr input format
SS656En	<5>	Enable input secondary stream source is ITU656 format
SSDEdgeEn	<6>	Double edge sampling for ITU656 input
Reserved	<7>	Reserved

16 PS Input control (R/W) [PSCTRL]

PSSrcSel	<1:0>	Select primary stream input source
		00 Video 0 (PC)
		01 Video 1 (V1)
		10 Video 2 (V2)
		11 Reserved, tie SYNC and clock signals to 0
PSInvOddField	<2>	Invert internal detected primary stream odd field signal
Reserved	<3>	Reserved
PS444En	<4>	Input primary stream data format, refer to BAS#08<2>
		0 RGB/YPbPr input format

		1	YCbCr input format
	PS656En	<5>	Enable input primary stream source is ITU656 format
	PSDEdgeEn	<6>	Double edge sampling for PS ITU656 input
	Reserved	<7>	Reserved

17 Memory Access Control Register(R/W) [MEMACCR]

	MemWEn	<0>	Directly write enable
	MemREn	<1>	Directly read enable
	HostMode	<2>	Host data mode
		0	2x16-bit per each host cycle
		1	1x24-bit per each host cycle
	HostBus	<3>	Host data bus width, refer to MEM#61~66 port
		0	32-bit Bus
		1	8-bit Bus
	PSOEn	<4>	Data output of directly memory via PS path
	SSOEn	<5>	Data output of directly memory via SS path
	WCopyEn	<6>	Window copy enable
		0	Disable window copy
		1	Enable window copy
	MclkSel	<7>	Memory clock select
		0	Memory clock from external PIN (XIN)
		1	Memory clock from internal PLL

18 Inverted MSB of PS & SS (R/W) [INVMSB]

InvPSBit7	<0>	Inverted bit 7 of PS input data
InvPSBit15	<1>	Inverted bit 15 of PS input data
InvPSBit23	<2>	Inverted bit 23 of PS input data
Reserved	<3>	Reserved
InvSSBit7	<4>	Inverted bit 7 of SS input data
InvSSBit15	<5>	Inverted bit 15 of SS input data
InvSSBit23	<6>	Inverted bit 23 of SS input data
Reserved	<7>	Reserved

Note: Please refer to General Application Note

PLL Registers

1B PLL Setting Register for Memory and Display(R/W) [PLLSETR]

OPLLPd	<0>	Power Down for Display PLL	
		0	PLL normal Operation
		1	PLL Power Down
OPLLVon	<1>	Reset for Display PLL	
		0	PLL normal Operation
		1	Reset the PLL NF & NR Divider
OPLLBp	<2>	Bypass Mode for Display PLL	
		0	PLL normal Operation
		1	Bypass the PLL & FOUT=FIN
OPLLOe	<3>	Output Control for Display PLL	
		0	FOUT= Fck/NO
		1	FOUT=0
MPLLPd	<4>	Power Down for Memory PLL	
		0	PLL normal Operation
		1	PLL Power Down
MPLLVon	<5>	Reset for Memory PLL	
		0	PLL normal Operation
		1	Reset the PLL NF & NR Divider
MPLLBp	<6>	Bypass Mode for Memory PLL	
		0	PLL normal Operation
		1	Bypass the PLL & FOUT=FIN
MPLLOe	<7>	Output control for memory PLL	
		0	FOUT= Fck/NO
		1	FOUT=0

Note: FOUT = FIN * NF/(NR*NO) = FVCO/NO, here FVCO is between 80MHz and 190Mhz

Here, FIN is input clock (example:14.31818MHz XTAL)

NF/NR, and NO are refer to BAS#1C~1F definition

1C LSB of NF Value for Memory PLL(R/W) [MPLLNF]

MPLLNF	<7:0>	MPLLNF<7:0> Value for memory PLL

Note: NF is MPLLNF+2

1D MSB of NF/NR/NO Value for Memory PLL(R/W) [MPLLNRO]

MPLLNR	<4:0>	MPLLNR<4:0> value for memory PLL
MPLLNO	<6:5>	MPLLNO<1:0> value for memory PLL
MPLLNF	<7>	MPLLNF<8> Value for memory PLL

Note: NR is MPLLNR+2, NO is MPLLNO+1

1E LSB of NF Value for Display PLL(R/W) [OPLLNF]

OPLLNF	<7:0>	OPLLNF<7:0> Value for display PLL

Note: NF is OPLLNF+2

1F MSB of NF/NR/NO Value for Display PLL(R/W) [OPLLNRO]

OPLLNR	<4:0>	OPLLNR<4:0> value for display PLL
OPLLNO	<6:5>	OPLLNO<1:0> value for display PLL
OPLLNF	<7>	OPLLNF<8> Value for display PLL

Note: NR is OPLLNR+2, NO is OPLLNO+1

➢ Capture Control Group Registers (Accessible when BAS#0E = 01h)

I. PS timing

INDEX (HEX)	Register Description Register Name	BITS	Function Description
20	PS Horizontal Capture Start LSB (R/W) [CAPPSHSTART]		
	CapPSHStartL	<7:0>	Bits<7:0> of PS horizontal capture start position (Unit: 1 pixel)
21	PS Horizontal Capture Start MSB (R/W) [CAPPSHSTART]		
	CapPSHStartH	<3:0>	Bits<11:8> of PS horizontal capture start position
	Reserved	<7:4>	Reserved
22	PS Horizontal Capture Source Size LSB (R/W) [CAPPSHSRCSIZE]		
	CapPSHSrcSizeL	<7:0>	Bits<7:0> of PS horizontal capture source size (Unit: 1 pixel)
23	PS Horizontal Capture Source Size MSB (R/W) [CAPPSHSRCSIZE]		
	CapPSHSrcSizeH	<3:0>	Bits<11:8> of PS horizontal capture source size
	Reserved	<7:4>	Reserved
24	PS Horizontal Capture Destination Size LSB (R/W) [CAPPSHDESTSIZE]		
	CapPSHDestSizeL	<7:0>	Bits<7:0> of PS horizontal capture destination size (Unit: 1 pixel)
25	PS Horizontal Capture Destination Size MSB (R/W) [CAPPSHDESTSIZE]		
	CapPSHDestSizeH	<3:0>	Bits<11:8> of PS horizontal capture destination size
	Reserved	<7:4>	Reserved

Note: CAPPSHSRCSIZE >= CAPPSHDESTSIZE

26	PS Vertical Capture Start (R/W) [CAPPSVSTART]		

	CapPSVStartL	<7:0>	Bits<7:0> of PS vertical capture start position (Unit: 1 line)

27 PS Vertical Capture Start (R/W) [CAPPSVSTART]

CapPSVStartH	<2:0>	Bits<10:8> of PS vertical capture start position
Reserved	<7:4>	Reserved

28 PS Vertical Capture Source Size LSB (R/W) [CAPPSVSRCSIZE]

CapPSVSrcSizeL	<7:0>	Bits<7:0> of PS vertical capture source size (Unit: 1 line)

29 PS Vertical Capture Source Size MSB (R/W) [CAPPSVSRCSIZE]

CapPSVSrcSizeH	<2:0>	Bits<10:8> of PS vertical capture source size
Reserved	<7:4>	Reserved

2A PS Vertical Capture Destination Size LSB (R/W) [CAPPSVDESTSIZE]

CapVDestSizeL	<7:0>	Bits<7:0> of PS vertical capture destination size (Unit: 1 line).

2B PS Vertical Capture Destination Size MSB (R/W) [CAPPSVDESTSIZE]

CapPSVDestSizeH	<2:0>	Bits<10:8> of PS vertical capture destination size
Reserved	<7:4>	Reserved

2E PS Interlace Control (R/W) [PSINTERLACECTR]

PSInterlaceEn	<0>	Enable PS interlace timing input	
PSFieldCap	<2:1>	PS field capture into memory	
		00	Capture even and odd field into memory
		01	Capture odd field only
		10	Capture even field only
		11	Reserved
PSFieldoffset	<7:4>	PS field capture offset	

30 PS Horizontal Scale Down Ratio LSB (R/W) [PSHDNRATIO]

PSHDnRatioL	<7:0>	Bits<7:0> of PS horizontal scale down ratio

31	PS Horizontal Scale Down Ratio MSB (R/W) [PSHDNRATIO]		
	PSHDnRatioH	<0>	Bit<8> of PS horizontal scale down ratio
	Reserved	<7:1>	Reserved

Note: PSHDNRATIO = CAPPSHDESTSIZE / CAPPSHSRCSIZE * 256

32	PS Vertical Scale Down Ratio LSB (R/W) [PSVDNRATIO]		
	PSVDnRatioL	<7:0>	Bits<7:0> of PS vertical scale down ratio

33	PS Vertical Scale Down Ratio MSB (R/W) [PSVDNRATIO]		
	PSVDnRatioH	<0>	Bit<8> of PS vertical scale down ratio
	Reserved	<7:1>	Reserved

Note: PSVDNRATIO = CAPPSVDESTSIZE / CAPPSVSRCSIZE * 256

II. VBI Input timing:

VBI captured data is always been stored in DRAM address, starting at 0.

To Disable VBI capture, set VBIVStart > VBIVEnd, and VBIHStart > VBIHEnd

34	VBI Vertical Start (R/W) [VBIVSTART]		
	VBIVStart	<7:0>	VBI vertical capture start position

35	VBI Vertical End (R/W) [VBIVEND]		
	VBIVend	<7:0>	VBI vertical capture end

36	VBI Horizontal Start (R/W) [VBIHSTART]		
	VBIHStart	<7:0>	VBI horizontal capture start position

37	VBI Horizontal Size (R/W) [VBIVSIZE]		
	VBIHSize	<7:0>	VBI horizontal capture size

III. ITU-656 Detection:

38 PS ITU-656 Hsync Start (R/W) [PS656HSTART]

PS656HStart	<7:0>	Primary stream ITU656data horizontal sync start position default value 20h

39 PS ITU-656 Hsync End (R/W) [PS656HEND]

PS656HEnd	<7:0>	ITU656data horizontal sync end position default value a0h

3A PS ITU-656 Vsync Start (R/W) [PS656VSTART]

PS656VStart	<7:0>	ITU656data vertical sync start position default value 02h

3B PS ITU-656 Vsync End (R/W) [PS656VEND]

PS656VEnd	<7:0>	ITU656data vertical sync end position default value 04h

3C SS ITU-656 Hsync Start (R/W) [SS656HSTART]

SS656HStart	<7:0>	ITU656data horizontal sync start position default value 20h

3D SS ITU-656 Hsync End (R/W) [SS656HEND]

SS656HEnd	<7:0>	ITU656data horizontal sync end position default value a0h

3E SS ITU-656 Vsync Start (R/W) [SS656VSTART]

SS656VStart	<7:0>	ITU656data vertical sync start position default value 02h

3F SS ITU-656 Vsync End (R/W) [SS656VEND]

SS656VEnd	<7:0>	ITU656data vertical sync end position default value 04h

IV. SS Input timing:

40	SS Horizontal Capture Start LSB (R/W) [CAPSSHSTART]		
	CapSSHStartL	<7:0>	Bits<7:0> of SS horizontal capture start position (Unit: 1 pixel)

41	SS Horizontal Capture Start MSB (R/W) [CAPSSHSTART]		
	CapSSHStartH	<3:0>	Bits<11:8> of SS horizontal capture start position
	Reserved	<7:4>	Reserved

42	SS Horizontal Capture Source Size LSB (R/W) [CAPSSHSRCSIZE]		
	CapSSHSrcSizeL	<7:0>	Bits<7:0> of SS horizontal capture source size (Unit: 1 pixel)

43	SS Horizontal Capture Source Size MSB (R/W) [CAPSSHSRCSIZE]		
	CapSSHSrcSizeH	<3:0>	Bits<11:8> of SS horizontal capture source size
	Reserved	<7:4>	Reserved

44	SS Horizontal Capture Destination Size LSB (R/W) [CAPSSHDESTSIZE]		
	CapSSHDestSizeL	<7:0>	Bits<7:0> of SS horizontal capture destination size (Unit: 1 pixel).

45	SS Horizontal Capture Destination Size MSB (R/W) [CAPSSHDESTSIZE]		
	CapSSHDestSizeH	<3:0>	Bits<11:8> of SS horizontal capture destination size
	Reserved	<7:4>	Reserved

Note: CAPSSHSRCSIZE >= CAPSSHDESTSIZE

46	SS Vertical Capture Start LSB (R/W) [CAPSSVSTART]		
	CapSSVStartL	<7:0>	Bits<7:0> of SS vertical capture start position (Unit:1 line)

47	SS Vertical Capture Start MSB (R/W) [CAPSSVSTART]		
	CapSSVStartH	<2:0>	Bits<10:8> of SS vertical capture start position

Reserved	<7:3>	Reserved

48 SS Vertical Capture Source Size LSB (R/W) [CAPSSVSRCSIZE]

CapSSVSrcSizeL	<7:0>	Bits<7:0> of SS vertical capture source size (Unit:1 line)

49 SS Vertical Capture Source Size MSB (R/W) [CAPSSVSRCSIZE]

CapSSVSrcSizeH	<2:0>	Bits<10:8> of SS vertical capture source size
Reserved	<7:3>	Reserved

4A SS Vertical Capture Destination Size LSB (R/W) [CAPSSVDESTSIZE]

CapSSVDestSizeL	<7:0>	Bits<7:0> of SS vertical capture destination size (Unit:1 line).

4B SS Vertical Capture Destination Size MSB (R/W) [CAPSSVDESTSIZE]

CapSSVDestSizeH	<2:0>	Bits<10:8> of SS vertical capture destination size
Reserved	<7:3>	Reserved

Note: CASSVSRCSIZE >= CAPSSVDESTSIZE

4E SS Interlace Control (R/W) [SSINTERLACECTRL]

SSInterlaceEn	<0>	Enable SS interlace timing input	
SSFieldCap	<2:1>	SS field capture	
		00	Reserved
		01	Capture odd field only
		10	Capture even field only
		11	Reserved
SSFieldoffset	<7:4>	SS field capture offset	

4F SS Scale Down Horizontal Filter Taps (R/W) [SSDOWNHFILTER]

SSHFltTaps	<2:0>	Secondary stream horizontal scale down filter taps	
		000	no filter
		001	2-tap filter
		010	4-tap filter
		011	8-tap filter

Reserved	<7:3>	Reserved

IV: Position Detection:

51 Data Threshold for Position Detection (R/W) [POSDATATH]

PosDataTh	<7:0>	Luma(brightness) threshold value

Note: CAP#51 is used to determine PS/SS non-blanking pixel for both horizontal and vertical direction. Any pixel luma value less than this value will be considered as blanking.

5A Horizontal Active Start LSB (R) [POSHDESTART]

PosHDEStartL	<7:0>	Bits<7:0> of detected horizontal active start position (Unit: 1 pixel)

5B Horizontal Active Start MSB (R) [POSHDESTART]

PosHDEStartH	<2:0>	Bits<10:8> of detected horizontal active start position
Reserved	<7:3>	Reserved

5C Horizontal Active End LSB (R) [POSHDEEND]

PosHDEEndL	<7:0>	Bits<7:0> of detected horizontal active start position (Unit: 1 pixel)

5D Horizontal Active End MSB (R) [POSHDEEND]

PosHDEEndH	<2:0>	Bits<10:8> of detected horizontal active end position
Reserved	<7:3>	Reserved

5E Vertical Active Start LSB (R) [POSVDESTART]

PosVDEStartL	<7:0>	Bits<7:0> of detected vertical active start line (Unit: 1 line)

5F Vertical Active Start MSB (R) [POSVDESTART]

PosVDEStartH	<2:0>	Bits<10:8> of detected vertical active start line
Reserved	<7:3>	Reserved

60 Vertical Active End LSB (R) [POSVDEEND]

PosVDEEndL	<7:0>	Bits <7:0> of detected vertical active end line (Unit: 1 line)

61 Vertical Active End MSB (R) [POSVDEEND]

PosVDEEndH	<2:0>	Bits<10:8> of detected vertical active end line
Reserved	<7:3>	Reserved

V: Mode Detection:

62 PS Horizontal Capture Total Counter LSB (R) [CAPPSHTOTALCNT]

CapPSHtotalCntL	<7:0>	Bits<7:0> of PS horizontal total count value

63 PS Horizontal Capture Total Counter MSB (R) [CAPPSHTOTALCNT]

CapPSHtotalCntH	<2:0>	Bits<10:8> of PS horizontal total count value
Reserved	<7:3>	Reserved

64 PS Vertical Capture Total Counter LSB (R) [CAPPSVTOTALCNT]

CapPSVtotalCntL	<7:0>	Bits<7:0> of PS vertical total count value

65 PS Vertical Capture Total Counter MSB (R) [CAPPSVTOTALCNT]

CapPSVtotalCntH	<2:0>	Bits<10:8> of PS vertical total count value
Reserved	<7:3>	Reserved

66 SS Horizontal Capture Total Counter LSB (R) [CAPSSHTOTALCNT]

CapSSHtotalCntL	<7:0>	Bits<7:0> of SS horizontal total count value

67 SS Horizontal Capture Total Counter MSB (R) [CAPSSHTOTALCNT]

CapSSHtotalCntH	<2:0>	Bits<10:8> of SS horizontal total count value
Reserved	<7:3>	Reserved

68 SS Vertical Capture Total Counter LSB (R) [CAPSSVTOTALCNT]

CapSSVtotalCntL	<7:0>	Bits<7:0> of SS vertical total count value

69 SS Vertical Capture Total Counter MSB (R) [CAPSSVTOTALCNT]

CapSSVtotalCntH	<2:0>	Bits<10:8> of SS vertical total count value
Reserved	<7:3>	Reserved

70 PS Double Buffer Flag LSB (R/W) [PSDBUFFLAGNUM]

PSDbufFlagNumL	<7:0>	Bits<7:0> of PS double buffer flag number

71 SS Double Buffer Flag LSB (R/W) [SSDBUFFLAGNUM]

SSDbufFlagNumL	<7:0>	Bits<7:0> of SS double buffer flag number

72 PS & SS Double Buffer Flag MSB (R/W) [DBUFFLAGNUM]

PSDbufFlagNumH	<2:0>	Bits<10:8> of PS double buffer flag number
SSDbufFlagNumH	<6:4>	Bits<10:8> of SS double buffer flag number
Reserved	<7><3>	Reserved

73 Tune Input PC Clock Phase (R/W) [TUNEPCCLK]

TunePCclk	<2:0>	Phase delay number(8 steps)	
	<4:3>	Phase delay types	
		00	PCclk
		01	PCclk + delay phase
		10	Inversed PCclk
		11	Inversed PCclk + delay phase
Reserved	<7:5>	Reserved	

74 Tune Input V1 Clock Phase (R/W) [TUNEV1CLK]

TuneV1clk	<2:0>	Phase delay number(8 steps)	
	<4:3>	Phase delay types	
		00	V1clk
		01	V1clk + delay phase
		10	Inversed V1clk
		11	Inversed V1clk + delay phase
Reserved	<7:5>	Reserved	

75 Tune Input V2 Clock Phase (R/W) [TUNEV2CLK]

TuneV2clk	<2:0>	Phase delay number(8 steps)	
	<4:3>	Phase delay types	
		00	V2clk
		01	V2clk + delay phase
		10	Inversed V2clk
		11	Inversed V2clk + delay phase
Reserved	<7:5>	Reserved	

➢ Memory Control Group Registers (Accessible when BAS#0E = 02h)

I.DRAM control

INDEX (HEX)	Register Name	BITS	Function Description
20	DRAM Access control (R/W) [DRAMACCESSCTRL]		
	PSInputEnable	<0>	Enable PS input
	SSInputEnable	<1>	Enable SS input
	PowerUp	<2>	Enable power up
	PSOutputEnable	<3>	Enable PS output
	SSOutputEnable	<4>	Enable SS output
	RefreshEnable	<5>	Enable DRAM refresh
	PowerDown	<6>	Enable power down
	SetMode	<7>	Enable DRAM setmode cycle
21	DRAM Write (R/W) [DRAMWRITE]		
	PMCLKSel	<0>	Select DRAM read clock signal path
			0 Internal loop
			1 External loop from pad MCLK to PMCLK
	WriteMask1	<1>	Write mask of DRAM byte 0, 1
	WriteMask2	<2>	Write mask of DRAM byte 2
	SoftRest	<3>	Software Reset
	DataDelay	<5:4>	DRAM data delay
	DataRdyDelay	<7:6>	DRAM data ready delay
22	Output FIFO & SS Input FIFO Control (R/W) [FIFOCONTROL]		
	OutputLevel	<3:0>	Stream output(PS and SS) FIFO level control
	SSInputLevel	<7:4>	SS input FIFO level control
23	PS Input FIFO Control (R/W) [FIFOCONTROL]		
	PSInputLevel	<3:0>	PS input FIFO level control
	Reserved	<7:4>	Reserved

Note: These are DRAM FIFO water mark, when FIFO reach this urgent level, the corresponding video source needs to be serviced(R/W or to/from DRAM)

24~27: Reserved

28 DRAM Minimum Refresh (R/W) [DRAMMINREFRESH]

MinRefresh	<7:0>	Minimum refresh requirement within the period of a output VSYNC, usually 1/60 sec

29 DRAM Control 0 (R/W) [DRAMCTRL]

TRAS	<1:0>	DRAM RAS control signal	
		00	5 memory clocks
		01	6 memory clocks
		01	7 memory clocks
		11	8 memory clocks
TRC	<4:2>	DRAM RC control signal	
		000	7 memory clocks
		001	8 memory clocks
		001	9 memory clocks
		011	10 memory clocks
		100	11 memory clocks
		101	12 memory clocks
		101	13 memory clocks
		111	14 memory clocks
TRCD	<5>	DRAM RCD control signals	
		0	No delay
		1	Delay 1 memory clock
TRP	<6>	DRAM RP control signal	
		0	No delay
		1	Delay 1 memory clock
TRPD	<7>	DRAM RPD control signal	
		0	No delay
		1	Delay 1 memory clock

2A DRAM Control 1 (R/W) [DRAMCTRL]

TWR	<0>	DRAM WR control signal	
		0	No delay
		1	Delay 1 memory clock
TCL	<1>	DRAM CL control signal	
		0	No delay
		1	Delay 1 memory clock
TRW	<2>	DRAM RW control signal	
		0	No delay
		1	Delay 1 memory clock
MemConfig	<4:3>	SDRAM Size	
		00	16Mb
		01	64Mb
		10	Reserved
		11	Reserved
BankConfig	<5>	Bank selector	
		0	A22, 0-4M = bank 0, 4-8M = bank 1
		1	A21, 4-6M = bank 0, 6-8M = bank 1
Reserved	<6>	Tie to 1	
TXSR	<7>	DRAM XSR control signal	

Note: MEM#29&2A is SDRAM timing parameters. Default value: MEM#29=ef, MEM#2A=4f

2B DRAM Read Address 0 (R/W) [DRAMRADDR]

MemReadAddr0	<7:0>	Bits<7:0> of DRAM read address. (unit: 2 pixels)

2C DRAM Read Address 1 (R/W) [DRAMRADDR]

MemReadAddr1	<7:0>	Bits<15:8> of DRAM read address

2D DRAM Read Address 2 (R/W) [DRAMRADDR]

MemReadAddr2	<4:0>	Bits<20:16> of DRAM read address
Reserved	<7:5>	Reserved

30 XY Mirror Input (R/W) [XYMIRRORIN]

PSInputFlipX	<0>	Enable PS X mirror capture(horizontally captured in the reversed direction)
PSInputFlipY	<1>	Enable PS Y mirror capture(vertically captured in the reversed direction, i.e. up side down capture)
SSInputFlipX	<2>	Enable SS X mirror capture(horizontally captured in the reversed direction)
SSInputFlipY	<3>	Enable SS Y mirror capture(vertically captured in the reversed direction, i.e. up side down capture)
GSInputFlipX	<4>	Enable GS X mirror write(horizontally written in the reversed direction)
GSInputFlipY	<5>	Enable GS Y mirror capture(vertically written in the reversed direction, i.e. up side down written)
WCInputFlipX	<6>	Enable Window Copy X mirror copy-in (horizontally copy-in in the reversed direction)
WCInputFlipY	<7>	Enable Window Copy Y mirror copy-in(vertically copy-in in the reversed direction, i.e. up side down copy-in)

31 XY Mirror Output (R/W) [XYMIRROROUT]

PSOutputFlipX	<0>	Enable PS X mirror display(horizontally display in the reversed direction)
PSOutputFlipY	<1>	Enable PS Y mirror display (vertically displayed in the reversed direction, i.e. up side down display)
SSOutputFlipX	<2>	Enable SS X mirror display (horizontally displayed in the reversed direction)
SSOutputFlipY	<3>	Enable SS Y mirror display (vertically displayed in the reversed direction, i.e. up side down display)
WCOutputFlipX	<4>	Enable Window Copy X mirror copy-out (horizontally copy- out in the reversed direction)
WCOutputFlipY	<5>	Enable Window Copy Y mirror copy- out (vertically copy-out in the reversed direction, i.e. up side down copy- out)
Reserved	<7:6>	Reserved

32 Skip Mode (R/W) [SKIPMODE]

PSInputSkip	<1:0>	PS DRAM input address pointer incremental unit
		00 2 fields/1 frame stockpile
		even1, odd1, even1, odd1 ….,
		Note: Stride >= size
		01 Reserved
		10 4 fields/2frames stockpile
		F1(1),F2(1),F3(1),F4(1),F1(2),F2(2),F3(2)…
		Note: Stride >= size * 4
		11 Reserved
Reserved	<2>	Reserved
PSITwoField	<3>	PSI two field mode
SSITwoField	<4>	SSI two field mode
MemControlEn	<5>	0 Disable sdram controller
		1 Enable sdram controller
PSDbufferEn	<6>	PS dobule buffering enable
SSDbufferEn	<7>	SS dobule buffering enable

II. DRAM input window control

33 PS DRAM Input Start (R/W) [DRAMPSISTART]

DRAMPSIStart	<7:0>	PS input DRAM address start (Unit: 8192 pixels)

34 PS DRAM Input Horizontal Stride (R/W) [DRAMPSIHSTRIDE]

DRAMPSIHStride	<7:0>	PS input DRAM horizontal stride (Unit: 4/8/12 pixels)

Note: Set stride value at 64/128/256 boundary, will better ease DRAM timing.

35 PS DRAM Input Horizontal Size (R/W) [DRAMPSIHSIZE]

DRAMPSIHSize	<7:0>	PS input DRAM horizontal size (Unit: 4/8/12 pixels)

Note: PS DRAM Input Horizontal Size should same as PS Horizontal Destination Size

DRAMPSIHSIZE = CAPPSHDESTSIZE(CAP#25&24) / K, K= 4 or 8 or 12

36 SS DRAM Input Start (R/W) [DRAMSSISTART]

DRAMSSIStart	<7:0>	SS input DRAM address start (Unit: 8192 pixels)

37 SS DRAM Input Horizontal Stride (R/W) [DRAMSSIHSTRIDE]

DRAMSSIHStride	<7:0>	SS input DRAM horizontal stride (Unit: 4/8/12 pixels)

38 SS DRAM Input Horizontal Size (R/W) [DRAMSSIHSIZE]

DRAMSSIHSize	<7:0>	SS input DRAM horizontal size (Unit: 4/8/16 pixels)

Note: SS DRAM Input Horizontal Size should same as SS Horizontal Destination Size

DRAMSSIHSIZE = CAPSSHDESTSIZE(CAP#45&44) / K, K= 4 or 8 or 12

III. DRAM window copy control

39 Window Copy Source Start LSB (R/W) [WCSRCSTART]

GSInputStart1	<7:0>	Bits<7:0> of GS input DRAM address start. (Unit: 8192 pixels)

3A Window Copy Source Start (R/W) [WCSRCSTART]

GSInputStart2	<7:0>	Bits<15:8> of GS input DRAM address start

3B Window Copy Source Start MSB (R/W) [WCSRCSTART]

GSInputStart3	<3:0>	Bits<18:16> of GS input DRAM address start
Reserved	<7:4>	Reserved

3C Window Copy Source Stride (R/W) [GSDRAMINPUTSTRIDE]

GSIStride	<7:0>	GS input DRAM stride. (8 pixels)

3D Window Copy Size (R/W) [GSDRAMINPUTSIZE]

GSHSize	<7:0>	GS input DRAM size. (Unit: 8 pixels)

3E Direct Write Stride (R/W) [WCSTRIDE]

WCStride	<7:0>	DRAM window copy stride. (Unit: 8 pixels)

3F Window Copy Destination Start LSB (R/W) [WCDESTSTART]

WCSrcStart1	<7:0>	Bits<7:0> of DRAM window copy source address start. (Unit: 8 pixels)

40 Window Copy Destination Start (R/W) [WCDESTSTART]

WCDestStart2	<7:0>	Bits<15:8> of DRAM window copy source address start

41 Window Copy Destination Start MSB (R/W) [WCDESTSTART]

WCDestStart3	<3:0>	Bits<20:16> of DRAM window copy source address start
Reserved	<7:4>	Reserved

Note: After writing to MEM#41, the Window Copy operation will be carried out.

42 Direct Read/Write Address LSB (R/W) [DASTART]

DAddrStart1	<7:0>	Bits<7:0> of DRAM window copy source address start. (Unit: 8 pixels)

43 Direct Read/Write Address (R/W) [DASTART]

DAddrStart2	<7:0>	Bits<15:8> of DRAM window copy source address start

44 Direct Read/Write Address MSB (R/W) [DASTART]

DAddrStart3	<3:0>	Bits<20:16> of DRAM window copy source address start
Reserved	<7:4>	Reserved

45 Window Copy Size (R/W) [WCSIZE]

WCSize	<7:0>	DRAM Directly Write size. (Unit: 8 pixels) or DRAM window copy total lines [7:0] for Window Copy.

46 Window Copy Line Total (R/W) [WCLINETOTAL]

WCLineTotal	<7:0>	DRAM window copy total lines[2:0]. (1 line)

IV. DRAM output window control

47 PS DRAM Output Start (R/W) [DRAMPSOSTART]

DRAMPSOStart	<7:0>	PS output DRAM address start. (Unit: 8192 pixels)

48 PS DRAM Output Horizontal Stride (R/W) [DRAMPSOHSTRIDE]

DRAMPSOHStride	<7:0>	PS output DRAM horizontal stride. (Unit: 4/8/12 pixels)

49 PS DRAM Output Horizontal Size (R/W) [DRAMPSOHSIZE]

DRAMPSOHSize	<7:0>	PS output DRAM horizontal size. (Unit: 4/8/12 pixels)

Note: PS DRAM Output Horizontal Size should same as PS Horizontal Display Source Size
DRAMPSOHSIZE = DISPSHSRCSIZE(DIS#41&40) / K, K= 4 or 8 or 12

4A SS DRAM Output Start (R/W) [DRAMSSOSTART]

DRAMSSOStart	<7:0>	SS output DRAM address start. (Unit: 8192 pixels)

4B SS DRAM Output Horizontal Stride (R/W) [DRAMSSOHSTRIDE]

DRAMSSOHStride	<7:0>	SS output DRAM horizontal stride. (4/8/12 pixels)

4C SS DRAM Output Horizontal Size (R/W) [DRAMSSOHSIZE]

DRAMSSOHSize	<7:0>	SS output DRAM horizontal size. (4/8/12 pixels)

Note: SS DRAM Output Horizontal Size should same as SS Horizontal Display Size
DRAMSSOHSIZE = [DISSSHDEEND(DIS#3B&3A) - DISSSHDESTART(DIS#39&38)] / K,
K= 4 or 8 or 12

4D VBI Start Address LSB (R/W) [VBISTART]

VBIAddrStart1	<7:0>	Bit<7:0> of VBI starting address.

4E VBI Start Address (R/W) [VBISTART]

VBIAddrStart2	<7:0>	Bit<15:8> of VBI starting address.

4F VBI Start Address MSB (R/W) [VBISTART]

VBIAddrStart3	<3:0>	Bit<19:16> of VBI starting address.
Reserved	<7:4>	Reserved

50 Front Motion Detect Control (R/W) [FRONTM]

FrontMYth	<6:0>	Y threshold Value for Front Motion
EnFrontM	<7>	Enable Front Motion Detection

51 Tune Memory Write Clock Phase (R/W) [TUNEMCLK]

TuneMclk	<2:0>	Phase delay number(8 steps)	
	<4:3>	Phase delay types	
		00	Mclk
		01	Mclk + delay phase
		10	Inversed Mclk
		11	Inversed Mclk + delay phase
Reserved	<7:5>	Reserved	

52 Tune Memory Read Clock Phase (R/W) [TUNEPMCLK]

TunePMclk	<2:0>	Phase delay number(8 steps)	
	<4:3>	Phase delay types	
		00	PMclk
		01	PMclk + delay phase
		10	Inversed PMclk
		11	Inversed PMclk + delay phase
Reserved	<7:5>	Reserved	

V. DRAM data port

60 Read Status (R) [READSTATUS]

Status	<0>	Data Ready
Reserved	<7:1>	Reserved

61 Byte 0 (R)(W) [BYTE0]

RByte0(R)	<7:0>	Bits<7:0> of DRAM for read-out
WByte0(W)	<7:0>	Bits<7:0> of Pixel 0 for 16-bit mode Write, or Dummy field for 24-bit mode Write

62	Byte 1 (R)(W) [BYTE1]		
	RByte1(R)	<7:0>	Bits<15:8> of DRAM read-out
	WByte1(W)	<7:0>	Bits<15:8> of Pixel 0 for 16-bit mode Write, or Blue field for 24-bit mode Write
63	Byte 2 (R)(W) [BYTE2]		
	RByte2(R)	<7:0>	Bits<23:16> of DRAM read-out
	WByte2(W)	<7:0>	Bits<7:0> of Pixel 1 for 16-bit mode Write, or Green field for 24-bit mode Write
64	Byte 3 (R)(W) [BYTE3]		
	RByte3(R)	<7:0>	Bits<31:24> of DRAM read-out
	WByte3(W)	<7:0>	<15:8> of Pixel 1 for 16-bit mode Write, or Red field for 24-bit mode Write
65	Byte 4 (R) [BYTE4]		
	RByte4	<7:0>	Bits<39:32> of DRAM read-out
66	Byte5 (R) [BYTE5]		
	RByte4	<7:0>	Bits<47:40> of DRAM read-out

DRAM data read ports are defined in MEM#61~66. MemReadAddr is defined in MEM#42~44. After reading MEM#60, the read cycle will be strobe if bit-0 is 0. MEM#60 should be read until bit 0 is 1. Then, read MEM#61~66 for the data read from SDRAM.

➢ Display Control Group Registers (Accessible when BAS#0E = 03h)

I. Display Timing

INDEX	Register Description		
(HEX)	Register Name	BITS	Function Description
20	Display Horizontal Total LSB (R/W) [DISHTOTAL]		
	DisHTotalL	<7:0>	Bits<7:0> of display horizontal total (Unit: 1 pixel)
21	Display Horizontal Total MSB (R/W) [DISHTOTAL]		
	DisHTotalH	<3:0>	Bits<11:8> of display horizontal total
	Reserved	<7:4>	Reserved
22	Display Horizontal Sync LSB (R/W) [DISHSEND]		
	DisHSEndL	<7:0>	Bits<7:0> of display horizontal sync end (Unit: 1 pixel)
23	Display Horizontal Sync MSB (R/W) [DISHSEND]		
	DisHSEndH	<3:0>	Bits<11:8> of display horizontal sync end
	Reserved	<7:4>	Reserved

Note: Horizontal sync start at position 1.

24	Horizontal Display Start LSB (R/W) [DISHDESTART]		
	DisHDEStartL	<7:0>	Bits<7:0> of horizontal display start (Unit: 1 pixel)
25	Horizontal Display Start MSB (R/W) [DISHDESTART]		
	DisHDEStartH	<3:0>	Bits<11:8> of horizontal display start
	Reserved	<7:4>	Reserved
26	Horizontal Display End LSB (R/W) [DISHDEEND]		
	DisHDEEndL	<7:0>	Bits<7:0> of horizontal display end (Unit: 1 pixel)
27	Horizontal Display End MSB (R/W) [DISHDEEND]		

DisHDEEndH	<3:0>	Bits<11:8> of horizontal display end
Reserved	<7:4>	Reserved

28 Display Vertical Total LSB (R/W) [DISVTOTAL]

DisVTotalL	<7:0>	Bits<7:0> of display vertical total (Unit: 1 pixel)

29 Display Vertical Total MSB (R/W) [DISVTOTAL]

DisVTotalH	<3:0>	Bits <11:8> of display vertical total
Reserved	<7:4>	Reserved

2A Display Vertical Sync LSB (R/W) [DISVSEND]

DisVSEndL	<7:0>	Bits<7:0> of display vertical sync end (Unit: 1 pixel)

2B Display Vertical Sync MSB (R/W) [DISVSEND]

DisVSEndH	<3:0>	Bits<11:8> of display vertical sync end
Reserved	<7:4>	Reserved

Note: Vertical sync start at line 1.

2C Vertical Display Start LSB (R/W) [DISVDESTART]

DisVDEStartL	<7:0>	Bits<7:0> of vertical display start (Unit: 1 pixel)

2D Vertical Display Start MSB (R/W) [DISVDESTART]

DisVDEStartH	<3:0>	Bits<11:8> of vertical display start
Reserved	<7:4>	Reserved

2E Vertical Display End LSB (R/W) [DISVDEEND]

DisVDEEndL	<7:0>	Bits<7:0> of vertical display end(Unit: 1 pixel)

2F Vertical Display End MSB (R/W) [DISVDEEND]

DisVDEEndH	<3:0>	Bits<11:8> of vertical display end
Reserved	<7:4>	Reserved

II. Window Output Timing

30 PS Horizontal Display Start LSB (R/W) [DISPSHDESTART]

DisPSHDEStartL	<7:0>	Bits<7:0> of PS horizontal display start (Unit: 1 pixel)

31 PS Horizontal Display Start MSB (R/W) [DISPSHDESTART]

DisPSHDEStartH	<3:0>	Bits<11:8> of PS horizontal display start
Reserved	<7:4>	Reserved

32 PS Horizontal Display End LSB (R/W) [DISPSHDEEND]

DisPSHDEEndL	<7:0>	Bits<7:0> of PS horizontal display end(Unit: 1 pixel)

33 PS Horizontal Display End MSB (R/W) [DISPSHDEEND]

DisPSHDEEndH	<3:0>	Bits<11:8> of PS horizontal display end
Reserved	<7:4>	Reserved

34 PS Vertical Display Start LSB (R/W) [DISPSVDESTART]

DisPSVDEStartL	<7:0>	Bits<7:0> of PS vertical display start (Unit: 1 pixel)

35 PS Vertical Display Start MSB (R/W) [DISPSVDESTART]

DisPSVDEStartH	<3:0>	Bits<11:8> of PS vertical display start
Reserved	<7:4>	Reserved

36 PS Vertical Display End LSB (R/W) [DISPSVDEEND]

DisPSVDEEndL	<7:0>	Bits<7:0> of PS vertical display end(Unit: 1 pixel)

37 PS Vertical Display End MSB (R/W) [DISPSVDEEND]

DisPSVDEEndH	<3:0>	Bits<11:8> of PS vertical display end
Reserved	<7:4>	Reserved

38 SS Horizontal Display Start LSB (R/W) [DISSSHDESTART]

DisSSHDEStartL	<7:0>	Bits<7:0> of SS horizontal display start (Unit: 1 pixel)

39 SS Horizontal Display Start MSB (R/W) [DISSSHDESTART]

DisSSHDEStartH	<3:0>	Bits<11:8> of SS horizontal display start
Reserved	<7:4>	Reserved

3A SS Horizontal Display End LSB (R/W) [DISSSHDEEND]

DisSSHDEEndL	<7:0>	Bits<7:0> of SS horizontal display end (Unit: 1 pixel)

3B SS Horizontal Display End MSB (R/W) [DISSSHDEEND]

DisSSHDEEndH	<3:0>	Bits<11:8> of SS horizontal display end
Reserved	<7:4>	Reserved

3C SS Vertical Display Start LSB (R/W) [DISSSVDESTART]

DisSSVDEStartL	<7:0>	Bits<7:0> of SS vertical display start (Unit: 1 pixel)

3D SS Vertical Display Start MSB (R/W) [DISSSVDESTART]

DisSSVDEStartH	<3:0>	Bits<11:8> of SS vertical display start
Reserved	<7:4>	Reserved

3E SS Vertical Display End LSB (R/W) [DISSSVDEEND]

DisSSVDEEndL	<7:0>	Bits<7:0> of SS vertical display end (Unit: 1 pixel)

3F SS Vertical Display End MSB (R/W) [DISSSVDEEND]

DisSSVDEEndH	<3:0>	Bits<11:8> of SS display vertical display end
Reserved	<7:4>	Reserved

III. Zoom In Control Registers

40 PS Horizontal Display Source Size LSB (R/W) [DISPSHSRCSIZE]

DisPSHSrcSizeL	<7:0>	Bits<7:0> of PS horizontal display source size (Unit: 1 pixel)

41 PS Horizontal Display Source Size MSB (R/W) [DISPSHSRCSIZE]

DisPSHSrcSizeH	<3:0>	Bits<11:8> of PS horizontal display source size
Reserved	<7:4>	Reserved

42 PS Horizontal Display Destination Size LSB (R/W) [DISPSHDESTSIZE]

DisPSHDestSizeL	<7:0>	Bits<7:0> of PS horizontal display destination size (Unit: 1 pixel).

43 PS Horizontal Display Destination Size MSB (R/W) [DISPSHDESTSIZE]

DisPSHDestSizeH	<3:0>	Bits<11:8> of PS horizontal display destination size
Reserved	<7:4>	Reserved

Note: DISPSHDESTSIZE >= DISPSHSRCSIZE

44 PS Vertical Display Source Size LSB (R/W) [DISPSVSRCSIZE]

DisPSVSrcSizeL	<7:0>	Bits<7:0> of PS vertical display source size (Unit:1 pixel)

45 PS Vertical Display Source Size MSB (R/W) [DISPSVSRCSIZE]

DisPSVSrcSizeH	<3:0>	Bits<11:8> of PS vertical display source size
Reserved	<7:4>	Reserved

46 PS Vertical Display Destination Size LSB (R/W) [DISPSVDESTSIZE]

DisPSVDestSizeL	<7:0>	Bits<7:0> of PS vertical display source size (Unit:1 pixel)

47 PS Vertical Display Destination Size MSB (R/W) [DISPSVDESTSIZE]

DisPSVDestSizeH	<3:0>	Bits<11:8> of PS vertical display destination size
Reserved	<7:4>	Reserved

Note: DISPSVDESTSIZE >= DISPSVSRCSIZE

48 PS Zoom In Filter Control (R/W) [PSZOOMFCTRL]

PSVZoomEn	<0>	Enable PS vertical scale-up filtering
PSHZoomEn	<1>	Enable PS horizontal scale-up filtering
Reserved	<7:2>	Reserved

4A PS Horizontal Scale Up Ratio LSB (R/W) [PSHUPRATIO]

PSHUpRatioL	<7:0>	Bits<7:0> of PS horizontal scale up ratio

4B PS Horizontal Scale Up Ratio MSB (R/W) [PSHUPRATIO]

PSHUpRatioH	<7:0>	Bits<15:8> of PS horizontal scale up ratio

Note: PSHUPRATIO = DISPSHSRCSIZE / DISPSHDESTSIZE * 8192

4A Delta PS Horizontal Scale Up Ratio LSB (R/W) [PSDELTAHUPRATIO]

PSDeltaHUpRatioL	<7:0>	Bits<7:0> delta of PS horizontal scale up ratio for Keystone

4B Delta PS Horizontal Scale Up Ratio MSB (R/W) [PSDELTAHUPRATIO]

PSDeltaHUpRatioH	<3:0>	Bits<11:8> delta of PS horizontal scale up ratio for Keystone
PSHDEStartInc	<5:4>	Delta of starting point of PS horizontal DE for Keystone
		00 Added by 0
		01 Added by 1
		10 Added by 0
		11 Substrate by 1
PSHDEEndInc	<7:6>	Delta of Ending point of PS horizontal DE for Keystone
		00 Added by 0
		01 Added by 1
		10 Added by 0
		11 Substrate by 1

Note: This definition is valid when DIS#CB<4>='1' and used in Keystone

4C PS Vertical Scale Up Ratio LSB (R/W) [PSVUPRATIO]

PSVUpRatioL	<7:0>	Bits<7:0> of PS vertical scale up ratio

4D PS Vertical Scale Up Ratio MSB (R/W) [PSVUPRATIO]

PSVUpRatioH	<7:0>	Bits<15:8> of PS vertical scale up ratio

Note: PSVUPRATIO = DISPSVSRCSIZE / PSDISVDESTSIZE * 8192

4E PS Horizontal Scale Up Initial Phase LSB (R/W) [PSHPHASE]

PSHUpPhaseL	<7:0>	Bit<7:0> of PS horizontal scale up initial phase

4F PS Horizontal Scale Up Initial Phase MSB (R/W) [PSHPHASE]

PSHUpPhaseH	<7:0>	Bit<15:8> of PS horizontal scale up initial phase

50 PS Vertical Scale Up Initial Phase LSB (R/W) [PSVPHASE]

PSVUpPhaseL	<7:0>	Bit<7:0> of PS vertical scale up initial phase

51 PS Vertical Scale Up Initial Phase MSB (R/W) [PSVPHASE]

PSVUpPhaseH	<7:0>	Bit<15:8> of PS vertical scale up initial phase

54 Output Mode (R/W) [OUTPUTMODE]

OutputMode	<1:0>	Data pixel output mode	
		00	24-bit output
		01	Dual out
		10	Reserved
		11	Zero output
FlipOdd	<2>	Dual RGB output data flip	
OffsetMode	<3>	Dual RGB output data offset	
Reserved	<4>	Reserved	
DitherMode	<5>	Enable dither output	
		0	No dither
		1	8 bits to 6 bits
Reserved	<6>	Reserved	
LutEn	<7>	Enable built-in LUT look-up table	

55 LUT Write Index (R/W) [LUTWINDEX]

LUTWIndex	<7:0>	LUT access index

5C LUT Red Color LSB (R/W) [LUTRED]

LUTRed	<7:0>	LUT red color port

5D LUT Green Color LSB (R/W) [LUTGREEN]

LUTGreen	<7:0>	LUT green color port	

5E LUT Blue Color LSB (R/W) [LUTBLUE]

LUTBlue	<7:0>	LUT blue color port	

5F LUT Read/Write Trigger (R/W) [LUTWEN]

Reserved	<5:0>	Reserved	
LUTWEn	<7:6>	Write color field enable	
		00	Red, Green and Blue written into LUT
		01	Only Red is written into LUT
		10	Only Green written into LUT
		11	Only Blue written into LUT

56 Pattern Generator and GPO (R/W) [PATTERNGEN]

PatternMode	<1:0>	00	Fram line
		01	Color bar
		10	Gray level
		11	Line moier
PatternEn	<4>	Enable pattern generation	
GPO	<7:5>	General purpose output port	

Note: Set register GPO(DIS#56<7:5>) value will effect pin GPO2~0 output status in phase

IV. OSD Color Registers

58 OSD Write Address LSB (R/W) [OSDRAMWADDR]

OSDRamWAddrL	<7:0>	Bit<7:0> of OSD ram write address

59 OSD Write Address MSB (R/W) [OSDRAMWADDR]

OSDRamWAddrH	<2:0>	Bit<10:8> of OSD ram write address
Reserved	<7:3>	Reserved

5A OSD Write Data Port (W) [OSDRAMWDATA]

	OSDWData	<7:0>	OSD ram write data port

60 Color 0 Red (R/W) [COLOR0RED]

Color0Red	<7:0>	Color 0 Red Component

61 Color 0 Green (R/W) [COLOR0GREEN]

Color0Green	<7:0>	Color 0 Green Component

62 Color 0 Blue (R/W) [COLOR0RED]

Color0Blue	<7:0>	Color 0 Blue Component

63 Color 1 Red (R/W) [COLOR1RED]

Color1Red	<7:0>	Color 1 Red Component

64 Color 1 Green (R/W) [COLOR1GREEN]

Color1Green	<7:0>	Color 1 Green Component

65 Color 1 Blue (R/W) [COLOR1BLUE]

Color1Blue	<7:0>	Color 1 Blue Component

66 Color 2 Red (R/W) [COLOR2RED]

Color2Red	<7:0>	Color 2 Red Component

67 Color 2 Green (R/W) [COLOR2GREEN]

Color2Green	<7:0>	Color 2 Green Component

68 Color 2 Blue (R/W) [COLOR2BLUE]

Color2Blue	<7:0>	Color 2 Blue Component

69 Color 3 Red (R/W) [COLOR3RED]

Color3Red	<7:0>	Color 3 Red Component

6A Color 3 Green (R/W) [COLOR3GREEN]

Color3Green	<7:0>	Color 3 Green Component

6B	Color 3 Blue (R/W) [COLOR3BLUE]		
	Color3Blue	<7:0>	Color 3 Blue Component
6C	Color 4 Red (R/W) [COLOR4RED]		
	Color4Red	<7:0>	Color 4 Red Component
6D	Color 4 Green (R/W) [COLOR0GREEN]		
	Color4Green	<7:0>	Color 4 Green Component
6E	Color 4 Blue (R/W) [COLOR4BLUE]		
	Color4Blue	<7:0>	Color 4 Blue Component
6F	Color 5 Red (R/W) [COLOR5RED]		
	Color5Red	<7:0>	Color 5 Red Component
70	Color 5 Green (R/W) [COLOR5GREEN]		
	Color5Green	<7:0>	Color 5 Green Component
71	Color 5 Blue (R/W) [COLOR5BLUE]		
	Color5Blue	<7:0>	Color 5 Blue Component
72	Color 6 Red (R/W) [COLOR6RED]		
	Color6Red	<7:0>	Color 6 Red Component
73	Color 6 Green (R/W) [COLOR6GREEN]		
	Color6Green	<7:0>	Color 6 Green Component
74	Color 6 Blue (R/W) [COLOR6BLUE]		
	Color6Blue	<7:0>	Color 6 Blue Component
75	Color 7Red (R/W) [COLOR7RED]		
	Color7Red	<7:0>	Color 7 Red Component

76 Color 7 Green (R/W) [COLOR7GREEN]

Color7Green	<7:0>	Color 7 Green Component

77 Color 7 Blue (R/W) [COLOR7BLUE]

Color7Blue	<7:0>	Color 7 Blue Component

V. OSD Control Register

78 OSD Color Select (R/W) [OSDCOLORSEL]

Osd1ColorSel	<1:0>	OSD1 color selection, 8 colors only apply when Font2byte= '1' and PixDepth1= '1' 00 select OSD1 colors from index 3..0 01 select OSD1 colors from index 7..4 10 select OSD1 colors from index 7..0 11 Reserved
Osd2ColorSel	<3:2>	OSD2 color selection, 8 colors only apply when Font2byte= '1' and PixDepth2= '1' 00 select OSD2 colors from index 3..0 01 select OSD2 colors from index 7..4 10 select OSD2 colors from index 7..0 11 Reserved
Font2byte	<4>	Two-byte font charter code mode, effective only when RomMode = '1'
Reserved	<7:5>	Reserved

79 Blink Time (R/W) [BLINKTIME]

BlinkTimer	<6:0>	Blinking timing value
BlinkType	<7>	0 Reverse color 1 Bypass

Note: OSD Blinking frequency = Vsync frequency / BlinkTimer

80 OSD Modes (R/W) [OSDMODE]

RomMode	<0>	Enable ROM mode	
		0	Internal RAM mode
		1	External ROM mode
Reserved	<1>	Tie to 0	
Number	<7:2>	Adjust rom address width to access external rom data	

Note: The method of select the Number value show on OSD application note

81 Logic Operation (R/W) [FOREOP]

Color0Op	<1:0>	Logic operation between color 0 and video	
		00	NOP, show only OSD
		01	OR, video or color 0
		10	AND, video and color 0
		11	XOR, video xor color 0
Color1Op	<3:2>	Logic operation between color 1 and video	
		00	NOP, show only OSD
		01	OR, video or color 1
		10	AND, video and color 1
		11	XOR, video xor color 1
Color2Op	<5:4>	Logic operation between color 2 and video	
		00	NOP, show only OSD
		01	OR, video or color 2
		10	AND, video and color 2
		11	XOR, video xor color 2
Color3Op	<7:6>	Logic operation between color 3 and video	
		00	NOP, show only OSD
		01	OR, video or color 3
		10	AND, video and color 3
		11	XOR, video xor color 3

83 Logic Operation (R/W) [FOREOP]

Color4Op	<1:0>	Logic operation between color 4 and video	
		00	NOP, show only OSD
		01	OR, video or color 4

		10	AND, video and color 4
		11	XOR, video xor color 4
	Color5Op	<3:2>	Logic operation between color 5 and video
		00	NOP, show only OSD
		01	OR, video or color 5
		10	AND, video and color 5
		11	XOR, video xor color 5
	Color6Op	<5:4>	Logic operation between color 6 and video
		00	NOP, show only OSD
		01	OR, video or color 6
		10	AND, video and color 6
		11	XOR, video xor color 6
	Color7Op	<7:6>	Logic operation between color 7 and video
		00	NOP, show only OSD
		01	OR, video or color 7
		10	AND, video and color 7
		11	XOR, video xor color 7

Note: Color 0 ~ 7 are defined in DIS#60~77.

82 Fading Alpha Value (R/W) [FADEALPHA]

FadeAlpha	<5:0>	The alpha factor for fading effect ranging
Reserved	<7:6>	Reserved

Note: FADEALPHA range from 00h to 20h, there is 33-level of fade-in/fade-out effect.

Output = Image * FADEALPHA/32 + OSD * (1 – (FADEALPHA /32))

Show only OSD: FADEALPHA = “000000“ --- minimum alpha value(00h)

Show only Image: FADEALPHA = “100000“ --- maximum alpha value(20h)

VI. OSD 1 Registers

84 OSD1 Control (R/W) [OSDCONTROL1]

PixDepth1	<0>	Number of bits per pixel of OSD1

		0	One bit per pixel
		1	Two bits per pixel
BlinkEn1	<1>	OSD1 blinking enable, effective when RomMode = '1'	
		0	Disable blinking
		1	Enable blinking
HZoom1	<3:2>	OSD1 horizontal zoom factor	
		00	OSD1 pixel H size equals to 1X of video pixel
		01	OSD1 pixel H size equals to 2X of video pixel
		10	OSD1 pixel H size equals to 4X of video pixel
		11	OSD1 pixel H size equals to 8X of video pixel
VZoom1	<5:4>	OSD1 vertical zoom factor	
		00	OSD1 pixel V size equals to 1X of video pixel
		01	OSD1 pixel V size equals to 2X of video pixel
		10	OSD1 pixel V size equals to 4X of video pixel
		11	OSD1 pixel V size equals to 8X of video pixel
Reserved	<6>	Reserved	
OsdEn1	<7>	OSD1 enable	
		0	Disable OSD1
		1	Enable OSD1

85 OSD1 ROM Start Address (R/W) [ROMSTARTADDR1]

RomStAddr1H	<7:0>	Bits<11:4> of OSD1 ROM start address (Unit: 16 bytes)

86 OSD1 Font Address Unit (R/W) [FONTADDRUNIT1]

RomStAddr1L	<3:0>	Bits<3:0> OSD1 ROM start address (Unit: 16 bytes)
FontAddrUnit1	<7:4>	OSD1 font address unit (n), font address is multiple of 2(n+5) bytes, max. is 216

90 OSD1 Horizontal Start (R/W) [OSDHSTART1]

OsdHStart1	<7:0>	On Screen Display horizontal start position (Unit: 8 video pixels)

91 OSD1 Vertical Start (R/W) [OSDVSTART1]

OsdVStart1	<7:0>	On Screen Display vertical start position (Unit: 4 video

lines)

92 OSD1 RAM Start Address (R/W) [RAMADDRST1]

RamAddrSt1	<7:0>	OSD1 RAM start address (Unit: 8 bytes)

8B OSD1 RAM Horizontal Stride MSB (R/W) [RAMSTRIDE1]

RamStride1H	<1:0>	Bits <9:8> of OSD1 RAM line stride (Unit: 1 bytes)
Reserved	<7:2>	Reserved

93 OSD1 RAM Horizontal Stride LSB (R/W) [RAMSTRIDE1]

RamStride1L	<7:0>	Bits<7:0> of OSD1 RAM line stride(Unit: 1 bytes)

94 OSD1 Bitmap Horizontal Size LSB (R/W) [BMAPHSIZE1]

BmapHSize1L	<7:0>	Bits<7:0> of OSD1 horizontal bitmap size (Unit: 1 OSD pixel)

95 OSD1 Bitmap Horizontal Size MSB (R/W) [BMAPHSIZE1]

BmapHSize1H	<1:0>	Bits<9:8> of OSD1 bitmap horizontal size
Reserved	<7:2>	Reserved

96 OSD1 Bitmap Horizontal Total Pixels LSB (R/W) [BMAPHTOTAL1]

BmapHTotal1L	<7:0>	Bits<7:0> of OSD1 bitmap horizontal total (Unit: 1 OSD pixel)

97 OSD1 Bitmap Horizontal Total Pixels MSB (R/W) [BMAPHTOTAL1]

BmapHTotal1H	<1:0>	Bits<9:8> of OSD1 bitmap horizontal total
Reserved	<7:2>	Reserved

98 OSD1 Bitmap Vertical Size LSB (R/W) [BMAPVSIZE1]

BmapVSize1L	<7:0>	Bits<7:0> of OSD1 bitmap vertical size(Unit: 1 OSD line)

99 OSD1 Bitmap Vertical Size MSB (R/W) [BMAPVSIZE1]

BmapVSize1H	<1:0>	Bits<9:8> of OSD1 bitmap vertical size
Reserved	<7:2>	Reserved

9A OSD1 Bitmap Vertical total Lines LSB (R/W) [BMAPVTOTAL1]

BmapVTotal1L	<7:0>	Bits<7:0> of OSD1 bitmap vertical total(Unit: 1 OSD line)

9B OSD1 Bitmap Vertical Total Lines MSB (R/W) [BMAPVTOTAL1]

BmapVTotal1H	<1:0>	Bits<9:8> of OSD1 bitmap vertical total
Reserved	<7:2>	Reserved

9C OSD1 Icon Horizontal Total (R/W) [ICONHTOTAL1]

IconHtotal1	<7:0>	OSD1 horizontal icon total (Unit: 1 icon)

9D OSD1 Icon Vertical Total (R/W) [ICONVTOTAL1]

IconVTotal1	<7:0>	OSD1 vertical icon total (Unit: 1 icon)

AE OSD1 Font Line Size (R/W) [FONTLINESIZE1]

Fontlinesize1	<7:0>	memory size of a line of font (Unit: 1 byte)

VII. OSD 2 Registers

88 OSD2 Control (R/W) [OSDCONTROL2]

PixDepth2	<0>	Number of bits per pixel of OSD2	
		0	One bit per pixel
		1	Two bits per pixel
BlinkEn2	<1>	OSD2 blinking enable, effective when RomMode = '1'	
		0	Disable blinking
		1	Enable blinking
Hzoom2	<3:2>	OSD2 horizontal zoom factor	
		00	OSD pixel H size equals to 1X of video pixel
		01	OSD pixel H size equals to 2X of video pixel
		10	OSD pixel H size equals to 4X of video pixel
		11	OSD pixel H size equals to 8X of video pixel
Vzoom2	<5:4>	OSD2 vertical zoom factor	
		00	OSD pixel V size equals to 1X of video pixel

		01	OSD pixel V size equals to 2X of video pixel
		10	OSD pixel V size equals to 4X of video pixel
		11	OSD pixel V size equals to 8X of video pixel
	Reserved	<6>	Reserved
	OsdEn2	<7>	OSD2 enable
		0	Disable OSD2
		1	Enable OSD2

89 OSD2 ROM Start Address (R/W) [ROMSTARTADDR2]

RomStAddr1H	<7:0>	Bits<11:4> of OSD2 ROM start address (Unit: 16 bytes)

8A OSD2 Font Address Unit (R/W) [FONTADDRUNIT2]

RomStAddr2L	<3:0>	Bits<3:0> OSD2 ROM start address (Unit: 16 bytes)
FontAddrUnit2	<7:4>	OSD1 font address unit (n), font address is multiple of 2(n+5) bytes, max. is 216

A0 OSD2 Horizontal Start (R/W) [OSDHSTART2]

OsdHStart2	<7:0>	On Screen Display horizontal start position (Unit: 8 video pixels)

A1 OSD2 Vertical Start (R/W) [OSDVSTART1]

OsdVStart2	<7:0>	On Screen Display vertical start position (Unit: 4 video lines)

A2 OSD2 RAM Start Address (R/W) [RAMADDRST2]

RamAddrSt2	<7:0>	OSD2 RAM start address (Unit: 8 bytes)

8C OSD2 RAM Horizontal Stride MSB (R/W) [RAMSTRIDE2]

RamStride2H	<1:0>	Bits <9:8> of OSD2 RAM line stride (Unit: 1 bytes)
Reserved	<7:2>	Reserved

A3 OSD2 RAM Horizontal Stride LSB (R/W) [RAMSTRIDE2]

RamStride2L	<7:0>	Bits<7:0> of OSD2 RAM line stride (Unit: 1 bytes)

A4 OSD2 Bitmap Horizontal Size LSB (R/W) [BMAPHSIZE2]

BmapHSize2L	<7:0>	Bits<7:0> of OSD1 horizontal bitmap size (Unit: 1 OSD pixel)

A5 OSD2 Bitmap Horizontal Size MSB (R/W) [BMAPHSIZE2]

BmapHSize2H	<1:0>	Bits<9:8> of OSD1 bitmap horizontal size
Reserved	<7:2>	Reserved

A6 OSD2 Bitmap Horizontal Total Pixels LSB (R/W) [BMAPHTOTAL2]

BmapHTotal2L	<7:0>	Bits<7:0> of OSD2 bitmap horizontal total (Unit: 1 OSD pixel)

A7 OSD2 Bitmap Horizontal Total Pixels MSB (R/W) [BMAPHTOTAL2]

BmapHTotal2H	<1:0>	Bits<9:8> of OSD2 bitmap horizontal total
Reserved	<7:2>	Reserved

A8 OSD2 Bitmap Vertical Size LSB (R/W) [BMAPVSIZE2]

BmapVSize2L	<7:0>	Bits<7:0> of OSD2 bitmap vertical size(Unit: 1 OSD line)

A9 OSD2 Bitmap Vertical Size MSB (R/W) [BMAPVSIZE2]

BmapVSize2H	<1:0>	Bits<9:8> of OSD2 bitmap vertical size
Reserved	<7:2>	Reserved

AA OSD2 Bitmap Vertical total Lines LSB (R/W) [BMAPVTOTAL2]

BmapVTotal2L	<7:0>	Bits<7:0> of OSD2 bitmap vertical total(Unit: 1 OSD line)

AB OSD2 Bitmap Vertical Total Lines MSB (R/W) [BMAPVTOTAL2]

BmapVTotal2H	<1:0>	Bits<9:8> of OSD2 bitmap vertical total
Reserved	<7:2>	Reserved

AC OSD2 Icon Horizontal Total (R/W) [ICONHTOTAL2]

IconHtotal2	<7:0>	OSD2 horizontal icon total (Unit: 1 icon)

AD OSD2 Icon Vertical Total (R/W) [ICONVTOTAL2]

	IconVTotal2	<7:0>	OSD2 vertical icon total (Unit: 1 icon)

AF OSD2 Font Line Size (R/W) [FONTLINESIZE2]

	Fontlinesize2	<7:0>	memory size of a line of font (Unit: 1 byte)

VIII. Alpha Blending Registers

B0 Mixer Configuration (R/W) [MIXERCONFIG]

	MixerMode	<1:0>	Mixer Mode output
		00	PS image output only
		01	SS image output only
		10	SS image on PS image output
		11	Mixing PS & SS (Enable Mixer block)
	KeyType	<3:2>	Select alpha key type
		00	PS output enable (pshde and psvde)
		01	SS output enable (sshde and ssvde)
		10	PS & Chroma compare
		11	SS & Chroma compare
	PSBackEn	<4>	Select image or background color on PS
		0	Image
		1	Background color
	SSBackEn	<5>	Select image or background color on SS
		0	Image
		1	Background color
	Reserved	<7:6>	Reserved

B1 PS Alpha Value (R/W) [PSALPHA]

	PSAlpha	<7:0>	PS alpha value

B2 SS Alpha Value (R/W) [SSALPHA]

	SSAlpha	<7:0>	SS alpha value

B3 Desktop Color Component Red (R/W) [DESKR]

	DeskColorRed	<7:0>	Desktop color red

B4 Desktop Color Component Green (R/W) [DESKG]

	DeskColorGreen	<7:0>	Desktop color green

B5 Desktop Color Component Blue (R/W) [DESKB]

	DeskColorBlue	<7:0>	Desktop color blue

B6 PS Background Color Component Red (R/W) [PSBACKR]

	PSBackRed	<7:0>	PS background color red

B7 PS Background Color Component Green (R/W) [PSBACKG]

	PSBackGreen	<7:0>	PS background color green

B8 PS Background Color Component Blue (R/W) [PSBACKB]

	PSBackBlue	<7:0>	PS background color blue

B9 SS Background Color Component Red (R/W) [SSBACKR]

	SSBackRed	<7:0>	SS background color red

BA SS Background Color Component Green (R/W) [SSBACKG]

	SSBackGreen	<7:0>	SS background color green

BB SS Background Color Component Blue (R/W) [SSBACKB]

	SSBackBlue	<7:0>	SS background color blue

BC Chroma Color Component Red (R/W) [CHROMAR]

	ChromaRed	<7:0>	Chroma red value

BD Chroma Color Component Green (R/W) [CHROMAG]

	ChromaGreen	<7:0>	Chroma green value

BE Chroma Color Component Blue (R/W) [CHROMAB]

	ChromaBlue	<7:0>	Chroma blue value

IX. Film Detection/Motion Adaptive Registers

C4 Motion Pixels Threshold LSB (R/W) [MOTIONCNTTH]

MvCntThL	<7:0>	Bit<7:0> of motion counter threshold

C5 Motion Pixels Threshold MSB (R/W) [MOTIONCNTTH]

MvCntThH	<7:0>	Bit<15:8> of motion counter threshold

C6 Lumina(Y) Threshold (R/W) [LUMATH]

YThL	<6:0>	Y threshold for film & motion adaptive
Reserved	<7>	Reserved

C7 Chroma(C) Threshold (R/W) [CHROMATH]

CThH	<6:0>	C threshold for film & motion adaptive
Reserved	<7>	Reserved

C8 Deinterlacing Control Register(R/W) [MCCTRL]

MCEn	<0>	Motion Adaptive Deinterlacing Enable
	0	Field Merge Deinterlacing Mode
	1	Motion Adaptive Deinterlacing Mode
MvMode	<1>	Motion Estimation Type
	0	Y/C Comparison
	1	Y Comparison Only
Reserved	<2>	Reserved
TestMv	<3>	Display Motion Part
Reserved	<7:4>	Reserved

C9 Film Detection Control Register(R/W) [FILMCTRL]

FilmDetEn	<0>	Film detection enable
	0	Disable
	1	Enable
ResetType	<1>	Non-Film Detection Type

		0	H/W Auto Detection
		1	S/W Reset to Non-Film after Film Detected
	FilmReset	<2>	Reset Film Detection, depending on bit1
		0	Disable Reset
		1	Reset when bit 1 is turn on
	Reserved	<3>	Reserved
	PdMatch	<7:4>	Number of film sequence matched

CE Motion Pixel Numbers LSB (R) [MVCNT]

MvCountL	<7:0>	Bit<7:0> of pixels numbers of difference between 2-field/frame

CF Motion Pixel Numbers MSB (R) [MVCNT]

MvCountH	<7:0>	Bit<15:8> of pixels numbers of difference between 2-field/frame

X. Keystone/Sharpness Registers

CB Keyston/Sharpness Control Register(R/W) [SHPKEYCTRL]

ShapEn	<0>	Sharpness enable	
		0	Disable
		1	Enable
KeyEn	<4>	Keystone enable	
		0	Disable
		1	Enable
Interlace	<5>	Interlace output enable	
EvenField	<6>	Even field mode	
TriLevel	<7>	Tri level analog data output enable	

C0 Keystone Parameters Address LSB (R/W) [KEYADDR]

KeyAddrL	<7:0>	Bit<7:0> of keystone fifo address

C1 Keystone Parameters Address MSB (R/W) [KEYADDR]

KeyAddrH	<3:0>	Bit<11:8> of keystone fifo address
Reserved	<6:4>	Reserved
KeyWriteEn	<7>	Keystone fifo write enable
		0 Disable
		1 Enable

Note: Keystone parameter for each scan line is stored into 1280x32 SRAM inside AL310. KeyAddr is the address of read/write pointer of this SRAM.

XI. Tri-Level Sync Registers

D0 Tri Level Sync Parameter (W) [TRISYNCA]

PeriodA	<7:0>	Tri level sync parameter Period_a

D1 Tri Level Sync Parameter (W) [TRISYNCB]

PeriodB	<7:0>	Tri level sync parameter Period_a

D2 Tri Level Sync Parameter (W) [TRISYNCD1]

Delta1	<6:0>	Bit<6> is sign bit
		ex. 60h means from blank_level , - 32 every unit
Reserved	<7>	Reserved

D3 Tri Level Sync Parameter (W) [TRISYNCD2]

Delta2	<6:0>	Bit<6> is sign bit
		ex. 20h means from sync_level, + 32 every unit
Reserved	<7>	Reserved

D4 Tri Level Sync Parameter (W) [TRISYNBLANK]

BlankData	<7:0>	Data of blanking period

D7 Tri Level Sync Parameter (W) [TRISYNCLEVEL]

SyncLevel	<7:0>	Sync level value

XII. SS Border Registers

E0 SS Left Border Start LSB (W) [SSLFSTART]

SSLFStartL	<7:0>	Bits<7:0> of SS left boder start position (Unit: 1 pixel)

E1 SS Left Border Start MSB (W) [SSLFSTART]

SSLFStartH	<3:0>	Bits<11:8> of SS left boder start position
Reserved	<7:4>	Reserved

E2 SS Right Border Start LSB (W) [SSRTSTART]

SSRTStartL	<7:0>	Bits<7:0> of SS right boder start position (Unit: 1 pixel)

E3 SS Right Border Start MSB (W) [SSRTSTART]

SSRTStartH	<3:0>	Bits<11:8> of SS right boder start position
Reserved	<7:4>	Reserved

E4 SS Top Border Start LSB (W) [SSTPSTART]

SSTPStartL	<7:0>	Bits<7:0> of SS top boder start position (Unit: 1 pixel)

E5 SS Top Border Start MSB (W) [SSTPSTART]

SSTPStartH	<3:0>	Bits<11:8> of SS top boder start position
Reserved	<7:4>	Reserved

E6 SS Bottom Border start LSB (W) [SSBTSTART]

SSBTStartL	<7:0>	Bits<7:0> of SS bottom boder start position (Unit: 1 pixel)

E7 SS Bottom Border start MSB (W) [SSBTSTART]

SSBTStartH	<3:0>	Bits<11:8> of SS bottom boder start position
Reserved	<7:4>	Reserved

E8 SS Border width (W) [SSBWIDTH]

SSBWidth	<7:0>	SS boder width (Unit: 1 pixel)

E9 SS Border Color Red (W) [SSBRED]

SSBRed	<7:0>	SS boder red color

EA SS Border Color Green (W) [SSBGREEN]

SSBGreen	<7:0>	SS boder green color

EB SS Border Color Blue (W) [SSBBULE]

SSBBlue	<7:0>	SS boder blue color

XIII. Display Parameter Registers

C2 Tune Display Horizontal Sync Phase (R/W) [DISTUNEHS]

DisHsDelay	<4:0>	Output horizontal sync delay (Unit: 1 oclk)

CC Tune Display Pixel Clock Phase (R/W) [DISTUNESCLK]

TuneSclk	<2:0>	Phase delay number(8 steps)
	<4:3>	Phase delay types
	00	Sclk
	01	Sclk + delay phase
	10	Inversed Sclk
	11	Inversed Sclk + delay phase
Reserved	<7:5>	Reserved

CD Tune Display Pixel Clock by 2 Phase (R/W) [DISTUNEDSCLK]

TuneDSclk	<2:0>	Phase delay number(8 steps)
	<4:3>	Phase delay types
	00	DSclk
	01	DSclk + delay phase
	10	Inversed DSclk
	11	Inversed DSclk + delay phase
Reserved	<7:5>	Reserved

CA Phase Detection Control Register(R/W) [PHASECTRL]

PhaseEn	<0>	Phase detection Enable	
		0	Disable
		1	Enable
PhaseMode	<2:1>	Phase detection precision	
		00	8-bit comparison
		01	7-bit comparison
		10	6-bit comparison
		11	5-bit comparison
Reserved	<7:3>	Tie to “00110“	

D7 Display Horizontal Total LSB (R) [DISHTOTAL]

HTotalCntL	<7:0>	Bit<7:0> of display horizontal total count

D8 Display Horizontal Total MSB (R) [DISHTOTAL]

HTotalCntH	<2:0>	Bit<10:8> of display horizontal total count
Reserved	<7:3>	Reserved

D9 Display Vertical Total LSB (R) [DISVTOTAL]

VTotalCntL	<7:0>	Bit<7:0> of display vertical total count

DA Display Vertical Total MSB (R) [DISVTOTAL]

VTotalCntH	<2:0>	Bit<10:8> of display vertical total count
Reserved	<7:3>	Reserved

DB Phase Counter LSB (R) [PHASECNT]

PhaseCntL	<7:0>	Bit<7:0> of phase count value

DC Phase Counter MSB (R) [PHASECNT]

PhaseCntH	<4:0>	Bit<12:8> of phase count value
Reserved	<7:5>	Reserved

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

(Excessive ratings are harmful to the lifetime. Only for user guidelines, not tested.)

Parameter		3.3V Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Input Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage Temperature	-40 ~ +125	°C
T_{VSOL}	Vapor Phase Soldering Temperature (15 Sec.)	220	°C

10.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V
T_{AMB}	Ambient Op. Temperature	0		+70	°C

10.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C; Some parameters are guaranteed by design only, not production tested)

Parameter	3.3V Rating			Unit
	Min.	Typical	Max.	

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
V_{IH}	Hi-level Input Voltage	0.7 V_{DD}	-	V_{DD}	V
V_{IL}	Lo-level Input Voltage	0		0.3 V_{DD}	V
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current	-5	-	+5	μA
I_{LO}	Output Leakage Current	-5	-	+5	μA

10.4 AC Characteristics

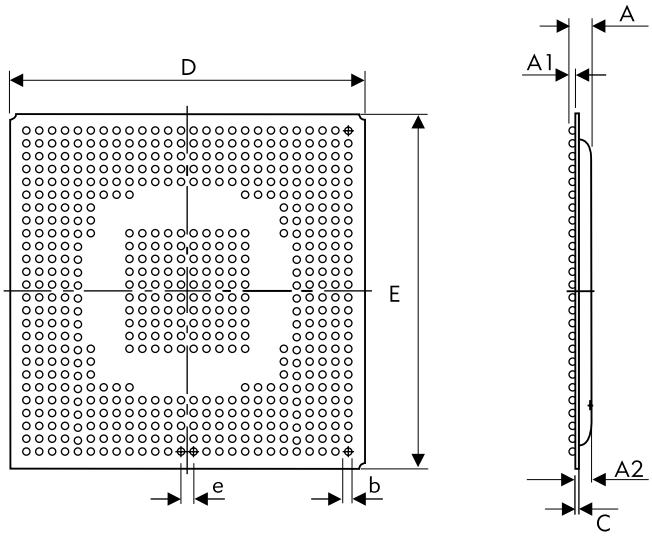
(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C; Some parameters are guaranteed by design only, not production tested)

11 Timing Diagrams

TBD.

12 Mechanical Drawing- BGA-308

PACKAGE OFFERING & OUTLINE DIMENSION



Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Body Thk.	Substrate Thk.
D	E	N	e	b	A	A1	A2	c
14	22	119	1.27	0.75	2.16	0.60	1.56	0.56
17	17	256	1.00	0.50	1.80	0.40	1.21	0.36
23	23	233, 241	1.27	0.75	2.33	0.60	1.73	0.56
		376, 420, 456, 484	1.00	0.60	2.23	0.50	1.73	0.56
27	27	256, 272, 292, 308, 316, 320, 324, 328, 330, 336, 348, 350, 352, 365, 376	1.27	0.75	2.33	0.60	1.73	0.56
		484	1.00	0.60	2.23	0.50	1.73	0.56
31	31	304, 329, 345, 350, 385, 409, 457	1.27	0.75	2.33	0.60	1.73	0.56
		556	1.00	0.55	2.18	0.45	1.73	0.56
		560, 900	1.00	0.60	2.23	0.50	1.73	0.56
35	35	352, 387, 388, 400, 432, 436, 452, 456, 472, 476, 484, 492, 496, 502, 504, 505, 508, 510, 516, 524, 548, 556, 561, 637, 728	1.27	0.75	2.33	0.60	1.73	0.56
		680, 700, 1156	1.00	0.60	2.23	0.50	1.73	0.56
37.5	37.5	480, 576, 601, 618, 673	1.27	0.75	2.33	0.60	1.73	0.56
40	40	596	1.27	0.75	2.33	0.60	1.73	0.56

(Unit: mm)

CONTACT INFORMATION

Averlogic Technologies Corp.
4F, No. 514, Sec. 2, Cheng Kung Rd., Nei-Hu Dist., Taipei, Taiwan
Tel: +886 2-27915050
Fax: +886 2-27912132
E-mail: sales@averlogic.com.tw
URL: http://www.averlogic.com.tw

Averlogic Technologies, Inc.
90 Great Oaks Blvd. #204, San Jose, CA 95119, U.S.A.
Tel: 1 408 361-0400
Fax: 1 408 361-0404
E-mail: sales@averlogic.com
URL: http://www.averlogic.com