POWER
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Marvell Solutions

88PG8x7 Family
Field Programmable DSP Switcher™

1 MHz, 4.5A Peak Current-Limit Step-Down Regulator with AnyVoltage™ Technology

Advance Datasheet, Patent Pending

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Document Status	
Advance Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Preliminary Information	This document contains preliminary data, and a revision of this document will be published at a later date. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
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Overview

The 88PG8x7 family is intelligent digital synchronous Step-Down (Buck) switching regulators with on-chip Low-Drop-Out (LDO) regulator controllers housed in a 3 mm X 3 mm QFN-16 package. Internally self-compensated, these step-down regulators require no external compensation and work with low-ESR output capacitors to simplify the design, minimize the board space, and reduce the amount of external components. The switching frequency for the step-down regulator is 1 MHz, allowing the use of low profile surface mount inductors and low value capacitors. The step-down regulator includes programmable output voltage to provide the user the ability to easily set the output voltage with external resistors, logic control, or serial data interface. The output voltage range is 0.72V to 3.63V.

The LDO regulator controller with an external P-Channel MOSFET forms a low dropout regulator capable of driving 800 mA output current. The output voltage of the LDO regulator is fixed. See the “Ordering Information” section for more details.

Other key features of the 88PG8x7 family include soft start and auto power MOSFET detection for the LDO regulator controller, an internal current limit for the step-down regulator, an undervoltage lockout, thermal shutdown, over voltage protection, and a Power-On Reset (POR) signal.

Features

- Tiny 3 mm X 3 mm QFN-16 package
- 1 MHz Switching frequency
- Low quiescent current of 1.9 mA (typ.)
- Stable with ceramic output capacitors
- No external compensation required
- Over 95% efficiency
- Peak switch current limit up to 4.5A
- Input voltage range: 2.75V to 5.5V
- Serial / Logic Programmability
- Any Voltage™ Technology provides 64 output voltage selections to provide flexibility
- Programmable output voltage range:
  - 0.72V to 3.63V
- P-Channel LDO regulator controller with programmable current limit
- Lead-free Packages
- Built-in undervoltage lockout
- Over voltage protection
- Thermal shutdown protection
- Output voltage margining capability

Application

- Portable computing
- Disk drive power supplies
- 3.3V PCI Express Bus

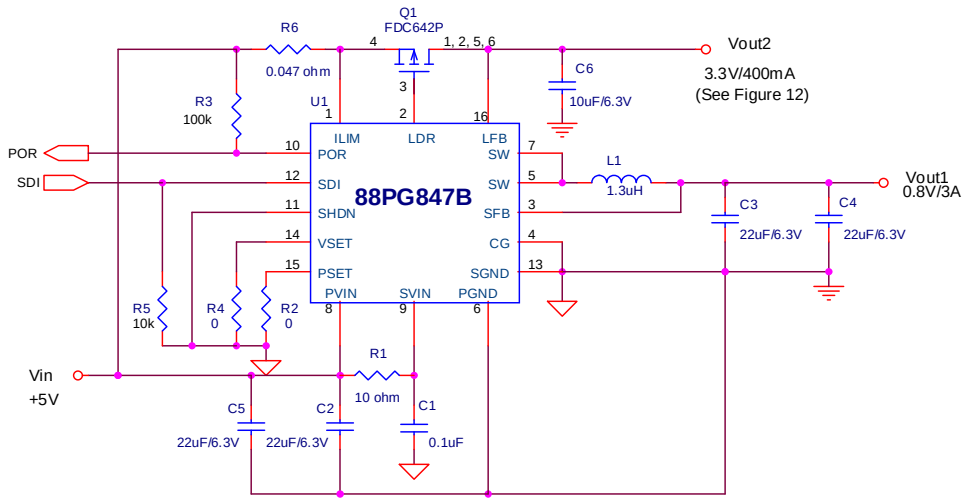

Figure 1: Typical High Efficiency 5V to 0.8V/3A Step-Down Regulator

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Table 1 provides information about other devices from the same product family.

Table 1: Product Selector Table

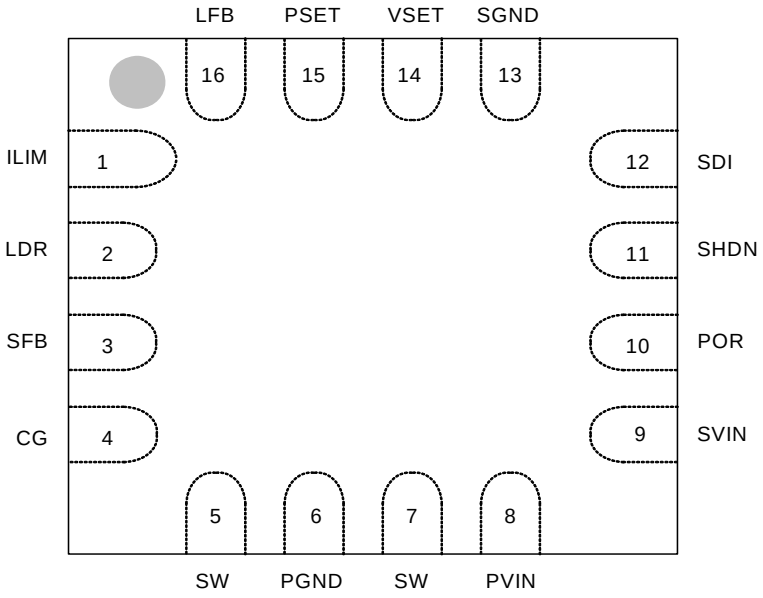
Part Number	Peak Current Limit	DC Loading
88PG847x	4.5A	3.0A
88PG837x	3.0A	2.0A
88PG827x	2.5A	1.6A
88PG817x	1.5A	1.0A
88PG807x	0.75A	0.5A

The devices listed in Table 1 have the same input and output voltage range for the step-down regulator.

Section 1. Signal Description

1.1 Pin Configuration

Figure 2: 88PG8x7 Family 3X3 mm QFN-16 Package - Top View



1.2 Pin Type Definitions

Table 2: Pin Type Definitions

Pin Type	Definitions
I	Input only
O	Output only
S	Supply
NC	Not Connected
GND	Ground

1.3 Pin Description

Table 3 provides pin descriptions for the 88PG8x7.

Table 3: Pin Description

Pin #	Pin Name	Pin Type	Pin Function
1	ILIM	I	Current-Limit Sense Pin for the LDO Regulator A built-in offset of 50 mV (typical) between SVIN and ILIM in conjunction with the sense resistor is used to set the current-limit threshold for the LDO regulator controller. Connecting this pin to SVIN disables the internal current limit circuitry. When the LDO controller is not used, the LDR pin must be left floating, the LFB pin must be connected to GND, and connect ILIM to VIN. This will reduce the supply current.
2	LDR	O	LDO Regulator Controller Driver Connect to the gate of an external P-channel MOSFET. The external P-Channel MOSFET needs to have a threshold of -2.5V or -1.8V and input capacitance (Ciss) of less than 1000 pF. When the LDO controller is not used, the LDR pin must be left floating, the LFB pin must be connected to GND, and connect ILIM to VIN. This will reduce the supply current.
3	SFB	I	Switching Regulator Feedback Senses the output voltage of the switching regulator.
4	CG	I	Connect to Ground This pin must be connected to ground.
5,7	SW	O	Switch Node Internal power MOSFET drain. This pin must connect to an external inductor.
6	PGND	GND	Power Ground The power ground must connect to the negative terminal of the input and output capacitors.

Table 3: Pin Description (Continued)

Pin #	Pin Name	Pin Type	Pin Function
8	PVIN	S	Power Input Voltage Internal power MOSFET source. Connect the decoupling capacitors between PVIN and PGND and position it as close as possible to the IC.
9	SVIN	S	Signal Input Voltage The input voltage is 2.75V to 5.5V for internal circuitry. Connect a 0.1 µF decoupling capacitor between SVIN and SGND and position it as close as possible to the IC.
10	POR	O	Power-On Reset Power-On Reset is an open drain output to indicate the status of the output voltage. The output pin goes high 40 ms after the output voltage is within the specified tolerance.
11	SHDN	I	Shutdown Logic high (≥ 2.0V) disables the switching step-down regulator and the LDO regulator controller. In shutdown, the switch node for the step-down regulator is high impedance. Logic low (≤ 0.8V) enables the step-down switching regulator and the LDO regulator controller. The high signal has to be at least 20 µs to disable both regulators.
12	SDI	I	Serial Data Input: The input data into this pin is used to program the output voltage (see section 3.2). This pin must be connected to ground if not used.
13	SGND	GND	Signal ground: This pin must connect to the power ground.
14	VSET	I	Voltage Set 1) This is used for selecting the output voltage level, when it is connected to SGND or SVIN in conjunction with PSET connection to SGND or SVIN. 2) Connect to an external resistor to ground to set the output voltage of the step-down switching regulator. See the “Electrical Characteristics” table for resistor values and Output Voltage Setting section. The total capacitance across this pin and SGND should be equal to 25 pF or less. Use resistors with tolerance 5% or better.
15	PSET	I	Percent Set 1) This is used for selecting the output voltage level when it is connected to SGND or SVIN in conjunction with VSET connection to SGND or SVIN. 2) Connect an external resistor to ground to set the output voltage of the step-down switching regulator. See the “Electrical Characteristics” table for resistor values and Output Voltage Setting section. Use resistor value with tolerance 5% or better.
16	LFB	I	LDO Regulator Controller Feedback Sense the output voltage of the LDO regulator. Connect to the drain of the P-channel MOSFET. When the LDO controller is not used, the LDR pin must be left floating, the LFB pin must be connected to GND, and connect ILIM to SVIN. This will reduce the supply current.

Section 2. Electrical Specifications

2.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Range	Units
Signal Input Voltage to SGND = PGND	S_{VIN}	-0.3 to 6.0	V
Power Input Voltage to SGND = PGND	P_{VIN}	-0.3 to 6.0	V
Switch Voltage to SGND = PGND	V_{SW}	-0.3 to (S_{VIN} +0.3)	V
Switching Regulator Feedback Voltage to SGND = PGND	V_{SFB}	-0.3 to (S_{VIN} +0.3)	V
Voltage Set to SGND = PGND	V_{VSET}	-0.3 to (S_{VIN} +0.3)	V
Percentage Set Voltage to SGND=PGND	V_{PSET}	-0.3 to (S_{VIN} +0.3)	V
Current Limit Voltage to SGND=PGND	V_{ILIM}	-0.3 to (S_{VIN} +0.3)	V
LDO Regulator Controller Driver Voltage to SGND=PGND	V_{LDR}	-0.3 to (S_{VIN} +0.3)	V
LDO Regulator Controller Feedback Voltage to SGND=PGND	V_{LFB}	-0.3 to (S_{VIN} +0.3)	V
Shutdown Voltage to SGND = PGND	V_{SHDN}	-0.3 to (S_{VIN} +0.3)	V
POR Voltage to SGND = PGND	V_{POR}	-0.3 to (S_{VIN} +0.3)	V
SDI Voltage to SGND = PGND	V_{SDI}	-0.3 to (S_{VIN} +0.3)	V
Operating Temperature Range[2]	T_{OP}	-40 to 85	°C
Maximum Junction Temperature	T_{JMAX}	125	°C
Storage Temperature Range	T_{STOR}	-65 to 150	°C
ESD Rating[3]		2	kV

1. Exceeding the absolute the maximum rating may damage the device
2. Specifications over the –40 °C to 85 °C operating temperature ranges are assured by design, characterization and correlation with statistical process controls
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF

2.2 Recommended Operating Conditions[1]

Parameter	Symbol	Range	Units
Signal Input Voltage	S_{VIN}	2.75 to 5.5	V
Power Input Voltage	P_{VIN}	2.75 to 5.5	V
Package Thermal Resistance[2]	θ_{JA}	70	°C/W
	θ_{JC}	19	°C/W

1. This device is not guaranteed to function outside the specified operating range
2. Test on 4-layer (JESD51-7) and vias (JESD51-5) board

2.3 Electrical Characteristics

The following applies unless otherwise noted: S_{VIN} = P_{VIN} = V_{VSET} = V_{PSET} = 5.0V, V_{OUT} = 1.5V, V_{SHDN} = V_{CG} = SGND = PGND, $L_{(BUCK)}$ = 1.3 µH, $C_{OUT\ (BUCK)}$ = 2 x 22 µF (Ceramic), PFET= FDC642P, $C_{OUT\ (LDO)}$ = 10 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C.**

Parameter	Symbol	Conditions	Min	Type	Max	Units
Signal Input Voltage Range	S_{VIN}	S_{VIN} = P_{VIN}	**2.75**		**5.5**	V
Power Input Voltage Range	P_{VIN}		**2.75**		**5.5**	V
Total Quiescent Current		No load, with LDO		1.9		mA
		No load, Without LDO, V_{LIM} = PV_{IN}, V_{LDR} = Float, V_{LFB} = 0V		1.2		mA
Shutdown Supply Current	I_{SVIN}	V_{SHDN} = S_{VIN} = 5.0V		1	50	µA
Undervoltage Lockout	V_{UVLO}	High threshold, SV_{IN} increasing		2.65	2.70	V
		Low threshold, SV_{IN} decreasing		2.55	2.60	V
Over-voltage Protection	V_{OVP}	High threshold, SV_{IN} increasing		5.7		V
		Low threshold, SV_{IN} decreasing		5.6		V
Shutdown Threshold Voltage	V_{SHDN}	Enable regulators			0.8	V
		Disable regulators	2.0			V
Shutdown Pin Input Current	I_{SHDN}	V_{SHDN} = 5.0V			5.0	µA
		V_{SHDN} = 0V			5.0	µA
Over-temperature Thermal Shutdown	T_{OTS}	T_J increasing (Disable regulators)		150		°C
		T_J decreasing (Enable regulators)		105		°C

2.4 Switching Step-down Regulator

The following applies unless otherwise noted: S_{VIN} = P_{VIN} = V_{VSET} = V_{PSET} = 5.0V, V_{OUT} = 1.5V, V_{SHDN} = V_{CG} = SGND = PGND, L = 1.3 µH, C_{OUT} = 2 x 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C**.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage		R_{VSET} = 11K, PWM mode		0.8		V
		V_{VSET} = SGND, V_{PSET} = SGND, PWM mode				
		R_{VSET} = 18.7K, PWM mode		1.0		
		V_{VSET} = SGND, V_{PSET} = SVIN, PWM mode				
		R_{VSET} = 31.6K, PWM mode		1.2		
		V_{VSET} = SVIN, V_{PSET} = SGND, PWM mode				
		R_{VSET} = 53.6K, PWM mode		1.5		
		V_{VSET} = SVIN, V_{PSET} = SVIN, PWM mode				
		R_{VSET} = 97.6K, PWM mode		1.8		
		R_{VSET} = 165K, PWM mode		2.5		
		R_{VSET} = 280K, PWM mode		3.0		
		R_{VSET} = 475K, PWM mode		3.3		
Percentage Set		R_{PSET} = 11K		-10		%
		R_{PSET} = 18.7K		-7.5		
		R_{PSET} = 31.6K		-5		
		R_{PSET} = 53.6K		-2.5		
		R_{PSET} = 97.6K		2.5		
		R_{PSET} = 165K		5		
		R_{PSET} = 280K		7.5		
		R_{PSET} = 475K		10		
Output Voltage Line Regulation	V_{LNREG}	S_{VIN} = P_{VIN} = 3.0V to 5.0V V_{OUT} = 1.5V I_{LOAD} = $I_{OUT(MAX)}$/4		0.10		%
Output Voltage Load Regulation	V_{LDREG}	S_{VIN} = P_{VIN} = 5.0V V_{OUT} = 1.5V I_{LOAD} = $I_{OUT(MAX)}$/4 to $I_{OUT(MAX)}$		0.10		%
Switching Frequency	f_{SW}	PWN mode		0.9		MHz

2.4 Switching Step-down Regulator (Continued)

The following applies unless otherwise noted: S_{VIN} = P_{VIN} = V_{VSET} = V_{PSET} = 5.0V, V_{OUT} = 1.5V, V_{SHDN} = V_{CG} = SGND = PGND, L = 1.3 µH, C_{OUT} = 2 x 22 µF (Ceramic), T_A = 25 °C. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C**.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum Peak Switch Current Limit	I_{LIM}	88PG847		4.5		A
		88PG837		3.0		
		88PG827		2.5		
		88PG817		1.5		
		88PG807		0.75		
Output Current	I_{OUT}	88PG847 L = 1.3 µH			**3.0**	A
		88PG837 L = 2.0 µH			**2.0**	
		88PG827 L = 3.3 µH			**1.6**	
		88PG817 L = 4.7 µH			**1.0**	
		88PG807 L = 4.7 µH			**0.5**	
Switch Leakage Current	I_{LSW}	S_{VIN} = P_{VIN} = V_{SHDN} = 5.0V V_{SW} = 5V		1	50	µA
		S_{VIN} = P_{VIN} = V_{SHDN} = 5.0V V_{SW} = 0V		1		
Power-On Reset Threshold Voltage	V_{PORTH}	V_{OUT} ≥ 1.35V		V_{OUT}* 90%		V
		V_{OUT} < 1.32V		V_{OUT}- 130 mV		
Power-On Reset Output Low Voltage	V_{PORL}	I_{SINK} = 2 mA, V_{SHDN} = SGND = PGND			0.4	V
Power-On Reset Leakage Current	I_{POR}	V_{SHDN} = 5.0V		1		µA
Power-On Reset Delay	t_{RESET}			40		ms

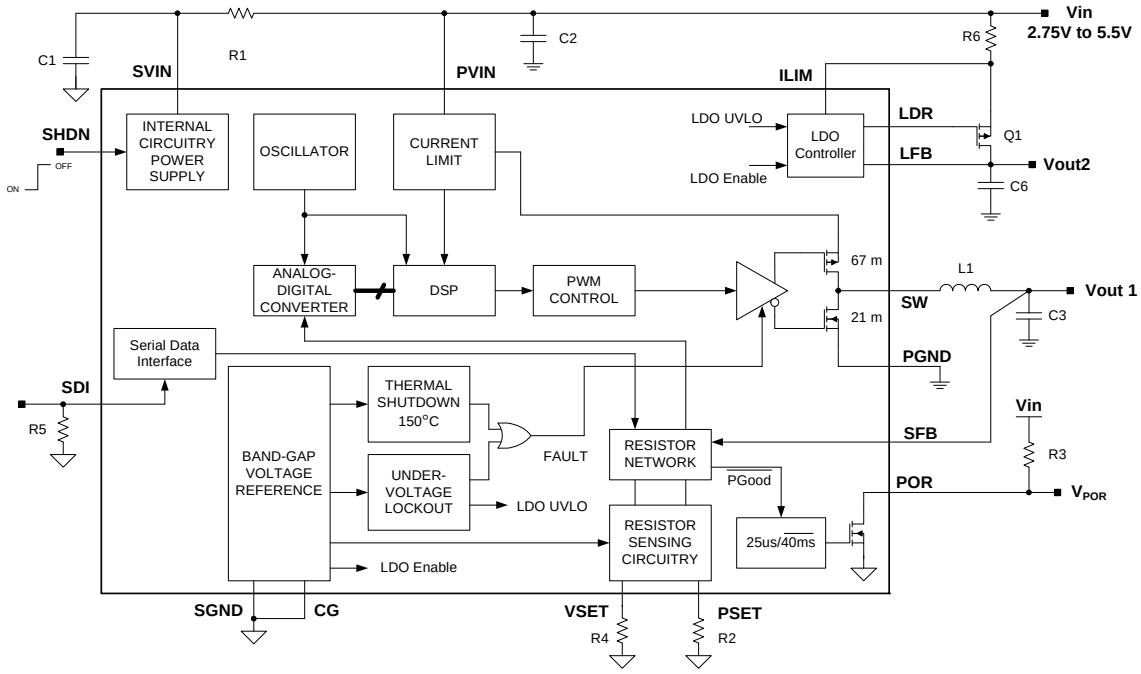
2.5 LDO Regulator Controller

The following applies unless otherwise noted: $S_{VIN} = P_{VIN} = 5.0V$, $V_{SHDN} = SGND = PGND$, PFET= FDC642P, $C_{OUT\ (LDO)} = 10\ \mu F$, $T_A = 25\ °C$. **Bold values indicate -40 °C ≤ T_A ≤ 85 °C.**

Parameter	Symbol	Conditions	Min	Type	Max	Units
88PG8X7B Output Voltage	V_{OUT}	I_{LOAD} = 10 mA		3.3		V
88PG8X7E Output Voltage	V_{OUT}	I_{LOAD} = 10 mA		2.5		V
Output Voltage		Room Temp, I_{LOAD} = 10 mA		±1		%
		Over Temp, I_{LOAD} = 10 mA		±2		
Line Regulation	V_{LNREG}	$S_{VIN} = P_{VIN}$ = 3.5V to 5.0V, V_{OUT} = 3.3V, I_{LOAD} = 10 mA		0.1		%
Load Regulation	V_{LDREG}	$S_{VIN} = P_{VIN}$ = 5.0V, V_{OUT} = 3.3V, I_{LOAD} = 10 mA to 800 mA		0.1		%
Current-Limit Threshold	V_{ILTH}	S_{VIN}-V_{ILIM}		50		mV

Section 3. Functional Description

Figure 3: 88PG8x7 Block Diagram

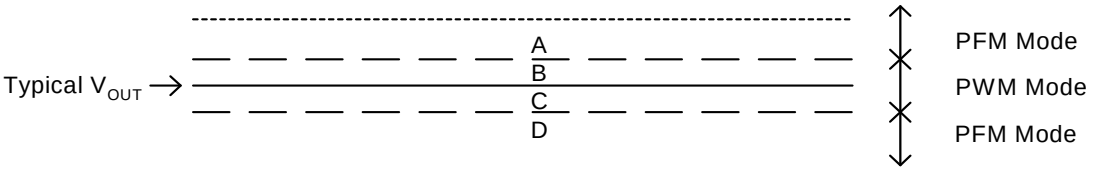


3.1 Regulation and Start-up

The step-down switching regulator uses Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) modes to regulate the output voltage using digital control. The mode of operation depends on the level of output current and the output voltage.

In steady states, the step-down switching regulator monitors the current flowing through the inductor to determine if the regulator is handling heavy or light load applications. For heavy load applications, the step-down regulator operates in the PWM mode (B and C) to minimize the ripple current for optimum efficiency and to minimize the ripple output voltage. The step-down regulator operates in the PFM and Discontinuous Conduction Mode (DCM) (A) to limit the switching actions for optimum efficiency in light load applications. In this mode, the average output voltage is slightly higher than the average output voltage for heavy transient load applications.

Figure 4: Output Voltage Window



3.1.1 Digital Soft Start

During start-up, the 88PG8x7 provides a soft start function. Soft start reduces surge currents from input voltage and provides well-controlled output voltage rise characteristics. Figure 5 shows that the rise time for a 88PG8x7 increases from 20 µs at for a 0.8V output to 70 µs for a 3.3V output with a 20 mA load. Higher load current or larger output capacitance will increase the rise time. The load current is increased to 3A (1.1 ohms) in Figure 6. The 3.3V output rise time nearly doubles to 130 µs with this load.

The 88PG8x7 has an internal switch current limit that operates on a cycle-by-cycle basis and limits the peak switch current. During soft start, the current limit threshold begins at approximately 34% of the peak current limit threshold and ramps to 100% in 7 steps at 25 µs per step (see Figure 7). During the switch first cycle, the high-side switch stays on until the switch current reaches the first current limit threshold (see Figure 8) which takes less than 1 µs. Then, the high-side switch turns off for a fixed off-time. If the output voltage is still low in 25 µs, then the current limit threshold increases to the next level. As can be seen from Figure 4, only 25 µs or 1 current step is required for the output to reach 0.8V and 75 µs or 3 current steps for 3.3V.

During soft start, the 88PG8x7 feeds a relatively constant current to the output capacitor in the first two steps. The average switch current during this period is approximately 2A. If more then 2 steps are required, then the switch current limit (I_{LIM}) will need to increase. The output voltage rise time is dependent on the value of the output capacitor, the output voltage, the load current (I_{OUT}), and the internal switch current limit circuitry and can be calculated using the following equation.

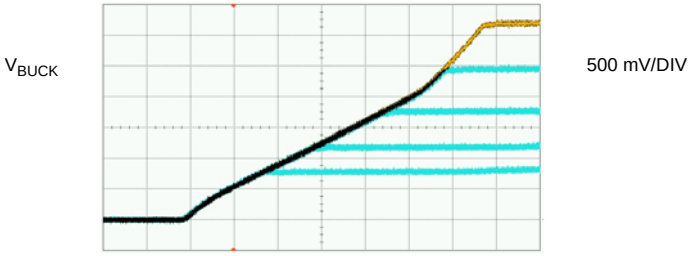
$$\text{Rise Time} = \frac{(C_{OUT} \times V_{OUT})}{(I_{LIM} - I_{OUT})}$$

$$= \frac{2 \times 22\mu F \times 3.3V}{2.0A - 0A}$$

$$= 72.6\mu S$$

Figure 5: Soft Startup

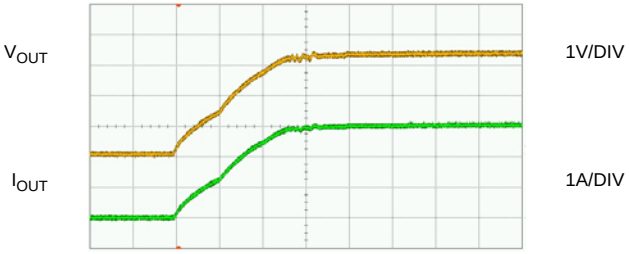
(0.8V, 1.2V, 1.8V, 2.5V, 3.3V)



I_{LOAD} = 20 mA

C_{OUT} = 2 x 22 µF

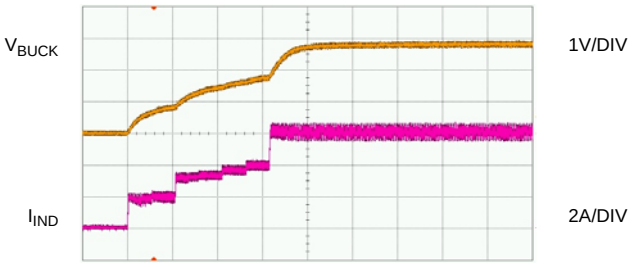
Figure 6: Soft Startup



V_{OUT} = 3.3V

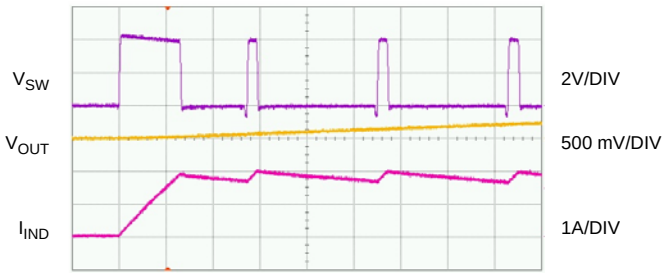
I_{LOAD} = 1.1Ω

Figure 7: Inductor Current Steps at Startup



I_{LOAD} = Heavy Load

Figure 8: First Switching Cycle

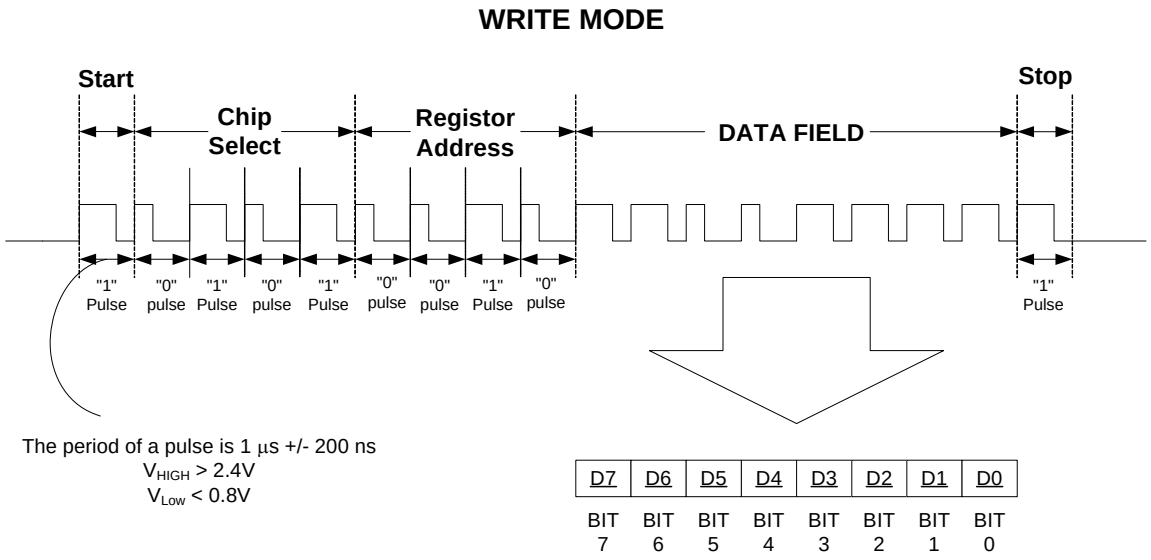


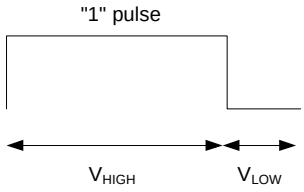
3.2 Output Voltage Setting

3.2.1 Serial Programmability

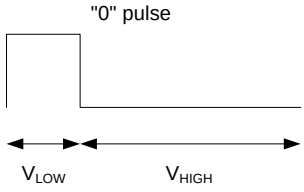
The output voltage of the step-down switching regulator can also program by using 18-bit serial data into the SDI pin.

Figure 9: Serial Programmability





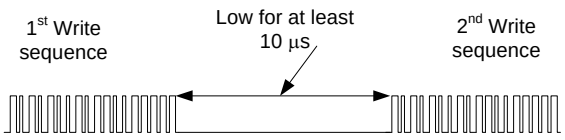
For "1" pulse, the high is 0.75 μs +/- 150 ns and the low period is 0.25 μs+/-50 ns



For "0" pulse, the high is 0.25 μs +/- 50 ns and the low period is 0.75 μs+/-150 ns

The write operation:

1) Each write sequence needs 18 pulses to complete.
2) During a non-write operation, the input needs to be at V_{LOW} (<0.8V).
3) In between two successive write operations, the SDI input needs to be at V_{LOW} (<0.8V) for a minimum of 10 μs



The first 4 bits (MSB-bits) of the data field are used to select the output voltage where the second 4 bits (LSB-bits) of the data field are used to trim the output voltage (percent of output voltage). The default value for the data field is as follows:

Table 4: Default Value of Data Field

	Data Field							
Description	Voltage Set				Percent Set			
Bits	7	6	5	4	3	2	1	0
Default Value	0	0	1	0	0	1	0	0

On power up, the output voltage is set according to VPSET and VVSET. The output voltage can then be field programmed by setting bit 3 and bit 7 to “1”. The output voltage and percent set are selected according to Table 5.

Table 5: Voltage and Percentage Set

	Data Field				V_{OUT} (V)	Data Field				Percent Set
Bits	7	6	5	4		3	2	1	0	
Value	1	0	0	0	0.8	1	0	0	0	-10%
	1	0	0	1	1.0	1	0	0	1	-7.5%
	1	0	1	0	1.2	1	0	1	0	-5.0%
	1	0	1	1	1.5	1	0	1	1	-2.5%
	1	1	0	0	1.8	1	1	0	0	+2.5%
	1	1	0	1	2.5	1	1	0	1	+5.0%
	1	1	1	0	3.0	1	1	1	0	+7.5%
	1	1	1	1	3.3	1	1	1	1	+10%

All combinations of the VSET (Table 7) can be used with all combinations of the PSET (Table 7) to provide maximum flexibility in output voltage selection (Table 5).

3.2.2 Logic Programmability

The output voltage of the step-down switching regulator can be programmed by connecting VSET and PSET pins to SGND and/or SVIN. This can be very useful for standard output voltages. This method will eliminate the use of an external resistor to set the output voltage.

Table 6: Output Voltage Setting

V_{VSET}	V_{PSET}	V_{OUT}
SGND	SGND	0.8V
SGND	SVIN	1.0V
SVIN	SGND	1.2V
SVIN	SVIN	1.5V
SGND	11 kΩ ≤ R_{PSET} ≤ 475 kΩ	Hi-Z

3.2.3 Output Voltage – AnyVoltage™ Technology

The output voltage of the step-down switching regulator is programmed by using Table 7 or Table 8 to select resistor values for VSET and PSET pin. The VSET pin sets the output voltage and the PSET pin trims the set voltage to a percentage value. For example, to program 2.25V output, a 165 kΩ resistor is selected for the VSET pin, and an 11 kΩ resistor is selected for the PSET pin. The 165 kΩ resistor sets the output voltage to 2.5V and the 11 kΩ resistor trims the set voltage by -10%.

Using the VSET resistor's value greater than 619 kΩ or less than 7.68 kΩ disables the step-down switching regulator and sets the SW pin to high impedance. If the VSET resistor's value is outside the 5% tolerance, the output can be either higher or lower than the set voltage.

Using resistor values greater than 619 kΩ or less than 7.68 kΩ for the PSET pin does not affect the set voltage. When the PSET pin is not used, it must be connected to ground. Like the VSET resistor, the percent value can be either higher or lower if the PSET resistor's value is outside the 5% tolerance.

Table 7: Any Voltage Programming Table for 1% Resistors

		PSET								
		-10.0%	**–7.5%**	**–5.0%**	**–2.5%**	**0%**	**2.5%**	**5.0%**	**7.5%**	**10.0%**
		11k	**18.7k**	**31.6k**	**53.6k**	**GND**	**97.6k**	**165k**	**280k**	**475k**
VSET	**11k**	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
	18.7k	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
	31.6k	1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
	53.6k	1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
	97.6k	1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
	165k	2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
	280k	2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
	475k	2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630

Table 8: Any Voltage Programming Table for 5% Resistors

		PSET								
		-10.0%	–7.5%	–5.0%	–2.5%	0%	2.5%	5.0%	7.5%	10.0%
		11k	18k	30k	51k	GND	100k	160k	270k	470k
VSET	11k	0.720	0.740	0.760	0.780	0.800	0.820	0.840	0.860	0.880
	18k	0.900	0.925	0.950	0.975	1.000	1.025	1.050	1.075	1.100
	30k	1.080	1.110	1.140	1.170	1.200	1.230	1.260	1.290	1.320
	51k	1.350	1.388	1.425	1.463	1.500	1.538	1.575	1.613	1.650
	100k	1.620	1.665	1.710	1.755	1.800	1.845	1.890	1.935	1.980
	160k	2.250	2.313	2.375	2.438	2.500	2.563	2.625	2.688	2.750
	270k	2.700	2.775	2.850	2.925	3.000	3.075	3.150	3.225	3.300
	470k	2.970	3.053	3.135	3.218	3.300	3.383	3.465	3.548	3.630

The VSET and PSET resistors are read once during start-up before the output voltage is turned on. After the output voltage is turned on, the output voltage can change to different values using serial programming interface. Otherwise to configure the output to a different voltage, power has to recycle or the 88PG8x7 has to turn OFF and back ON using the shutdown pin.

Figure 10 shows the startup waveforms of the 88PG8x7. Once the input voltage (V_{IN}) is above the under voltage lockout (UVLO) upper threshold (UTH), the VSET and PSET pin become active. Current is first sourced out of PSET pin and then the VSET pin, in exponentially increasing steps. After each step there is a blanking time before the VSET voltage is compared to an internal 1.2V reference. If the VSET voltage is below internal reference voltage, the current source proceeds to the next step. Once the VSET voltage is above the internal reference voltage the sequence stops and the output voltage (VOUT) is allowed to turn on. The Figure 11 shows the VSET waveform for VSET = 2.5V and PSET = –5% output. The 88PG8x7 keeps track of how many steps are required to determine the appropriate output voltage. Table 9 provides the number of steps necessary for each output voltage option. Using a VSET resistor of 165 kΩ requires the current source to step 4 times, and a PSET resistor of 31.6 kΩ requires 7 steps.

Figure 10: Startup Sequence

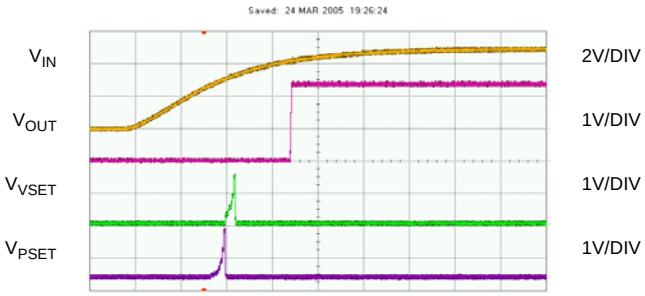


Figure 11: Soft Startup

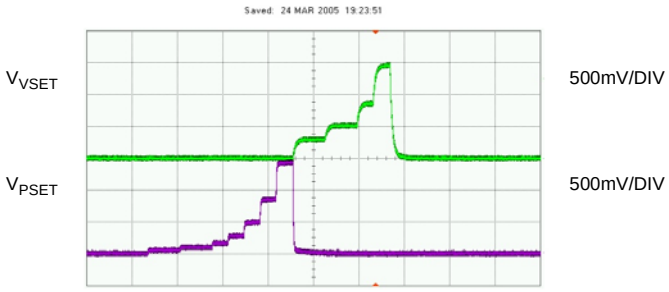


Table 9: Output Voltage Option Steps

Step	VOUT (V)	R_{VSET} (kΩ)
1	0	0
2	3.3	475
3	3.0	280
4	2.5	165
5	1.8	97.6
6	1.5	53.6
7	1.2	31.6
8	1.0	18.7
9	0.8	11

Step	PSET (%)	R_{PSET} (kΩ)
1	0	0
2	+10	475
3	+7.5	280
4	+5.0	165
5	+2.5	97.6
6	-2.5	53.6
7	-5.0	31.6
8	-7.5	18.7
9	-10	11

The 88PG8x7 provides an innovative technique to set the output voltage. During start-up it reads the value of external resistors, which are located outside the regulator's feedback loop to program the output voltage. By placing the output voltage programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. Normally, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. Whereas, the 88PG8x7 initial accuracy is 2% for any of the eight output voltages.

The VSET and PSET pins are sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination, which introduces excessive leakage current on the VSET and PSET pin, especially for the 3.3V output or +10%. The parasitic resistance on these nodes must be greater than 3 MΩ and the stray capacitance must be less than 25 pF; otherwise, a 3.3V output can potentially end up at 3V.

3.3 Programmable Current Limit for the LDO Regulator Controller

A sense resistor is placed between SVIN and ILIM pin to program the current limit of the LDO regulator controller. The following equation is used to determine the value of the sense resistor.

$$I_{LIM} = \frac{50mV(Typical)}{R_{SENSE}(m\Omega)}$$

When the LDO regulator controller is in current limit, the internal current-limit circuitry turns off the LDO regulator controller and holds the LDO regulator controller in the off state for 1ms (typical hold time). After the hold-time is expired, the LDO regulator controller is enabled. The current-limit circuitry continues to disable and enable the regulator until the current limit is removed.

The LDO regulator P-channel MOSFET can be selected from the following list based on the required threshold voltage of either -2.5V or -1.8V and a gate capacitance of less than 1000 pF.

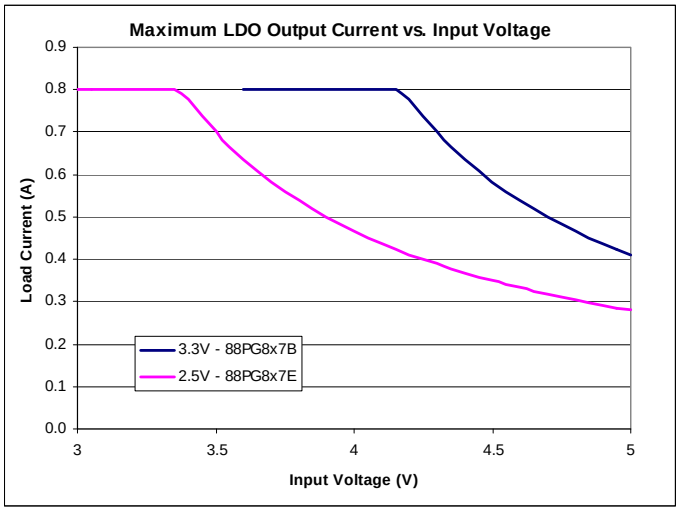
Table 10: P-Channel MOSFET Selection

Package	Vishay	Fairchild
Super SOT-6		FDC642P FDC634P
Super SOT-3 / micro 3		FDN340P FDN302P
SO-8	Si4433DY	FDS9431A
SC75-6 FLMP		FDJ127P
TO-263AB (D2-Pack)		FDP4020P
TSOP-6	Si3443DV	
SC70-6		FDG330P
SOT-23	Si2333DS	
1206-8 Chip FET	Si5473DC	
SC-89 (6-lead)	Si1039X	
SC75A/SC-89 (3-lead)	Si1012R/X	

3.3.1 Maximum LDO Output Current

The FDS642P is design to provide up to 800 mA of continuous output current. However, the tiny Super SOT-6 package can dissipate up to 0.7W. If the input and output voltage are close, then the full 800 mA is achieved, see Figure 12. As the input voltage increases, the IC dissipates more power, limiting the maximum output current. The output current has to decrease in order to keep the power dissipation under its 0.7W limit.

Figure 12: Maximum Output Current for the FDS642P P-Channel MOSFET



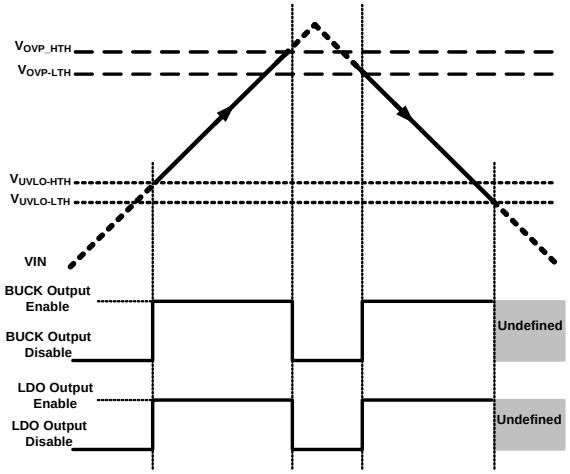
3.4 Undervoltage Lockout (UVLO)

At start-up, the 88PG8x7 incorporates undervoltage-lockout circuitry to enable the step-down switching regulator and the LDO controller when the input voltage is above 2.65V (typical). After the 88PG8x7 is enabled and the input voltage is lowered, the highest value of the minimum input voltage for both regulators to remain enabled is 2.55V (typical).

3.5 Over Voltage Protection (OVP)

The 88PG8x7 incorporates an over voltage protection circuitry to disable the step-down switching regulator and LDO controller when the input voltage is above 5.7V (typical). The step-down switching regulator and LDO controller are enabled when the input voltage is below 5.6V (typical).

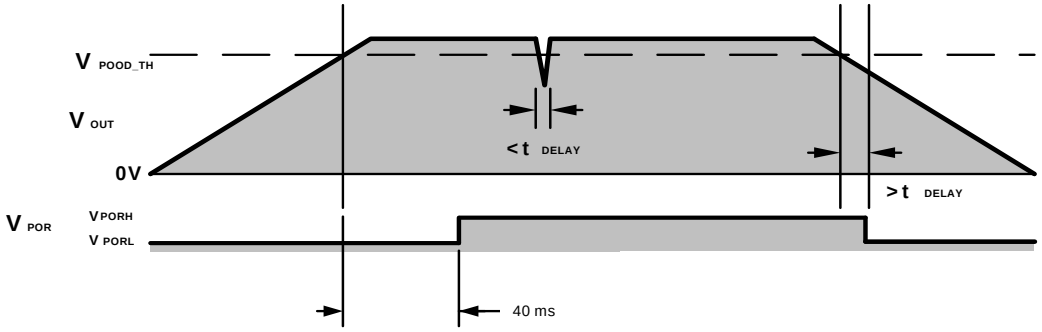
Figure 13: UVLO and OVP Waveforms



3.6 Power-On Reset (POR)

The Power-On Reset (POR) pin is an active-high, open-drain output pin. This output is held low when the output voltage of the step-down regulator is below the threshold. When the output voltage is above the threshold, the Power-On Reset pin goes high 40 ms later. Setting the output voltage greater than 1.35V, the threshold voltage is 0.9% * $V_{OUT\ (typical)}$. Setting the output voltage less than 1.32V, the threshold voltage is V_{OUT} – 130 mV (typical). A built-in 25 µs (t_{DELAY}) delay is incorporated to prevent nuisance tripping.

Figure 14: Power-On Reset Waveforms



3.7 Thermal Shutdown

When the junction temperature of the 88PG8x7 exceeds 150 °C (typical), the thermal shutdown circuitry disables the step-down regulator. The step-down switching regulator is enabled when the junction temperature is decreased to 105 °C (typical).

3.8 Adaptive Transient Response

The 88PG8x7 device's Smart Technology allows the step-down switching regulator to quickly respond to the multiple step loads and maintain stability over a wide range of applications. Figure 15 shows an example of a second step-load applied while the output voltage of the step-down switching regulator increased due to the inductive kick from the first step-load.

Condition: V_{IN} = 5.0V, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 10 µF, L = 1.3 µH, C_{OUT} = 2 x 22 µF, V_{OUT} = 1.2V, I_{LOAD} = 1A to 3A.

Figure 15: Adaptive Transient Response

The worst case overshoot (V_{SOAR}) during a full-load to light-load transient due to stored inductor energy (Figure 15) can be calculated as:

$$V_{SOAR} = \frac{\Delta I_{LOAD(MAX)}^{2} \times L}{2 \times C_{OUT} \times V_{OUT}}$$

Although the V_{SOAR} cannot be eliminated, its amplitude can be controlled based on the C_{OUT} capacitor value. The appropriate C_{OUT} value can easily be calculated for the acceptable V_{SOAR} level for each specific application.

$$C_{OUT} = \frac{\Delta I_{LOAD(MAX)}^{2} \times L}{2 \times V_{SOAR} \times V_{OUT}}$$

3.9 Using Ceramic Input Capacitors

Ceramic capacitors' low ESR, small case size and high ripple current ratings make them ideal for switching regulator applications. However, Tantalum or electrolytic capacitors must be placed in parallel with the ceramic capacitors in "Hot-Plug" application such as when using an AC-DC wall adaptor. If a wall adaptor is "Hot-Plugged" into the input supply, high transient current runs through the adaptor's long wires and produce ringing at the input (V_{IN}) of the 88PG8x7, see Figure 16. During this period, the 88PG8x7 is still "OFF" and the current I_{IN} is used to charge the input capacitor. At worst, these voltage spikes can be as high as twice the input voltage. To dampen the ringing, a small 47 µF to 100 µF Tantalum capacitor with an ESR in the range of 0.2 ohm to 1.0 ohm must be added, as shown in Figure 17.

Figure 16: Inrush with 22 µF Ceramic

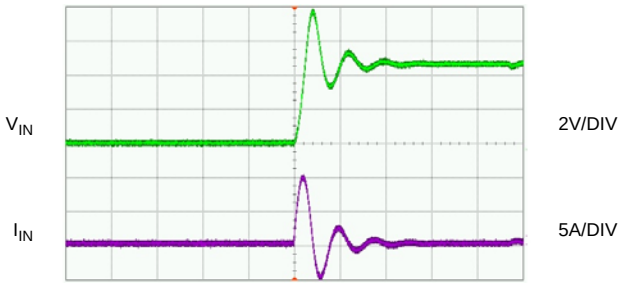
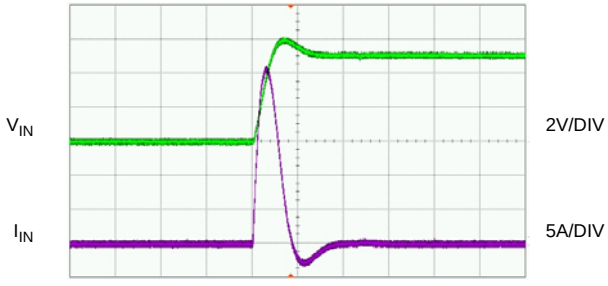


Figure 17: Inrush with 22 µF Ceramic + 100 µF TA



Ceramic input capacitor must not be replaced with any other type of capacitor and choose only X5R or X7R dielectric. These have the best voltage and temperature characteristics. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor in placed next to the IC. If Tantalum input capacitor is used, it must be rated for switching regulator applications and the operating voltage be derated by 50%.

3.10 Sequential Power up

Figure 18 shows a detailed start-up sequence waveforms of two 88PG847 devices cascaded together as shown in Figure 19. When the input voltage is above the under-voltage-lockout upper threshold (UVLO UTH) of 2.65V, the LDO output (V_{OUT1}) starts a slow ramp up and finishes in about 3 ms. Roughly, 3 ms after the input voltage is above the UVLO UTH the 2.5V (V_{OUT2}) output ramps up. The power-on-reset (POR) signal goes high 45 ms after V_{OUT1} and V_{OUT2} outputs are regulating. The POR signal enables U2 and the 1.5V output (V_{OUT3}) ramps up 3 ms later.

Figure 18: Start-Up Waveforms of two 88PG847 devices

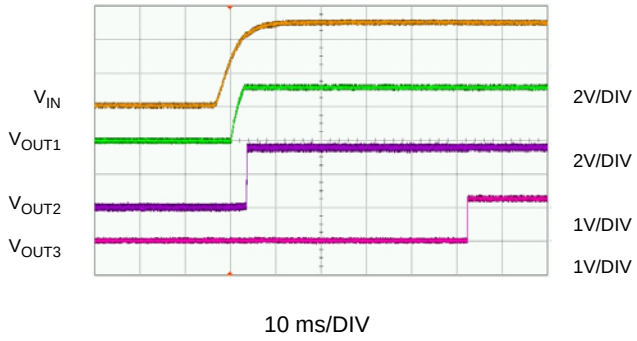
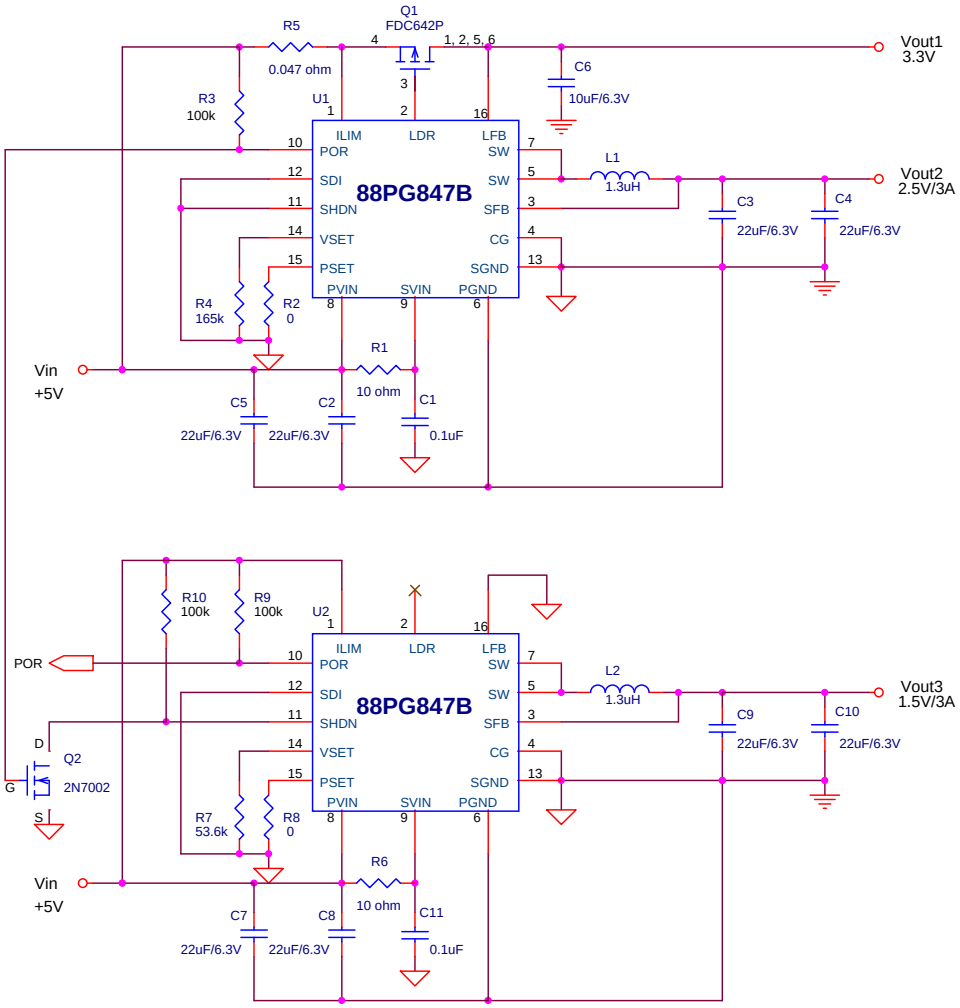


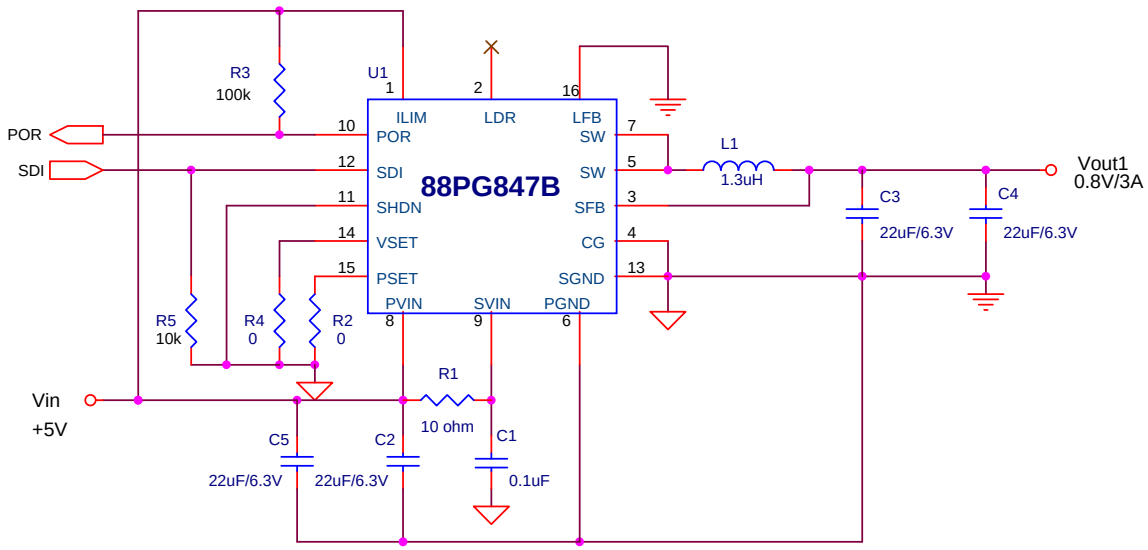
Figure 19: Power Sequence of Two 88PG8x7 devices



3.11 Disable the LDO Function

The LDO function can be disabled by connecting the ILIM pin to SVIN pin, and the LFB pin to ground. Also, the LDR pin is left floating, see Figure 20. Disabling the LDO function will lower the no-load supply current from 1.9 mA to 1.2 mA.

Figure 20: 88PG847B device without LDO Output



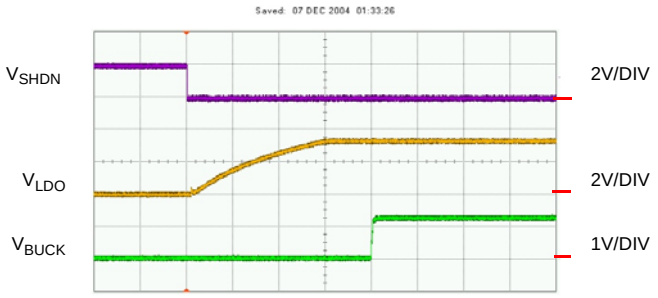
Section 4. Functional Characteristics

The following applies unless otherwise noted: T_A = 25°C, R_{SVIN} = 10Ω, C_{SVIN} = 0.1 µF, C_{PVIN} = 2 x 22 µF, L = 1.3 µH, $C_{OUT\ (BUCK)}$ = 2 X 22 µF, PFET = FDC642P, C_{OUT} (LDO) = 10 µF.

4.1 Start-up Waveforms

NOTE: When the input voltage rises above the UVLO's upper threshold, then there is a delay (4 ms typ) before the step-down regulator's output voltage turns on.

Figure 21: Startup Using the Shut-down Pin



1 ms/DIV

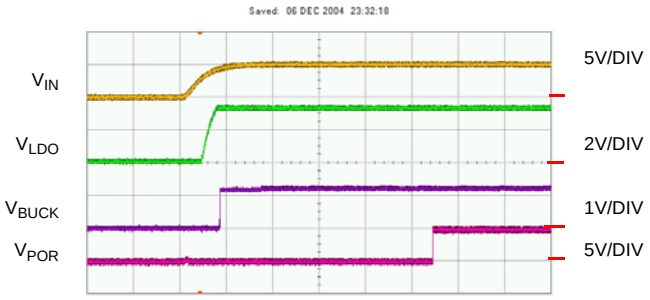
V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V
I_{LOAD} = No Load
t_{DLY}~ 4.0 ms

Figure 22: Turn Off Using the Shut-down Pin

1 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V
I_{LOAD} = No Load

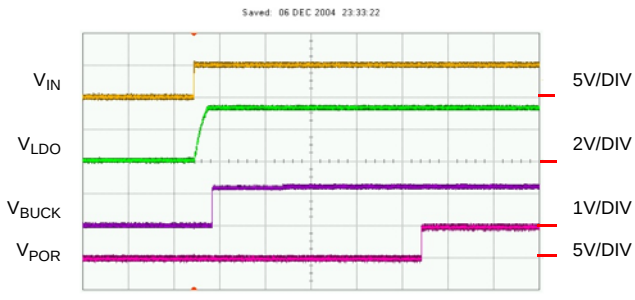
Figure 23: Startup Sequence



10 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V
I_{LOAD} = No Load

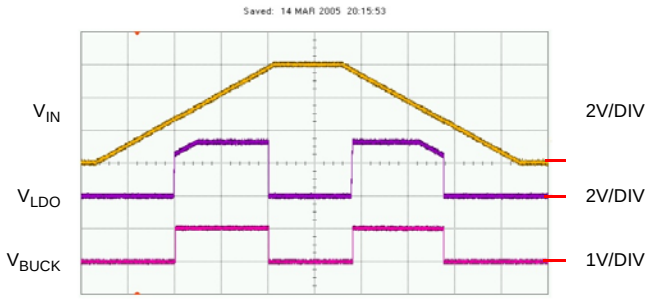
Figure 24: Soft Startup



10 ms/DIV

V_{IN} = 5.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.2V
I_{LOAD} = No Load

Figure 25: UVLO and OVP Thresholds



V_{IN} = 0 to 6.0V
V_{LDO}= 3.3V
V_{BUCK}= 1.0V
$I_{LOAD(BUCK)}$ = 1A
$I_{LOAD(BUCK)}$ = 500 mA
$V_{UVLO(HTH)}$ = 2.65V
$V_{UVLO(LTH)}$= 2.55V
$V_{OVP(HTH)}$ = 5.8V
$V_{OVP(LTH)}$ = 5.7V

4.2 Short-Circuit Waveforms

Figure 26: Step-Down Short-Circuit Response

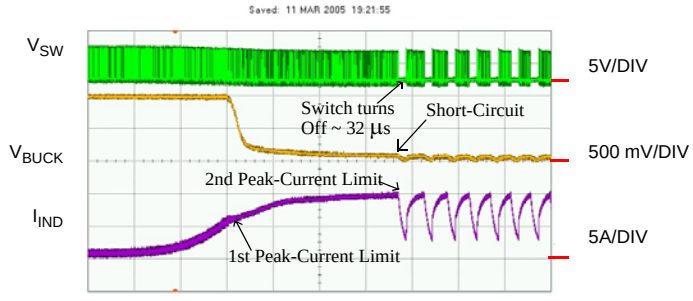
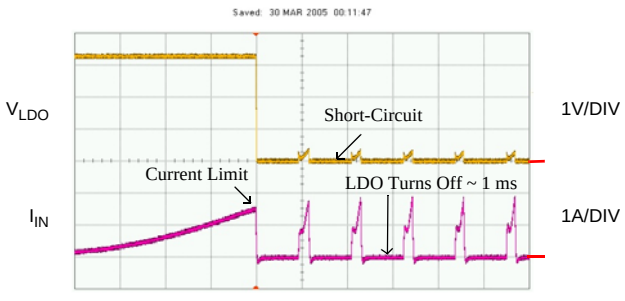


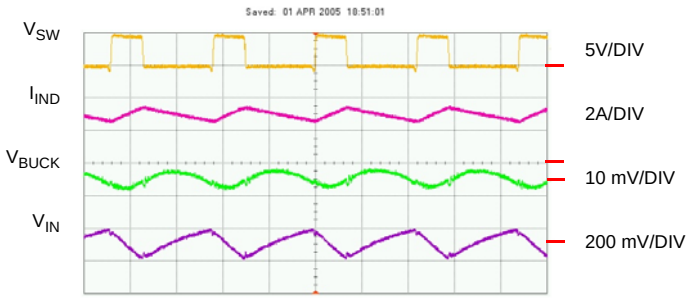
Figure 27: LDO Short-Circuit Response



4.3 Switching Waveforms

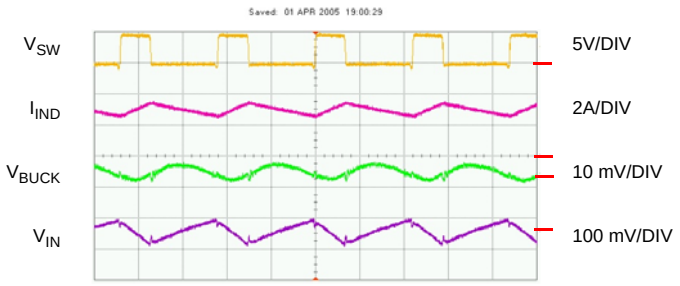
NOTE: For repeatability of measuring output ripple ($V_{BUCK\ (P-P)}$) for the BUCK regulator, the standard test procedure limits the scope bandwidth to 20 MHz and uses a coax cable with very short leads terminated into 50Ω. The coax leads must be routed away from the switching node as much as possible.

Figure 28: Switching Waveforms - PWM mode



C_{IN} = 22 µF
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 3.0A
$V_{OUT(P-P)}$ = 6.7 mV (Note)
$V_{IN(P-P)}$ = 190 mV
$I_{IND(P-P)}$ = 1.05A
$I_{IND(PK)}$ = 3.4A
Freq = 912 kHz

Figure 29: Switching Waveforms - PWM mode

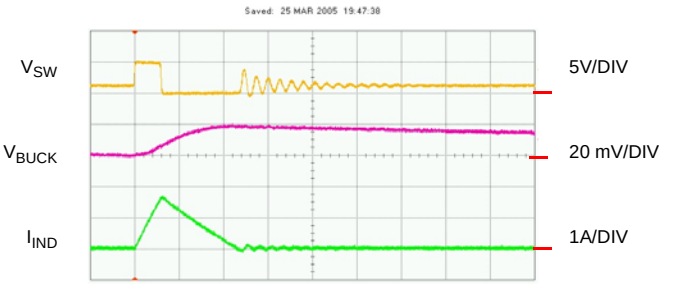


C_{IN} = 2 x 22 µF
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 3.0A
$V_{OUT(P-P)}$ = 6.7 mV (Note)
$V_{IN(P-P)}$ = 89 mV
$I_{IND(P-P)}$ = 1.05A
$I_{IND(PK)}$ = 3.4A
Freq = 912 kHz

Figure 30: Switching Waveforms - DCM Mode

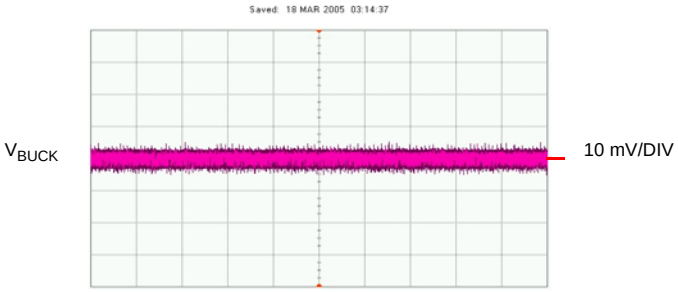
V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 24 mA
$V_{OUT(P-P)}$ =22 mV (Note)
$I_{IND(PK)}$ = 920 mA
Freq = 53 kHz

Figure 31: Switching Waveforms - DCM Mode-Zoom



V_{IN} = 5.0V
V_{BUCK}= 1.2V
I_{OUT} = 24 mA
Ringing Freq = 7.5 MHz

Figure 32: PWM Output Ripple Voltage



V_{IN} = 5.0V

V_{BUCK}= 1.2V

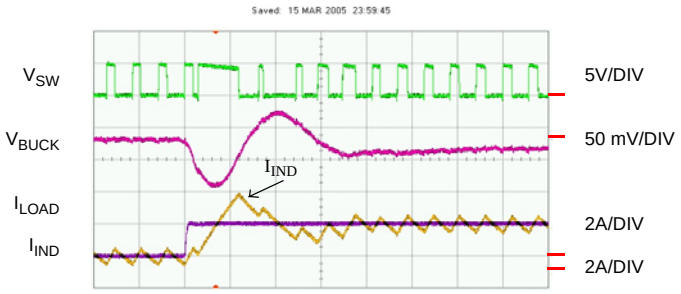
I_{OUT} = 3.0A

$V_{OUT(P-P)}$ = 21 mV (Note)

4.4 Load Transient Waveforms

4.4.1 Step-Down Regulator

Figure 33: Fast Load Rise Time



2 µs/DIV

V_{IN} = 5.0V

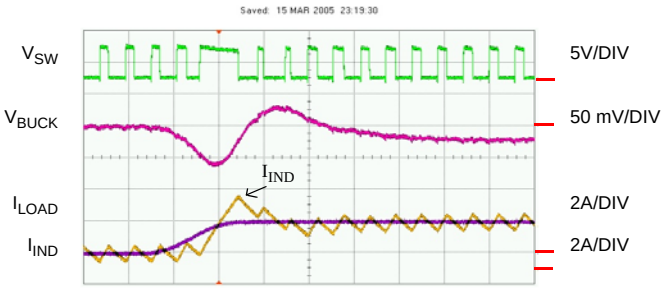
V_{BUCK}= 1.2V

I_{OUT} = 1 A to 3A

C_{OUT} = **2 x 22 µF**

t_{RISE} = 12 A/µs

Figure 34: Slow Load Rise Time



2 µs/DIV

V_{IN} = 5.0V

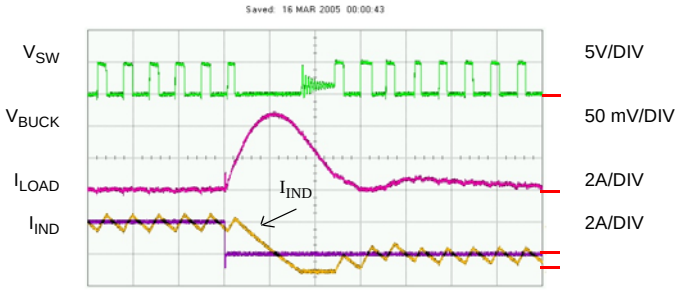
V_{BUCK}= 1.2V

I_{OUT} = 1 A to 3A

C_{OUT} = **2 x 22 µF**

t_{RISE} = 1 A/µs

Figure 35: Fast Load Fall Time



2 µs/DIV

V_{IN} = 5.0V

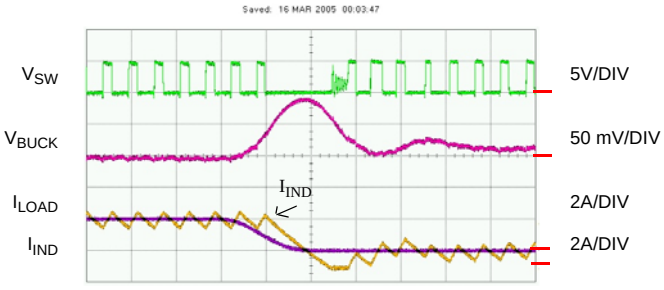
V_{BUCK}= 1.2V

I_{OUT} = 1 A to 3A

C_{OUT} = **2 x 22 µF**

t_{FALL} = 122 A/µs

Figure 36: Slow Load Fall Time



2 µs/DIV

V_{IN} = 5.0V

V_{BUCK}= 1.2V

I_{OUT} = 1 A to 3A

C_{OUT} = **2 x 22 µF**

t_{FALL} = 1 A/µs

Figure 37: Load Transient Response

20 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 2 x 22 µF
V_{CG} = GND

I_{LOAD} = 1A to 3A
t_{RISE} = 12 A/µs
t_{FALL} = 122 A/µs

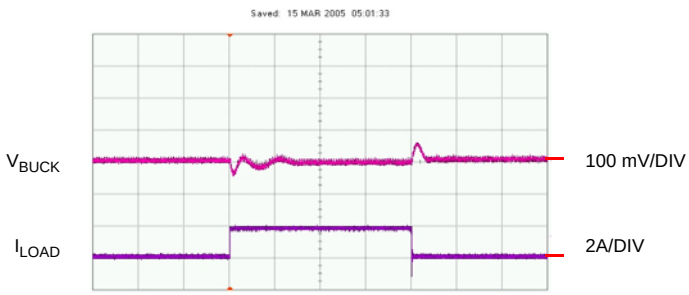
Figure 38: Double-Pulsed Load Response

20 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 2 x 22 µF
V_{CG} = GND

I_{LOAD} = 1A to 3A
t_{RISE} = 12 A/µs
t_{FALL} = 122 A/µs

Figure 39: Load Transient Response



20 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 4 x 22 µF
V_{CG} = GND

I_{LOAD} = 1A to 3A
t_{RISE} = 12 A/µs
t_{FALL} = 122 A/µs

Figure 40: Double-Pulsed Load Response

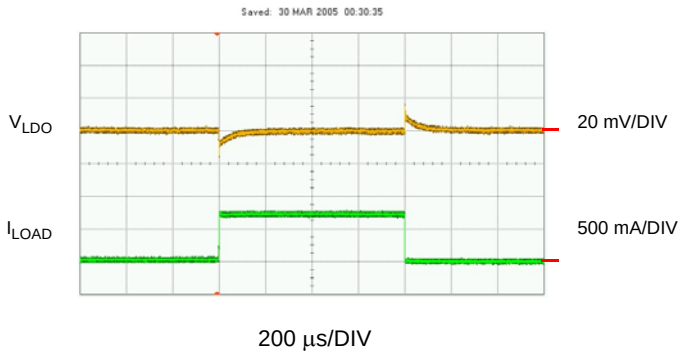
20 µs/DIV

V_{IN} = 5.0V
V_{BUCK}= 1.2V
C_{OUT} = 4 x 22 µF
V_{CG} = GND

I_{LOAD} = 1A to 3A
t_{RISE} = 12 A/µs
t_{FALL} = 122 A/µs

4.4.2 LDO Regulator

Figure 41: Load Transient Response



V_{IN} = 5.0V

V_{LDO}= 3.3V

C_{OUT} = 10 µF

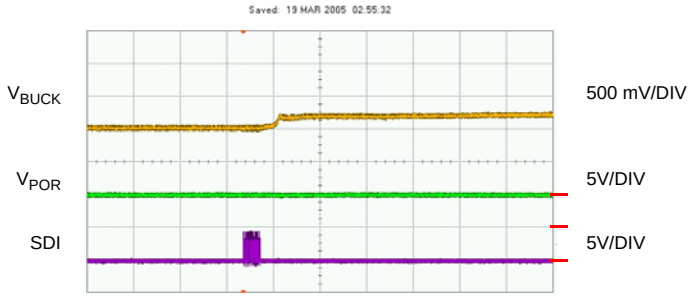
I_{LOAD} = 100 mA to 800 mA

4.5 Output Voltage Transient Waveforms

The following graphs show the effect of changing the step-down regulator's output voltage using the serial interface. Depending on the change in the step-size of the output voltage, the output load, and the output capacitance, the power-on reset pin de-asserts when the changes of the output voltage occur beyond the 25 µs (typical) delay.

4.5.1 Step-Down Regulator

Figure 42: V_{OUT} = 1.0V to 1.2V with No Load

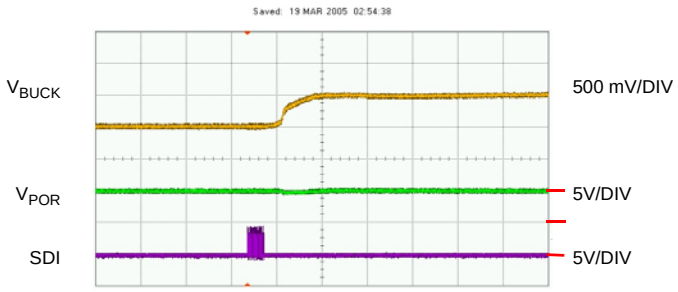


10 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) + 1000 µF

Figure 43: V_{OUT} = 1.0V to 1.5V with No Load

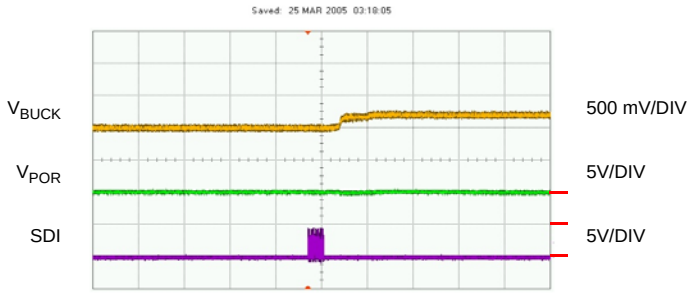


50 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) +1000 µF

Figure 44: V_{OUT} = 1.0V to 1.2V with I_{LOAD} = 3A

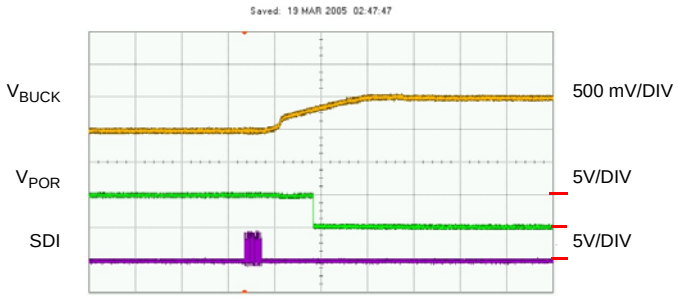


50 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) + 1000 µF

Figure 45: V_{OUT} = 1.0V to 1.2V with I_{LOAD} = 3A

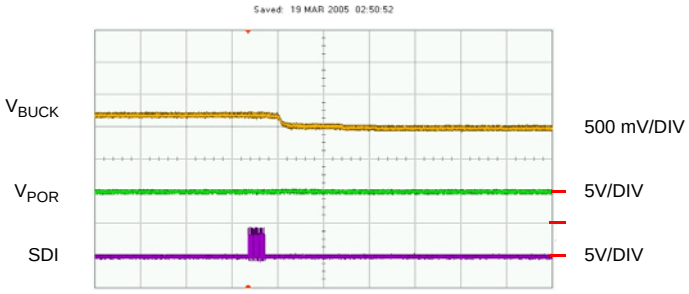


50 µs/DIV

V_{IN} = 5.0V

C_{OUT}= (2 x 22) +1000 µF

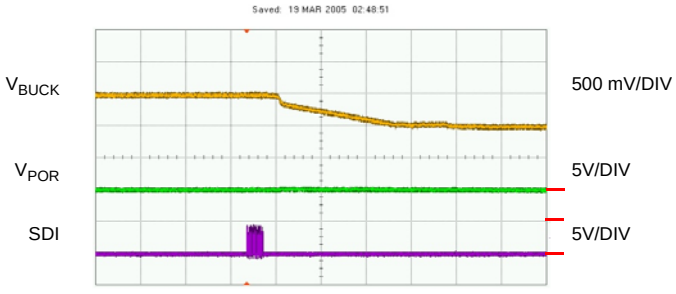
Figure 46: V_{OUT} = 1.2V to 1.0V with I_{LOAD} = 3A



V_{IN} = 5.0V

C_{OUT}= (2 x 22)+1000 µF

Figure 47: V_{OUT} = 1.5V to 1.0V with I_{LOAD} = 3A

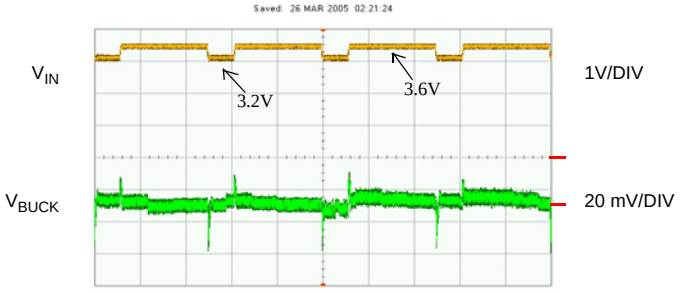


V_{IN} = 5.0V

C_{OUT}= (2 x 22)+1000 µF

4.6 Line Transient Waveforms

Figure 48: Line Transient @ V_{IN} = 3.6



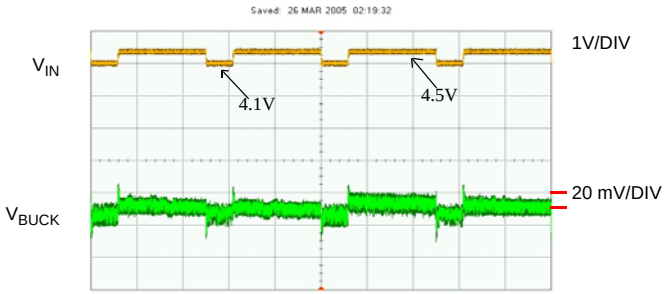
V_{IN} = 3.6V

C_{IN}= 22 µF

V_{BUCK} = 1.2V

I_{LOAD} = 3A

Figure 49: Line Transient @ V_{IN} = 4.5



V_{IN} = 4.5V

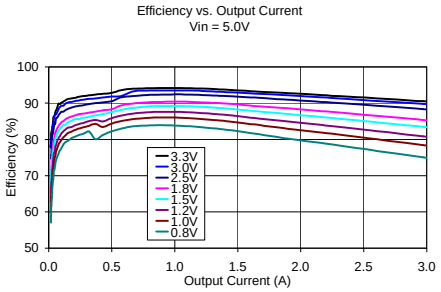
C_{IN}= 22 µF

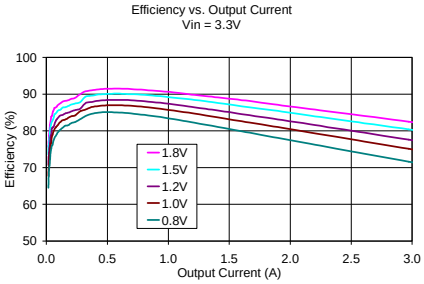
V_{BUCK} = 1.2V

I_{LOAD} = 3A

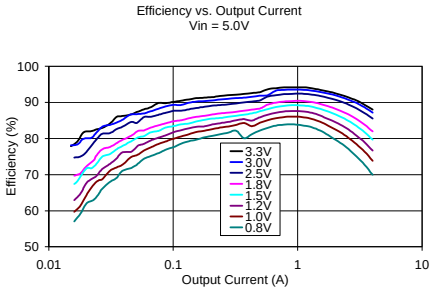
Section 5. Typical Characteristics

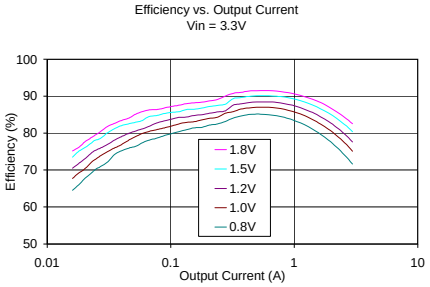
5.1 Efficiency Graphs



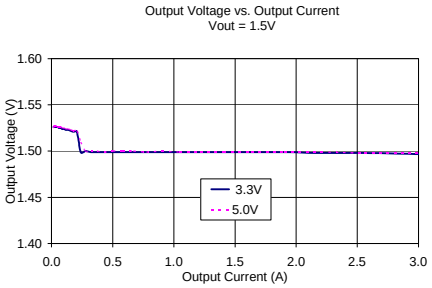


5.1.1 Efficiency Graphs in log scale

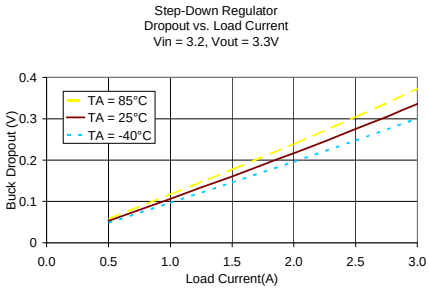


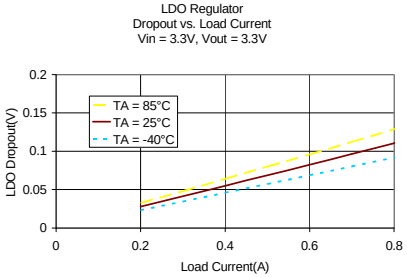


5.2 Load Regulation

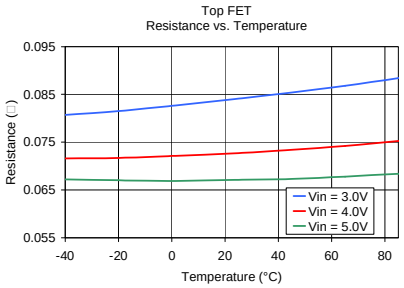


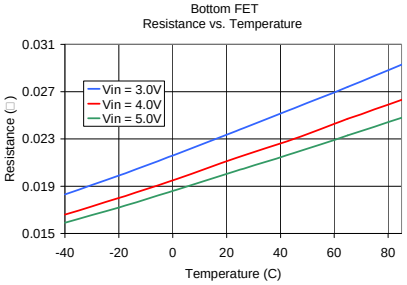
5.3 Dropout Voltage

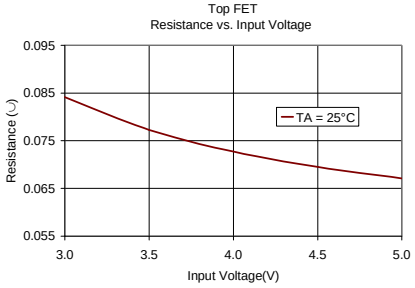


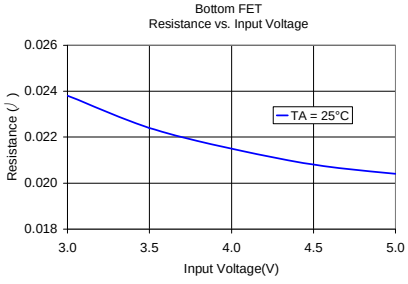


5.4 RDS (ON) Resistance



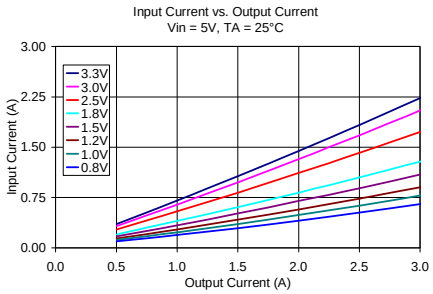


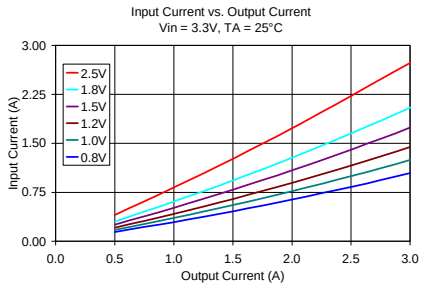


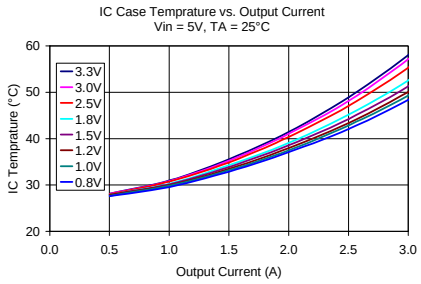


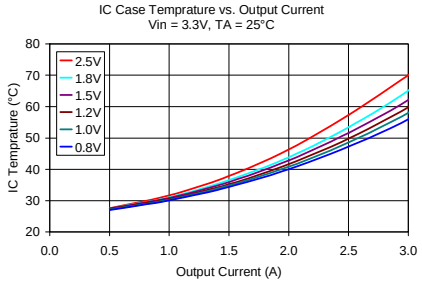
5.5 IC Case and Inductor Temperature

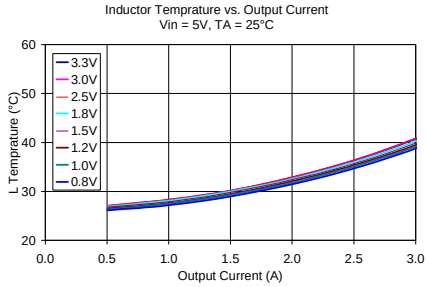
The following data was taken using a 1.4 square inch PCB 1 oz. copper and L = 1.3 µH. Actual results depend upon the size of the PCB proximity to other heat emitting components.

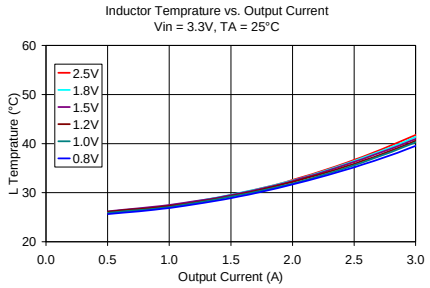






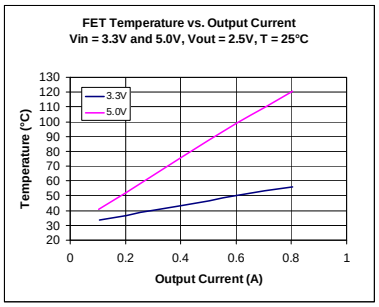


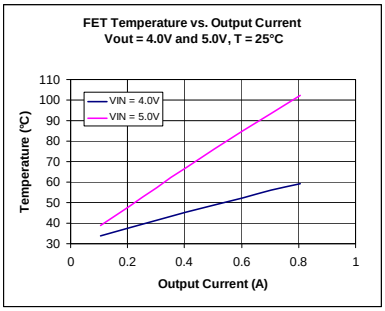


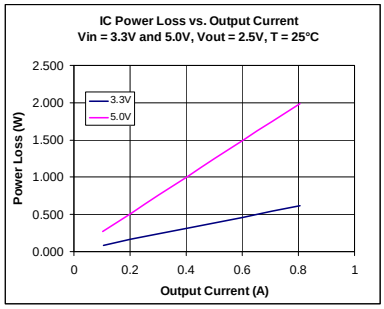


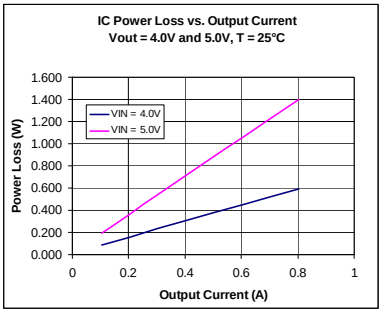
5.6 P-Channel MOSFET (FDS642P) Thermal Characteristics

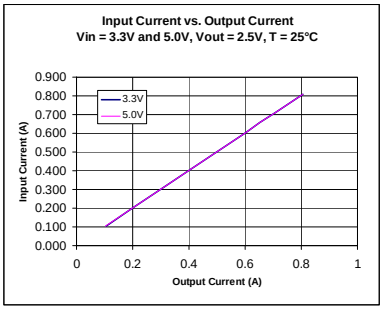
The following data was taken using 1.4 square inch PCB 1 oz. Copper. Actual results depend upon the size of the PCB and proximity to other heat emitting components.

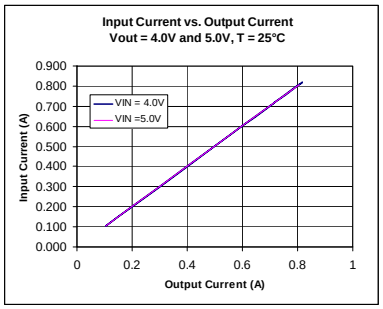




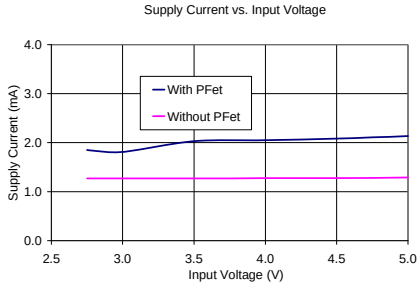




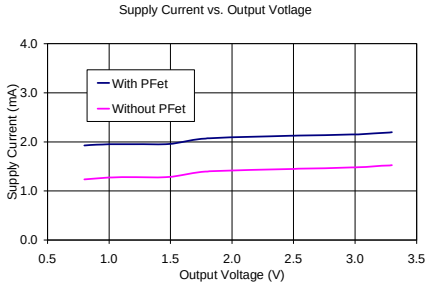




5.7 Input Voltage Graphs

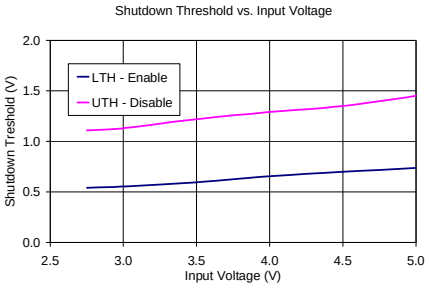


Load = No Load



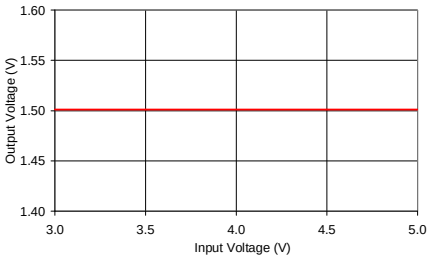
V_{IN} = 5.0V

Load = No Load



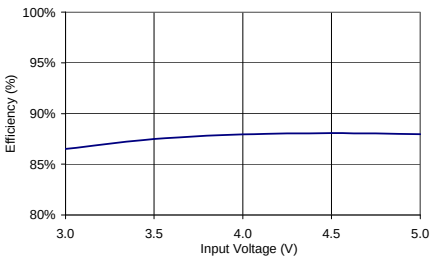
5.7.1 Step-Down Regulator

Output Voltage vs. Input Voltage



$I_{OUT(BUCK)}$ = 750 mA

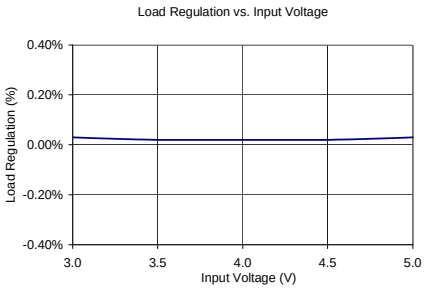
Efficiency vs. Input Voltage



$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 1.5A

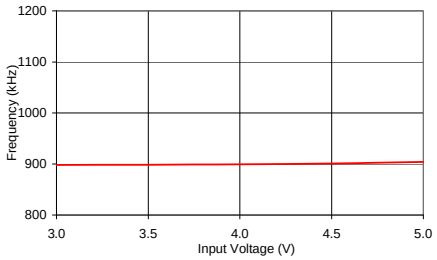
Load Regulation vs. Input Voltage



$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 750 mA

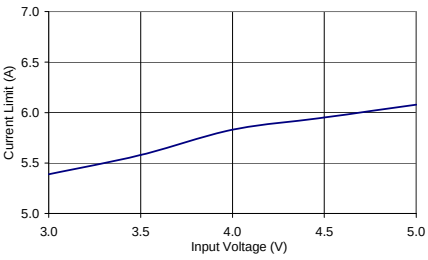
Frequency vs. Input Voltage



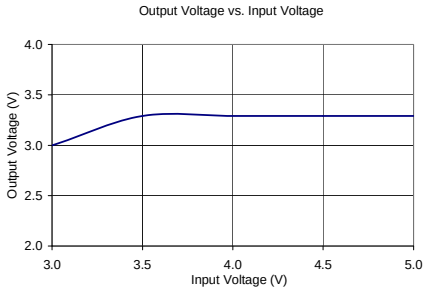
$V_{OUT(BUCK)}$ = 1.5V

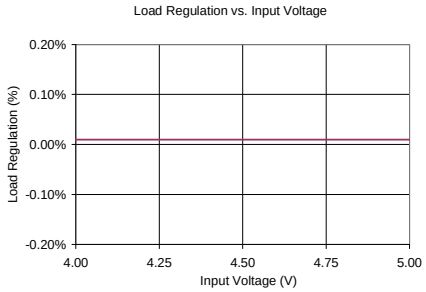
$I_{OUT(BUCK)}$ = 1.5A

Average Output Current Limit vs. Input Voltage



5.7.2 LDO Regulator

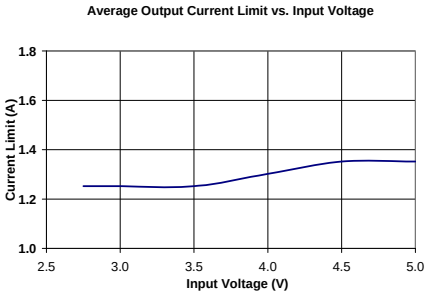




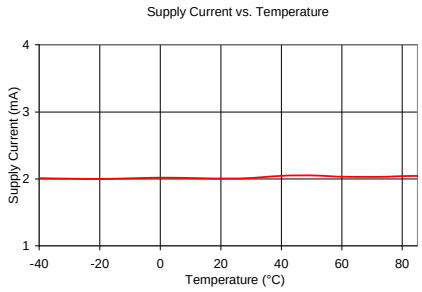
$I_{OUT(LDO)}$ = 10 mA

$V_{OUT(LDO)}$ = 3.3V

$I_{OUT(LDO)}$ = 10 mA - 800 mA

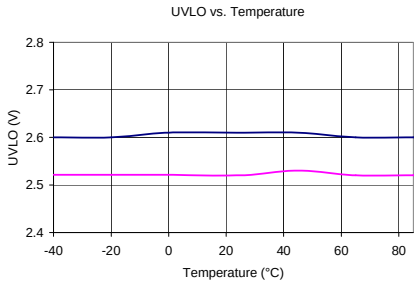


5.8 Temperature Graphs

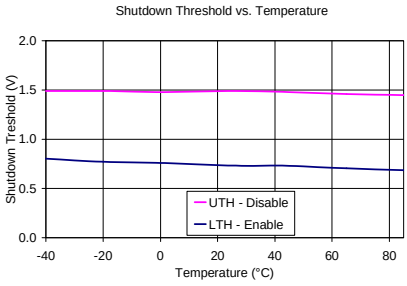


$I_{OUT(BUCK)}$ = No Load

$I_{OUT(LDO)}$ = No Load

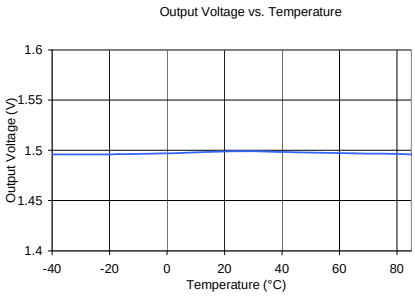


$I_{OUT(BUCK)}$ = 10 mA



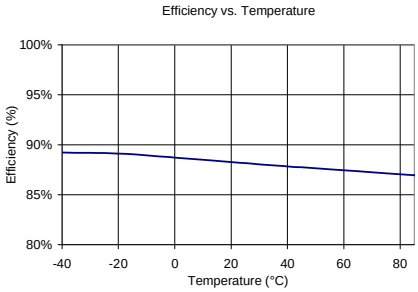
V_{IN}= 5V

5.8.1 Step-Down Regulator



V_{IN} = 5.0V

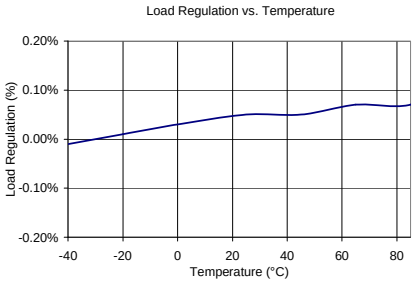
$I_{OUT(LDO)}$ = 750 mA



V_{IN} = 5.0V

$V_{OUT(BUCK)}$ = 1.5V

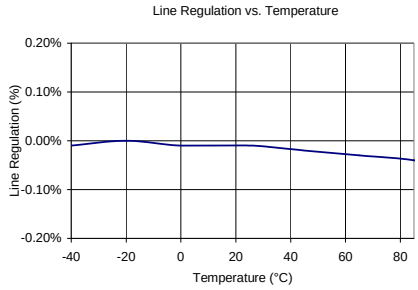
$I_{OUT(BUCK)}$ = 1.5A



V_{IN} = 5.0V

$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 750 mA - 3A

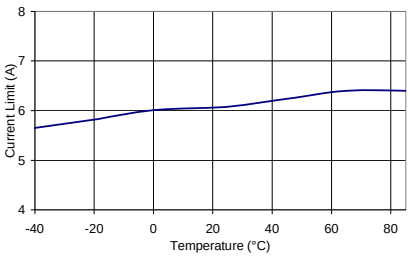


V_{IN} = 3.0V - 5.0V

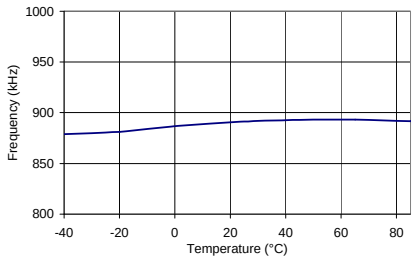
$V_{OUT(BUCK)}$ = 1.5V

$I_{OUT(BUCK)}$ = 1.5A

Average Output Current Limit vs. Temperature



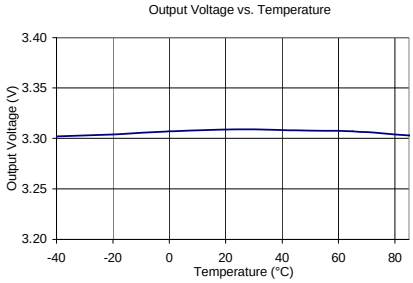
Frequency vs. Temperature



V_{IN} = 5.0V

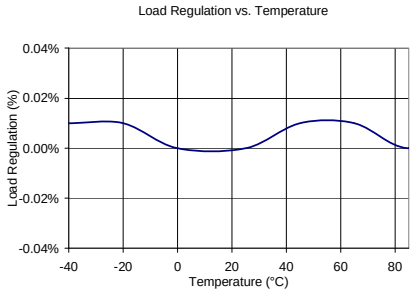
$I_{OUT(BUCK)}$ = 1.5A

5.8.2 LDO Regulator



V_{IN} = 5.0V

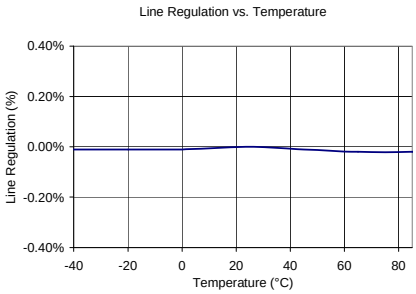
$I_{OUT(LDO)}$ = 10 mA



V_{IN} = 5.0V

$V_{OUT(LDO)}$ = 3.3V

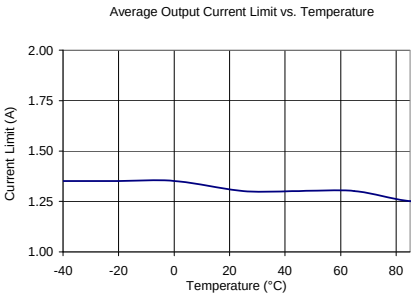
$I_{OUT(LDO)}$ = 10 mA - 800 mA



V_{IN} = 3.5V - 5.0V

$V_{OUT(LDO)}$ = 3.3V

$I_{OUT(LDO)}$ = 10 mA



V_{IN} = 5.0V

Section 6. Applications Information

6.1 PC Board Layout Considerations and Guidelines for 88PG8x7

Warning

If you want to avoid noise and abnormal operating behavior, follow these layout recommendations.

1. This is a 2-layer board with 1 ground plane and 1 routing layer.
2. Copy the routing layer in Figure 52 as much as possible and place it on the top layer. The ground plane in Figure 53 can be placed on any other layer. Use the recommend BOM in Table 11 through Table 16. Contact the factory where substitutions are made.
3. Review the recommended solder pad layout and notes on page 67. Make sure that you place a dot on the top silk screen to indicated the location of pin 1 for the 88PG8x7 and the FDS742P, see Figure 52. Ensure that the dot is outside the package outline. This way you can visually inspect the package orientation after assembly.
4. Do not replace the Ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor in placed next to the IC. If Tantalum input capacitor is used, it must be rated for switching regulator applications and the operating voltage be derated by 50%.
5. Use either X7R or X5R type ceramic capacitors. If Y5V or Z5U type capacitor are used, then you must double the recommended capacitance value.
6. Any type of capacitor can be placed in parallel with the output capacitor.
7. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that the Ceramic capacitors provide the lowest noise and smallest foot print solution.
8. Use planes for the ground, input and outputs power to maintain good voltage filtering and to keep power losses low.
9. If there is not enough space for a power plane for the input supply, then the input supply trace must be at least 3/8 inch wide.
10. If there is not enough space for a power plane for the output supplies, then place the output as close to the load as possible with a trace of at least 3/8 inch wide.
11. Do not lay out the inductor first. The input capacitor placement is the most critical for proper operation. The AC current circulating through the input capacitor and loop 1 (LP1) are square wave with rise and fall times of 8 ns and slew rates as high as 300 A/µs (see Figure 50). At these fast slew rates, stray PCB inductance can generate a voltage spike as high as 3V per inch of PCB trace, VIND = L * di/dt. Therefore, the Ceramic input capacitor must be place as close as possible to the PVIN and PGND pins with as short and wide trace as possible. Also, the PVIN and PGND traces must be placed on the top layer. This will isolate the fast AC currents from interfering with the analog ground plane.
12. The 88PG8x7 has two internal grounds, analog (SGND) and power (PGND). The analog ground ties to all the noise sensitive signals (PSET, VSET, and SVIN) while the power ground ties to the higher current power paths. Noise on an analog ground can cause problems with the IC's internal control and bias signals. For this reason, separate analog and power ground traces are recommended. The signal ground is connected to the power ground at one point, which is the (-) terminal of the output capacitor.
13. Keep loop 2 (LP2) as small as possible and connect the (-) terminal of the output capacitor as close to the (-) terminal of the input capacitor. A back-to-back placing of bypass capacitors, as shown in Figure 51, is recommended for best results.

14. Keep the switching node (SW) away from the SFB pin and all sensitive signal nodes, minimizing capacitive coupling effects. If the SFB trace must cross the SW node, cross it at a right angle.
15. Try not to route analog or digital lines in close proximity to the power supply especially the VSW node. If this can't be avoided, shield these lines with a power plane placed between the VSW node and the signal lines.
16. The type of solder paste recommended for QFN packages is "No clean", due to the difficulty of cleaning flux residues from beneath the QFN package.

Figure 50: Simplified Schematic

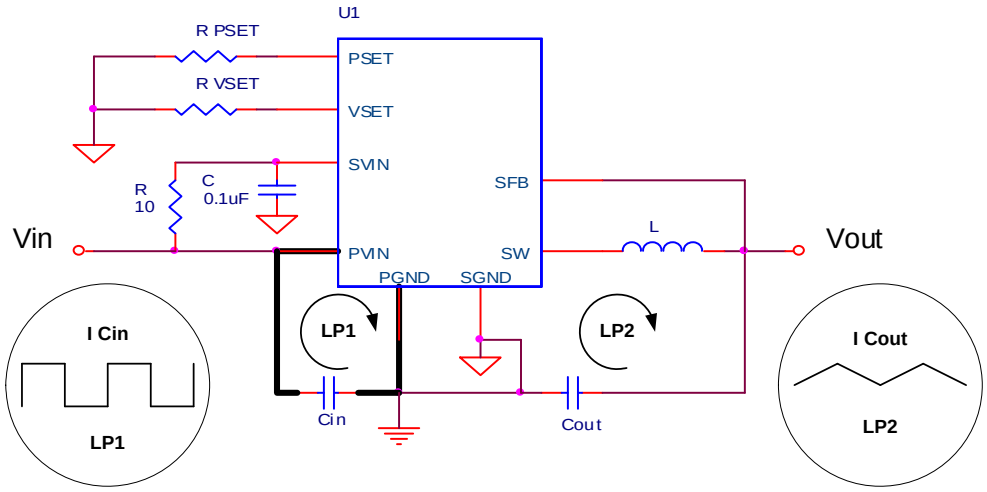
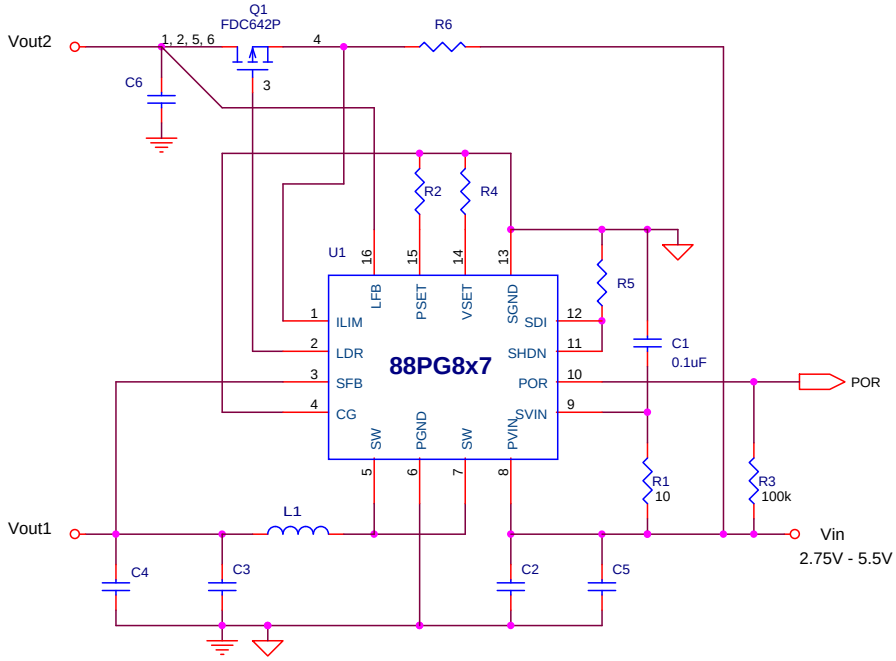


Figure 51: 88PG8x7 PCB Board Schematic



6.1.1 PC Board Layout Examples for 88PG8x7

- Actual board size = 700 mil x 700 mil; Area = 0.490 Sq. Inches.
- Total copper layers = 2 (Top and Bottom)
- All the components are on the top layer

Figure 52: Top Silk-Screen, Top Traces, Vias and Copper (Not to scale)

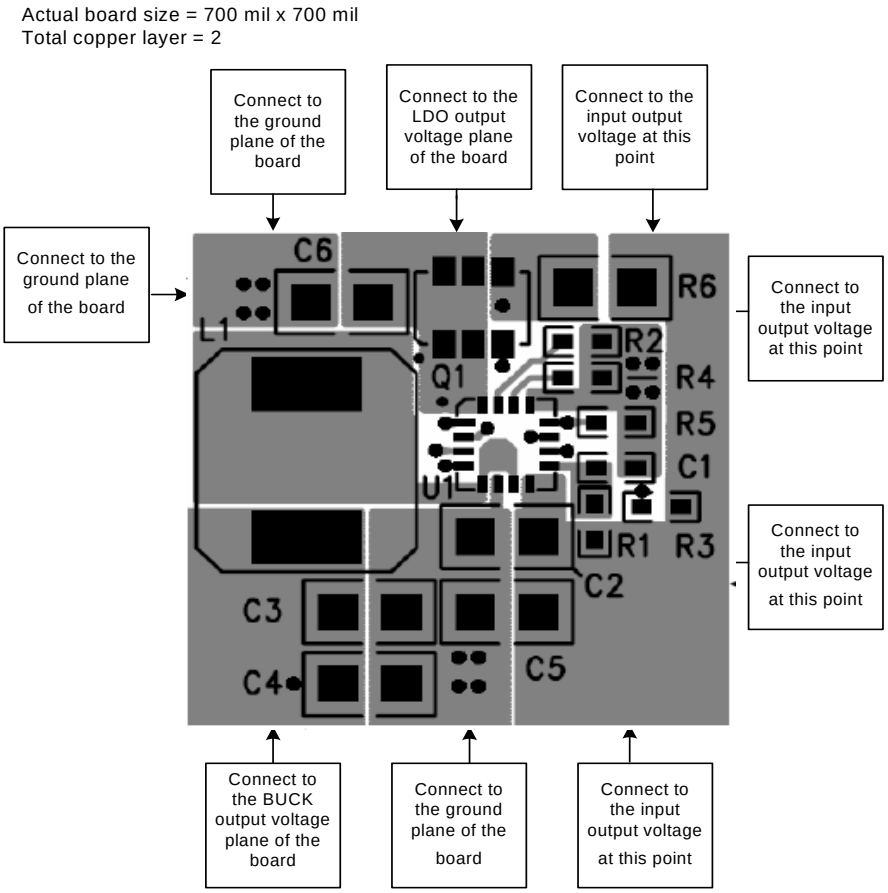
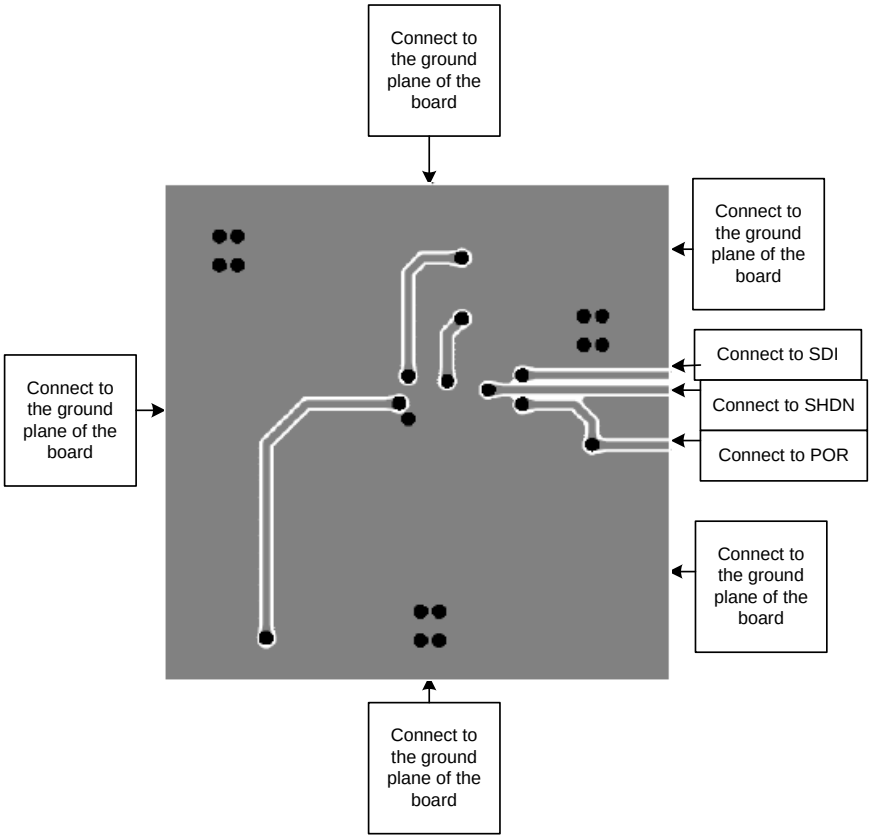


Figure 53: Bottom Silk Screen, Bottom Trace, Vias, and Bottom Copper (Not to scale)



6.2 Bill of materials for 88PG8x7

The following tables list the components used with the 88PG8x7.

Table 11: 88PG847 BOM

Item	Ref	Manufacturer	Manufacturer Part #	Description
1	**U1**	**Marvell Semiconductor**	**88PG847x**	**1 MHz, 4.5A Peak Current-Limit Step-Down Regulator with LDO Regulator Controller**
2	C1	TDK	C1005X5R1A104K	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
3	C2	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
4	C3	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	C4	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
6	C5	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
7	L1	Toko	#A918BY-1R3M=P3	1.3 µH, 3.1A, 28.6 mΩ, H = 2 mm, L = 6.2 mm, W = 6.3 mm
8	R1	Panasonic-ECG	ERJ-2RKF10R0X	10Ω, 1/16W, 1%, 0402 Case Size
9	R2			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
10	R3	Panasonic-ECG	ERJ-2GEJ104X	100 kΩ, 1/16W, 5%, 0402 Case Size
11	R4			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
12	R5	Panasonic-ECG	ERJ-2GEJ103X	10 kΩ, 1/16W, 5%, 0402 Case Size

Table 12: 88PG837 BOM

Item	Ref	Manufacturer	Manufacturer Part #	Description
1	**U1**	**Marvell Semiconductor**	**88PG837x**	**1 MHz, 3.0A Peak Current-Limit Step-Down Regulator with LDO Regulator Controller**
2	C1	TDK	C1005X5R1A104K	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
3	C2			

Table 12: 88PG837 BOM (Continued)

Item	Ref	Manufacturer	Manufacturer Part #	Description
4	C3	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	C4			
6	C5	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
7	L1	Toko	A918CY-2R0M=P3	2.0 µH, 2.47A, 24 mΩ, H = 2 mm, L = 6.2 mm, W = 6.3 mm
8	R1	Panasonic-ECG	ERJ-2RKF10R0X	10Ω, 1/16W, 1%, 0402 Case Size
9	R2			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
10	R3	Panasonic-ECG	ERJ-2GEJ104X	100 kΩ, 1/16W, 5%, 0402 Case Size
11	R4			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
12	R5	Panasonic-ECG	ERJ-2GEJ103X	10 kΩ, 1/16W, 5%, 0402 Case Size

Table 13: 88PG827 BOM

Item	Ref	Manufacturer	Manufacturer Part #	Description
1	**U1**	**Marvell Semiconductor**	**88PG827x**	**1 MHz, 2.5A Peak Current-Limit Step-Down Regulator with LDO Regulator Controller**
2	C1	TDK	C1005X5R1A104K	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
3	C2			
4	C3	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	C4			
6	C5	TDK	C2012X5R0J226MT	22 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
7	L1	Toko	A918BCY-3R3M=P3	3.3 µH, 1.99A, 39 mΩ, H = 2 mm, L = 6.2 mm, W = 6.3 mm
8	R1	Panasonic-ECG	ERJ-2RKF10R0X	10Ω, 1/16W, 1%, 0402 Case Size
9	R2			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size

Table 13: 88PG827 BOM (Continued)

Item	Ref	Manufacturer	Manufacturer Part #	Description
10	R3	Panasonic-ECG	ERJ-2GEJ104X	100 kΩ, 1/16W, 5%, 0402 Case Size
11	R4			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
12	R5	Panasonic-ECG	ERJ-2GEJ103X	10 kΩ, 1/16W, 5%, 0402 Case Size

Table 14: 88PG817 BOM

Item	Ref	Manufacturer	Manufacturer Part #	Description
1	**U1**	**Marvell Semiconductor**	**88PG817x**	**1MHz, 1.5A Peak Current-Limit Step-Down Regulator with LDO Regulator Controller**
2	C1	TDK	C1005X5R1A104K	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
3	C2			
4	C3	TDK	C2012X5R0J106MT	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	C4			
6	C5	TDK	C2012X5R0J106MT	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
7	L1	Toko	A918BCY-4R7M=P3	4.7 µH, 1.59A, 55 mΩ, H = 2 mm, L = 6.2 mm, W = 6.3 mm
8	R1	Panasonic-ECG	ERJ-2RKF10R0X	10Ω, 1/16W, 1%, 0402 Case Size
9	R2			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
10	R3	Panasonic-ECG	ERJ-2GEJ104X	100 kΩ, 1/16W, 5%, 0402 Case Size
11	R4			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
12	R5	Panasonic-ECG	ERJ-2GEJ103X	10 kΩ, 1/16W, 5%, 0402 Case Size

Table 15: 88PG807 BOM

Item	Ref	Manufacturer	Manufacturer Part #	Description
1	**U1**	**Marvell Semiconductor**	**88PG807x**	**1 MHz, 0.75A Peak Current-Limit Step-Down Regulator with LDO Regulator Controller**
2	C1	TDK	C1005X5R1A104K	0.1 µF, ± 10%, X5R, 10V, 0402 Case Size, Ceramic
3	C2			
4	C3	TDK	C2012X5R0J106MT	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
5	C4			
6	C5	TDK	C2012X5R0J106MT	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
7	L1	TDK	VLF3010AT-4R7MR70	4.7 µH, 0.7A, 240 mΩ, H = 1 mm, L = 2.6 mm, W = 2.8 mm
8	R1	Panasonic-ECG	ERJ-2RKF10R0X	10Ω, 1/16W, 1%, 0402 Case Size
9	R2			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
10	R3	Panasonic-ECG	ERJ-2GEJ104X	100 kΩ, 1/16W, 5%, 0402 Case Size
11	R4			See Any Voltage Programming Table, 1/16W, 1%, 0402 Case Size
12	R5	Panasonic-ECG	ERJ-2GEJ103X	10 kΩ, 1/16W, 5%, 0402 Case Size

Table 16: LDO Option BOM

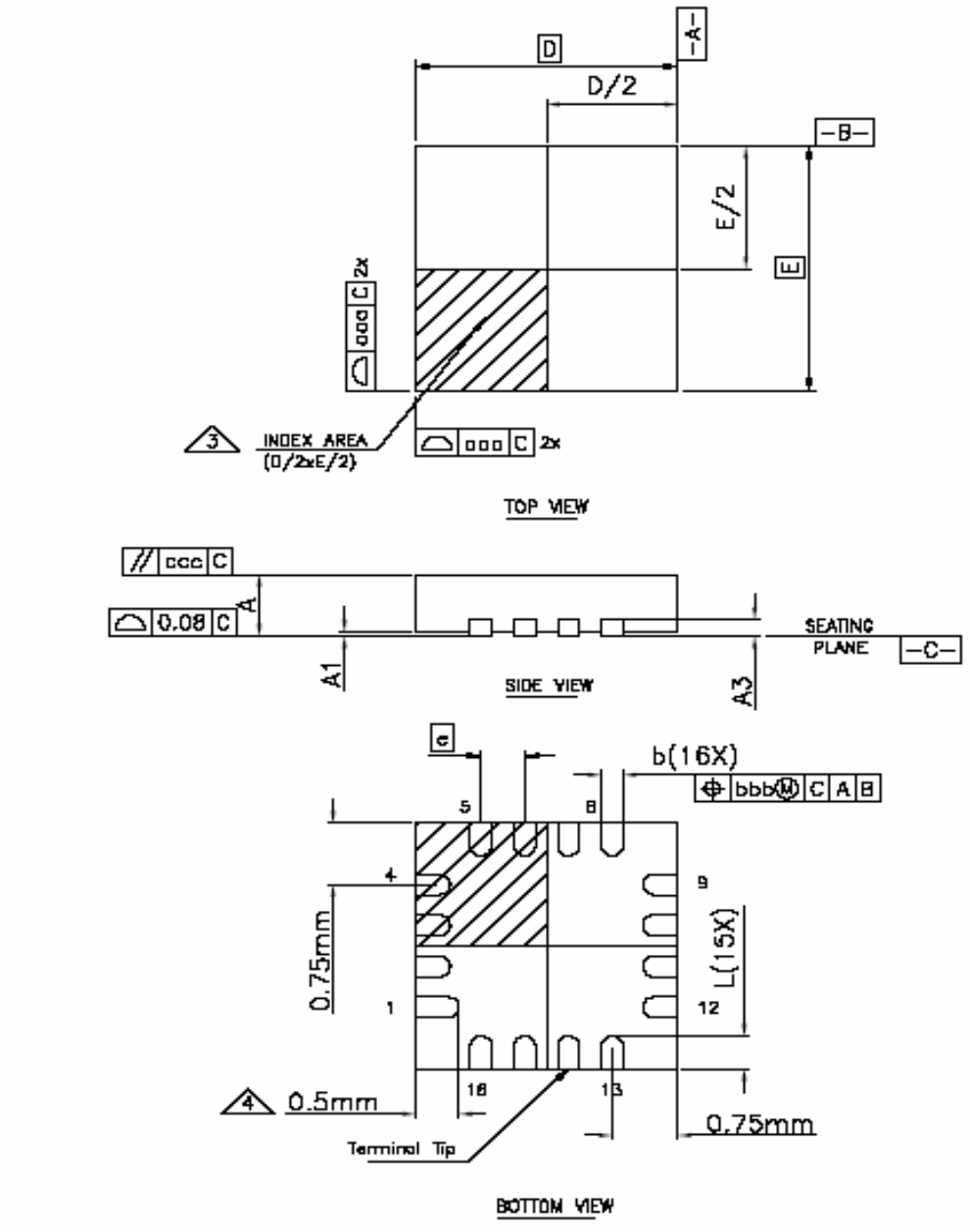
Item	Ref	Manufacturer	Manufacturer Part #	Description
1	Q1	Fairchild	FDC642P	PFET, 2.5V, SuperSOT-6 Package
2	C6	TDK	C2012X5R0J106MT	10 µF, ± 20%, X5R, 6.3V, 0805 Case Size, Ceramic
3	R6	Susumu Co Ltd.	RL1220T-R047-J	0.047Ω, 1/4W, 5%, 0805 Case Size

Table 17: Ceramic Capacitor Cross Reference

Manufacturer	Manufacturer Part #	Description
22 µF	Taiyo-Yuden	CE JMK212BJ226MG-T
	TDK	C2012X5R0J226MT
	Murata	GRM21BR60J226ME39L
10 µF	Taiyo-Yuden	CE JMK212BJ106MG-T
	TDK	C2012X5R0J106MT
	Murata	GRM219R60J106KE190
0.1 µF	Taiyo-Yuden	RM LMK105 BJ104KV-F
	TDK	C1005X5R1A104K

Section 7. Mechanical Drawing

7.1 88PG8x7 Mechanical Drawing



7.2 Dimensions

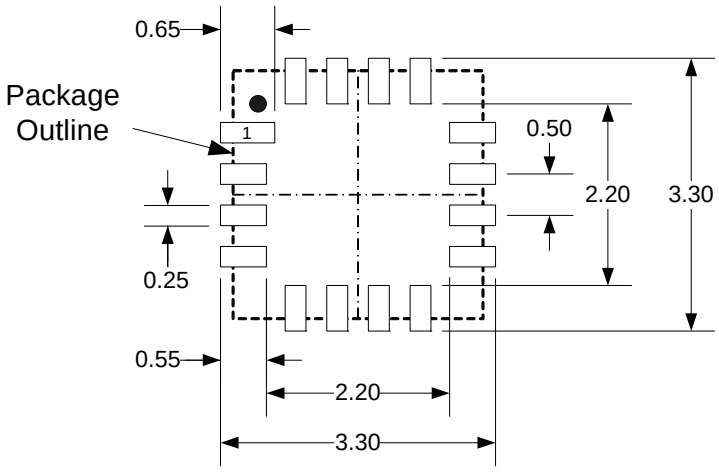
	Dimensions in mm			Dimensions in inch		
Symbol	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
aaa	--	--	0.15	--	--	0.006
bbb	--	--	0.10	--	--	0.004
ccc	--	--	0.10	--	--	0.004

Notes:

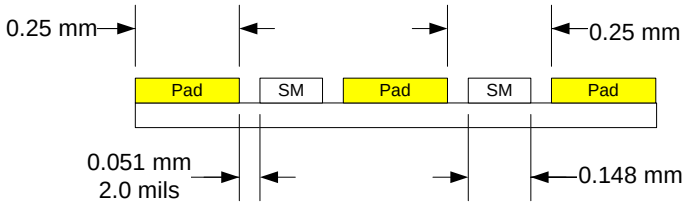
1. DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. DRAWINGS NOT TO SCALE
3. DIMENSIONS ARE IN MILLIMETERS
4. TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION
5. PIN 1 (0.5 mm) IS LONGER THAN OTHER PINS (0.4 mm)

7.3 Typical Pad Layout Dimensions

7.3.1 Recommended Solder Pad Layout



3x3 QFN-16
Land Pattern (mm)



Non-Solder Mask Defined Terminal
See Notes 4 and 5

Notes:

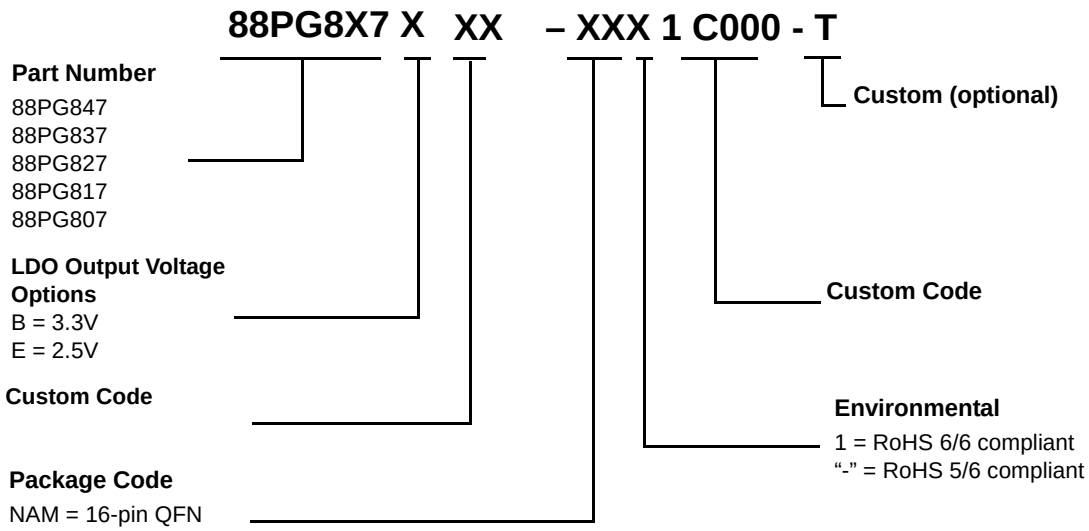
1. TOP VIEW
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE IN MILLIMETERS
4. OVERSIZE SOLDER MASK BY 4 MILS OVER PAD SIZE (2 MIL ANNULAR RING)
5. 0.148 mm SOLDER MASK (SM) BETWEEN PADS
6. TOLERANCE ±0.05 mm
7. PIN 1 IS LONGER THAN OTHER PINS BY 0.1 mm

Section 8. Ordering Information

8.1 Ordering Part Numbers and Package Markings

Figure 54 shows the ordering part numbering scheme for the 88PG8x7 devices. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 54: Sample Part Number



8.2 Sample Ordering Part Number

The standard ordering part numbers for the respective solutions are as follows:

Table 18: 88PG8x7 Ordering Part Numbers[1]

Marketing Part Number	Marking	LDO	Ambient Temperature Range[2]	Package[3]
88PG847B-NAM1	G47B	3.3V	-40 °C to 85 °C	3 X 3 QFN-16
88PG837B-NAM1	G37B	3.3V	-40 °C to 85 °C	3 X 3 QFN-16
88PG827B-NAM1	G27B	3.3V	-40 °C to 85 °C	3 X 3 QFN-16
88PG817B-NAM1	G17B	3.3V	-40 °C to 85 °C	3 X 3 QFN-16
88PG807B-NAM1	G07B	3.3V	-40 °C to 85 °C	3 X 3 QFN-16
88PG847E-NAM1	G47E	2.5V	-40 °C to 85 °C	3 X 3 QFN-16
88PG837E-NAM1	G37E	2.5V	-40 °C to 85 °C	3 X 3 QFN-16
88PG827E-NAM1	G27E	2.5V	-40 °C to 85 °C	3 X 3 QFN-16
88PG817E-NAM1	G17E	2.5V	-40 °C to 85 °C	3 X 3 QFN-16
88PG807E-NAM1	G07E	2.5V	-40 °C to 85 °C	3 X 3 QFN-16

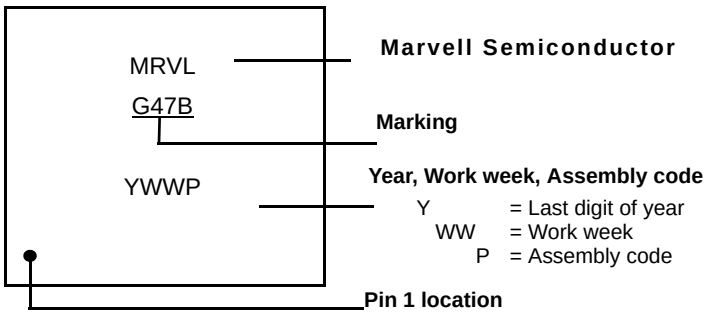
1. Contact Marvell® for details.
2. Specifications over the –40 °C to 85 °C operating temperature range are assured by design, characterization and correlation with statistical process controls.
3. Package dimensions are in mm.

8.3 Package Marking

8.3.1 Sample Package Marking and Pin 1 Locations

Figure 55 is an example of the package marking and pin 1 location for the 88PG847 part. Markings for the other variants are similar.

Figure 55: 88PG847 Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Locations of markings are approximate.

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