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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK1056, 2SK1057, 2SK1058

Silicon N-Channel MOS FET



ADE-208-1244 (Z)
1st. Edition
Mar. 2001

Application

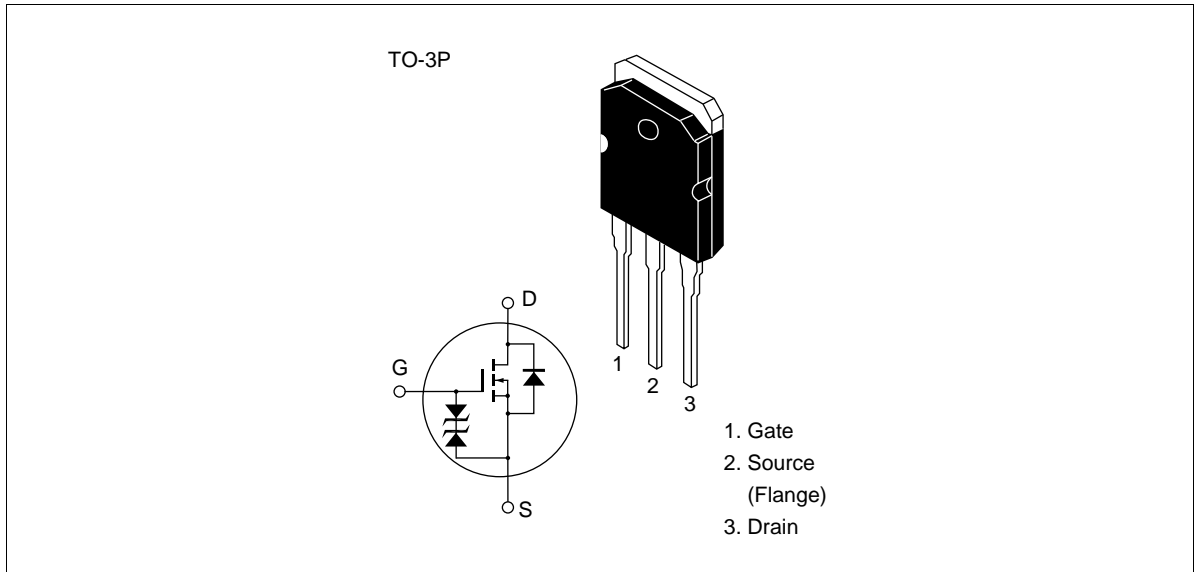
Low frequency power amplifier

Complementary pair with 2SJ160, 2SJ161 and 2SJ162

Features

- Good frequency characteristic
- High speed switching
- Wide area of safe operation
- Enhancement-mode
- Good complementary characteristics
- Equipped with gate protection diodes
- Suitable for audio power amplifier

Outline



Absolute Maximum Ratings (Ta = 25°C)

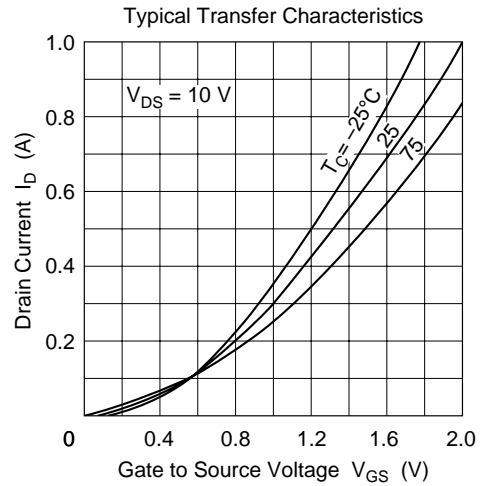
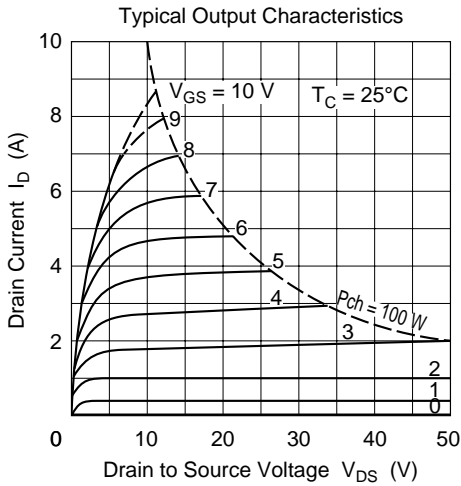
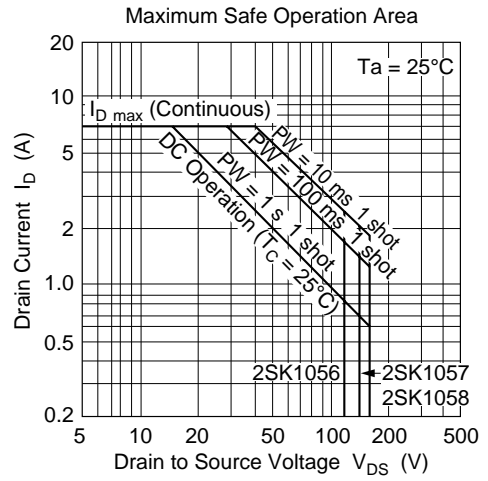
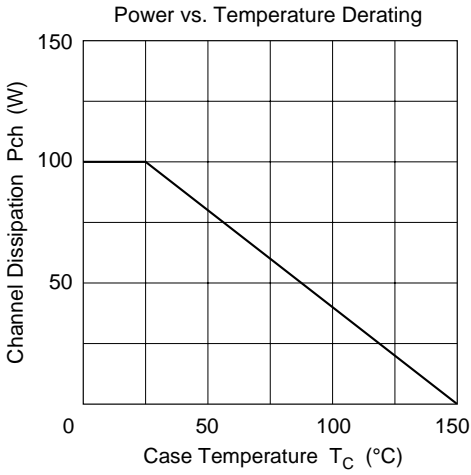
Item		Symbol	Ratings	Unit
Drain to source voltage	2SK1056	V_{DSX}	120	V
	2SK1057		140	
	2SK1058		160	
Gate to source voltage		V_{GSS}	±15	V
Drain current		I_D	7	A
Body to drain diode reverse drain current		I_{DR}	7	A
Channel dissipation		P_{ch}^{*1}	100	W
Channel temperature		Tch	150	°C
Storage temperature		Tstg	-55 to +150	°C

Note: 1. Value at $T_c = 25^\circ\text{C}$

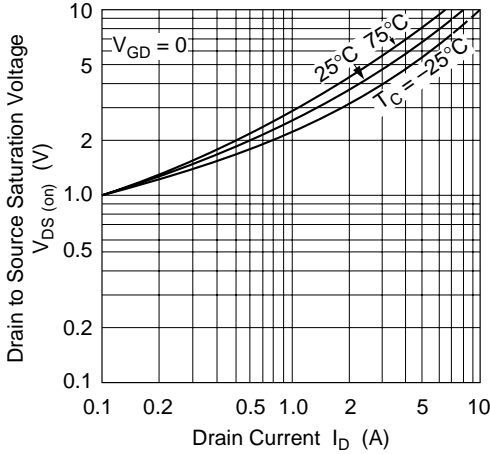
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
Drain to source breakdown voltage	2SK1056	$V_{(BR)DSX}$	120	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = -10 \text{ V}$
	2SK1057		140				
	2SK1058		160				
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 15	—	—	V	$I_G = \pm 100 \mu\text{A}$, $V_{DS} = 0$	
Gate to source cutoff voltage	$V_{GS(off)}$	0.15	—	1.45	V	$I_D = 100 \text{ mA}$, $V_{DS} = 10 \text{ V}$	
Drain to source saturation voltage	$V_{DS(sat)}$	—	—	12	V	$I_D = 7 \text{ A}$, $V_{GD} = 0$ *1	
Forward transfer admittance	yfs	0.7	1.0	1.4	S	$I_D = 3 \text{ A}$, $V_{DS} = 10 \text{ V}$ *1	
Input capacitance	Ciss	—	600	—	pF	$V_{GS} = -5 \text{ V}$, $V_{DS} = 10 \text{ V}$, $f = 1 \text{ MHz}$	
Output capacitance	Coss	—	350	—	pF		
Reverse transfer capacitance	Crss	—	10	—	pF		
Turn-on time	t_{on}	—	180	—	ns	$V_{DD} = 20 \text{ V}$, $I_D = 4 \text{ A}$,	
Turn-off time	t_{off}	—	60	—	ns		

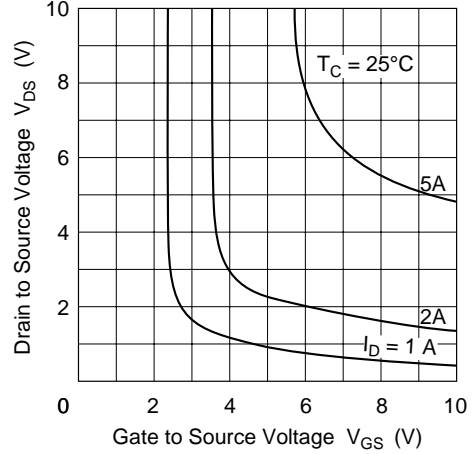
Note: 1. Pulse test



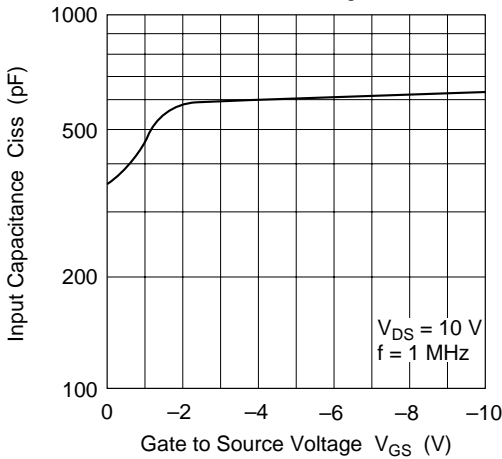
Drain to Source Saturation Voltage vs. Drain Current



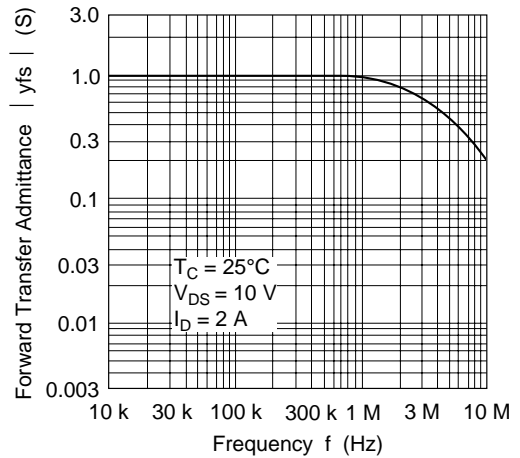
Drain to Source Voltage vs. Gate to Source Voltage

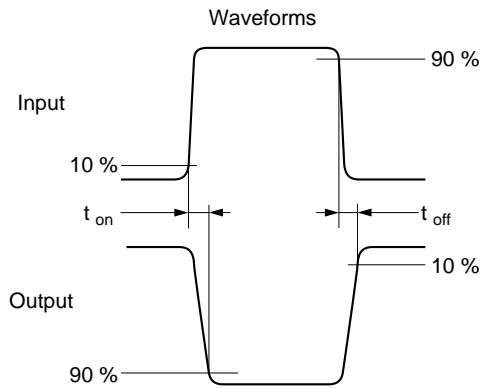
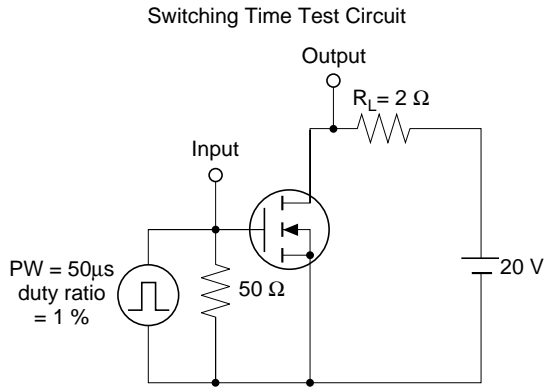
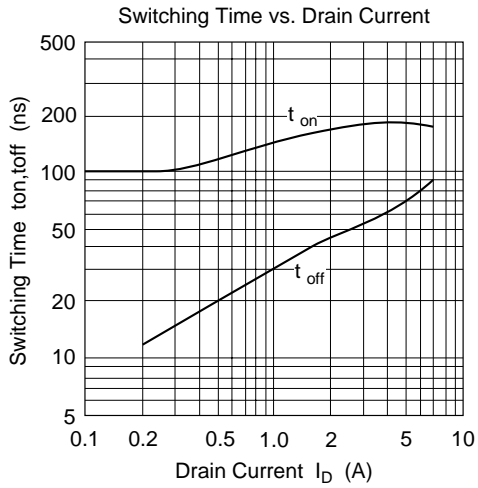


Input Capacitance vs. Gate Source Voltage



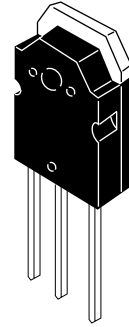
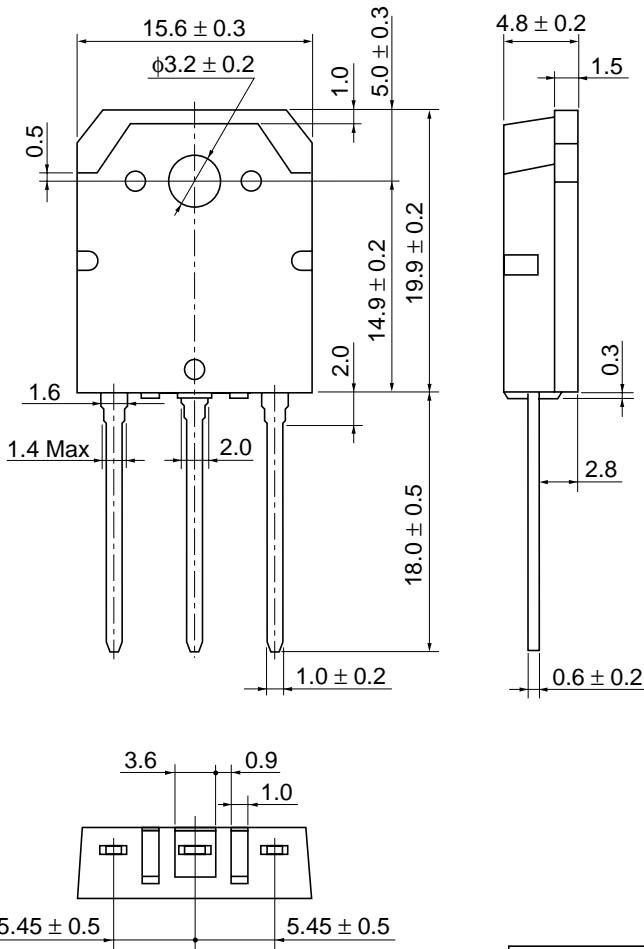
Forward Transfer Admittance vs. Frequency





Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	TO-3P
JEDEC	—
EIAJ	Conforms
Mass (reference value)	5.0 g

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