XZ1002-BD

8.5-11.0 GHz GaAs MMIC Core Chip

Rev 01-Sep-10

M/A-COM Tech Asia

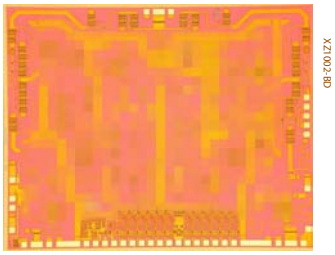
Features

- Highly Integrated Core Chip
- Transmit and Receive Modes of Operation
- Integrated T/R Switches, LNA and Driver Amplifier, 6-Bit Phase Shifter and 5-Bit Attenuator
- 21.0 dB Small Signal RX Gain
- +23.5 dBm TX P1dB Compression Point
- Compensated On-Chip Gate Bias Circuit
- Parallel Data Input
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010

General Description

The XZ1002-BD is a highly integrated dual path transmit/receive 3 port core chip. It is designed for applications operating within the 8.5 to 11.0 GHz range. The core consists of integrated transmit/receive switches, LNA, 6-bit phase shifter, 5-bit attenuator and driver amplifier. The digital control logic allows for parallel data input so that the phase shifter and attenuator may be changed instantaneously. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for phased array radar applications.

Chip Device Layout



Absolute Maximum Ratings

Supply Voltage (Vd)	6V
Gate Supply (Vs)	-6V to -4V
Logic Supply (Vl)	0 to 5.5V
Supply Current (Id)	350 mA
Input Power	TBD
Input Power RX	+20 dBm
Input Power RFCOM	+15 dBm
Storage Temperature (Tstg)	-65 to +165 ºC
Operating Temperature (Ta)	-55 to MTTF Graph[1]
Channel Temperature	MTTF Graph[1]

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

Electrical Characteristics (Ambient Temperature T=25 ºC)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	8.5		11
Input Return Loss RX/TX Mode (S11)	dB		15.0	
Output Return Loss RX/TX Mode (S22)	dB		15.0	
Receive Small Signal Gain (S21)	dB		21.0	
Transmit Small Signal Gain (S21)	dB		19.0	
Receive Output Power for 1 dB Compression Point (P1dB)	dBm		17.5	
Transmit Output Power for 1 dB Compression Point (P1dB)	dBm		23.5	
Receive Noise Figure (NF)	dB		5.2	
Receive Output Third Order Intercept (OIP3)	dBm		+28.0	
Phase Shifter Range (6 Bit, 64 states, 5.625 deg step)	deg	0		355
RMS Phase Error	deg		1.5	
Attenuator Range (5 Bit, 32 states, 0.9 dB step)	dB	0		28.5
RMS Attenuator Amplitude Error	dB		0.3	
Drain Bias Voltage (Vd1,2,3,4)	VDC	-	+4.0	+4.5
Gate Bias Voltage (Vs1,2,3)	VDC	-4.0	-5.0	
Control Voltage High (Va0,1,2,3,4) & (Vp0,1,2,3,4,5)	VDC	+2.0	+3.3	+5.0
Control Voltage Low (Va0,1,2,3,4) & (Vp0,1,2,3,4,5)	VDC	0.0	-	+0.8
Supply Current (Id) (Vd=4V, TX mode)	mA		280	
Supply Current (Ia) (Vs=-5V)	mA		35	
Supply Current (Il) (Vl=3.3V)	mA		9.5	

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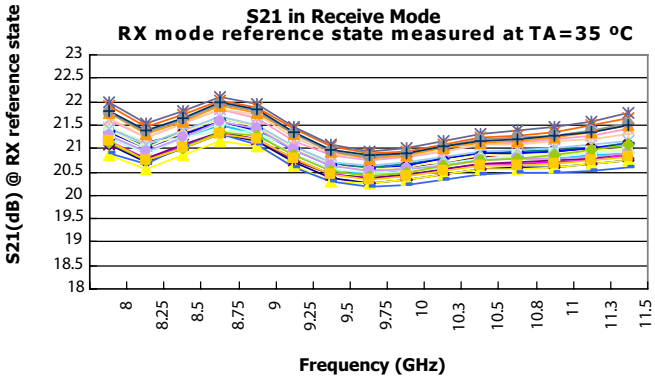
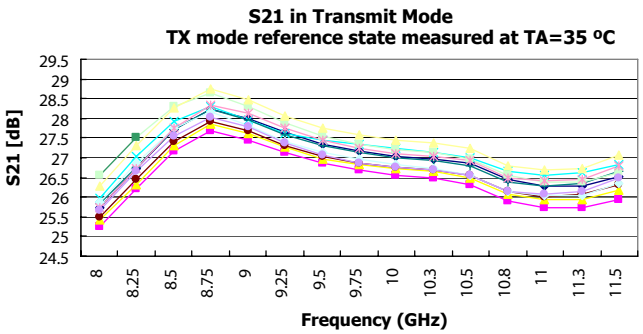
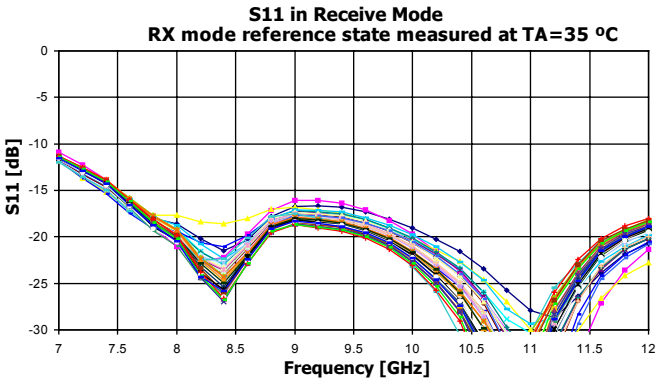
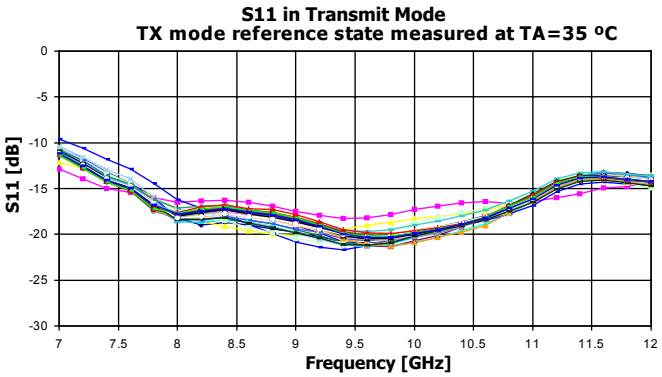
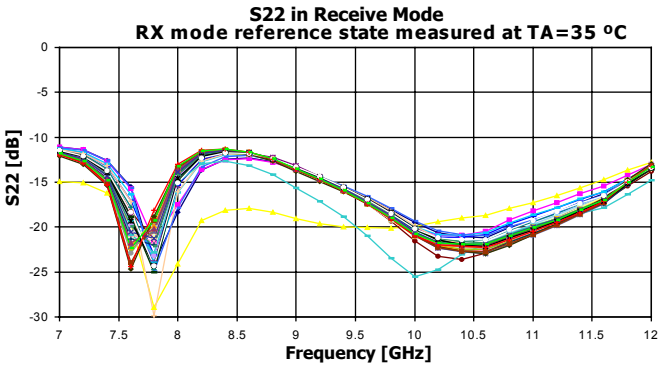
Measurements (Multiple Devices)

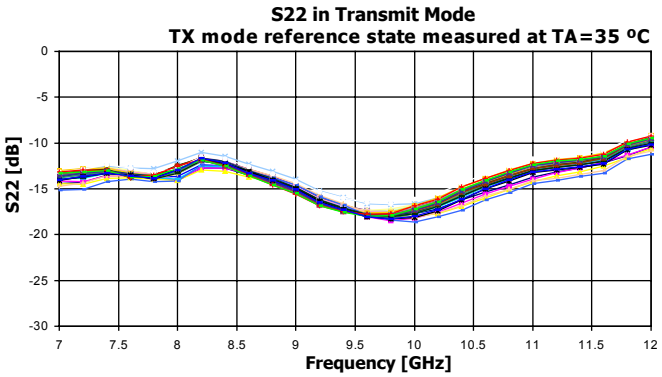












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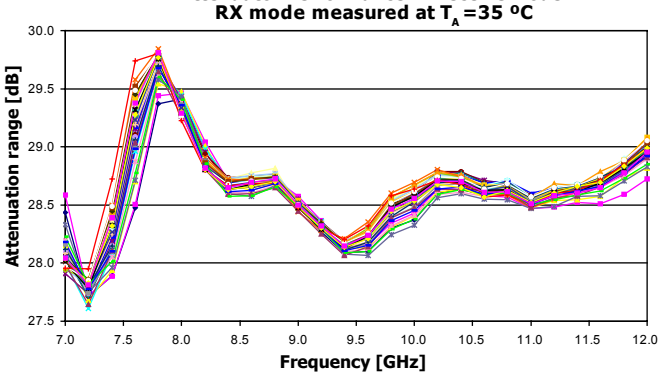
Measurements (cont.)

Attenuator Performance in Receive Mode
RX mode measured at T_A =35 ºC



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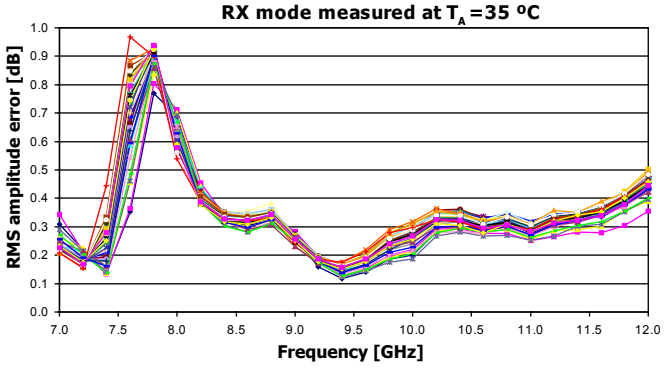

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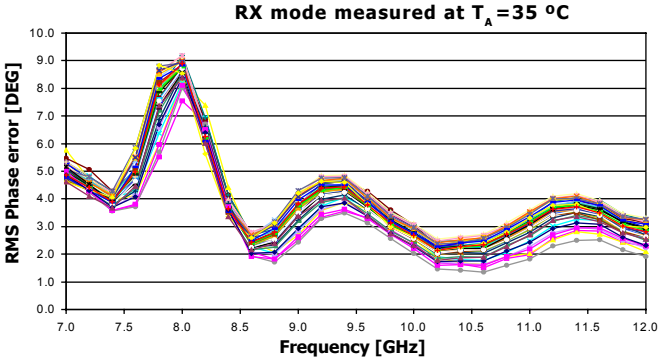
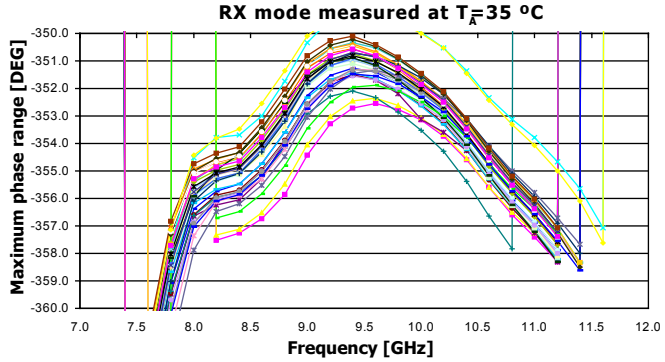
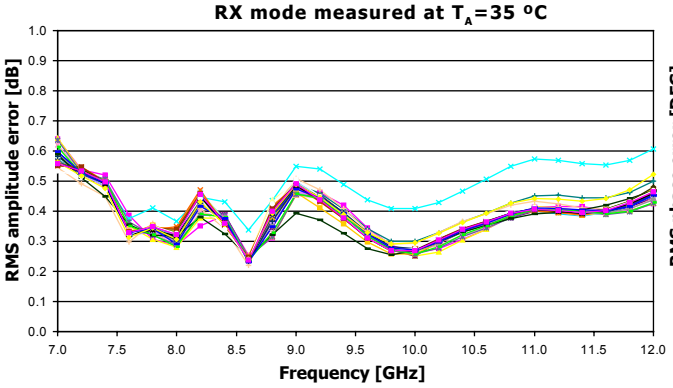


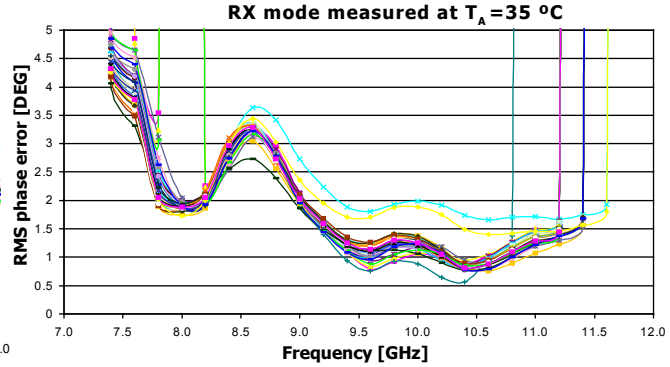
Phase Shifter Performance in Receive Mode
RX mode measured at T_A=35 ºC



Phase Shifter Performance in Receive Mode
RX mode measured at T_A =35 ºC



Phase Shifter Performance in Receive Mode
RX mode measured at T_A =35 ºC



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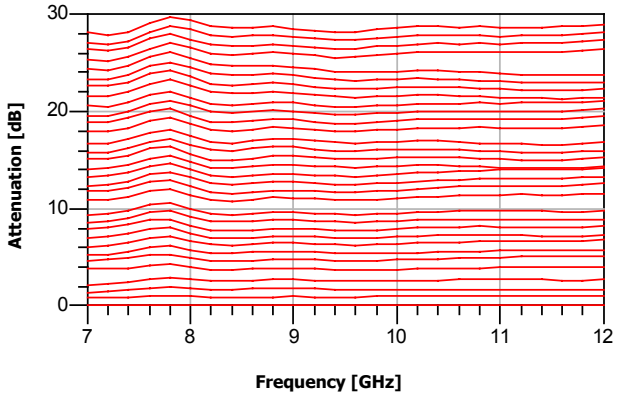
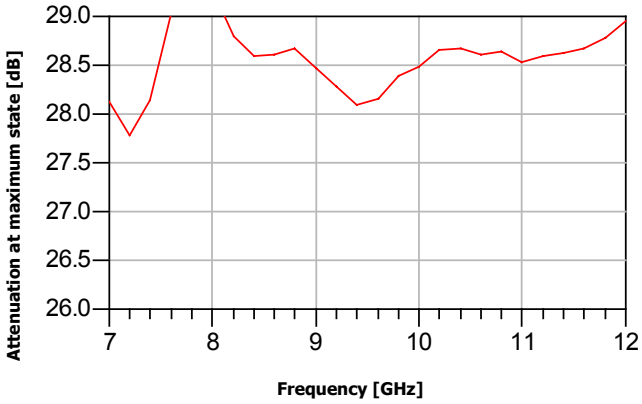
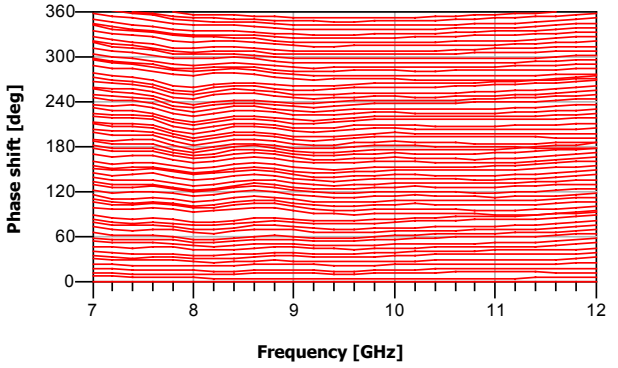
Measurements (cont.)

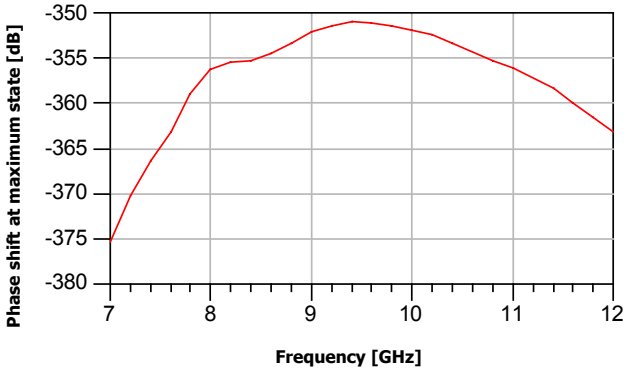
Attenuator Performance over 32 States in Receive Mode



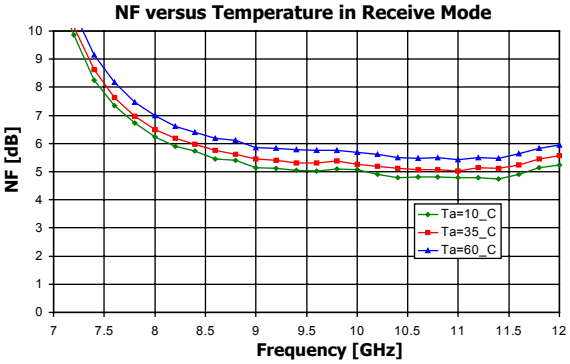


Phase Shifter Performance over 64 States in Receive Mode

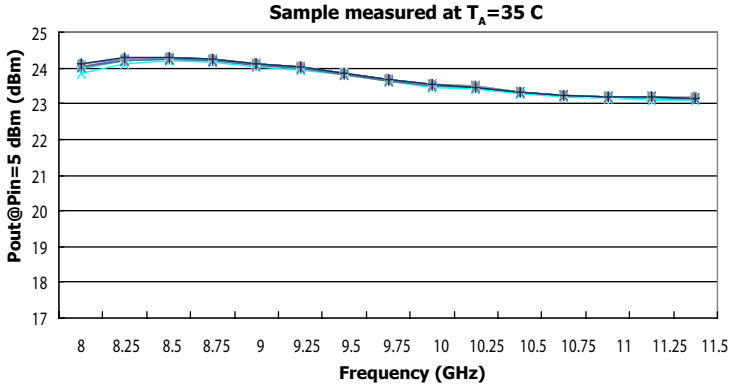




NF versus Temperature in Receive Mode



Large Signal Performance
Sample measured at T_A=35 C



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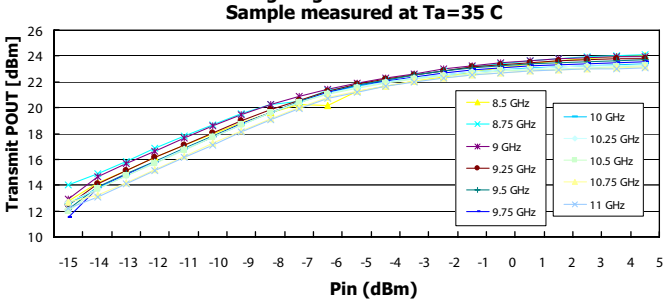
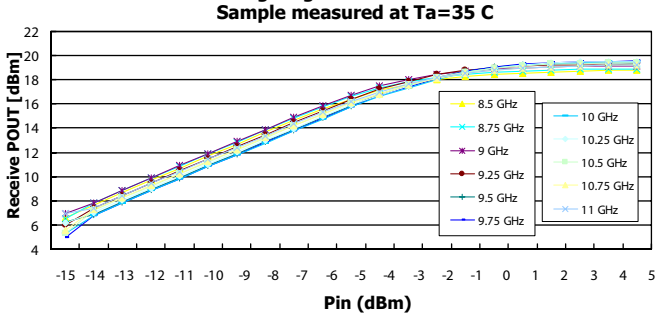
Measurements (cont.)

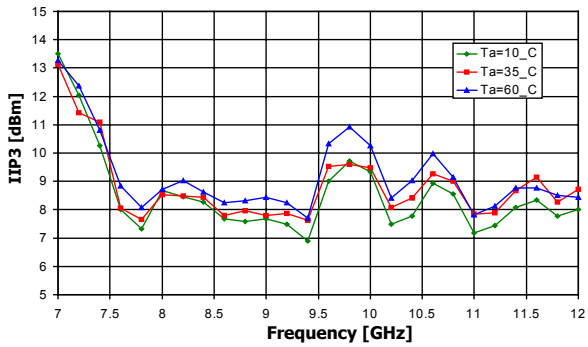
Large Signal Performance
Sample measured at Ta=35 C



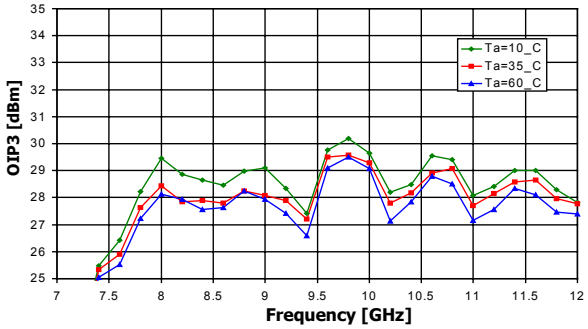
Large Signal Performance
Sample measured at Ta=35 C



IIP3 versus Temperature in Receive Mode

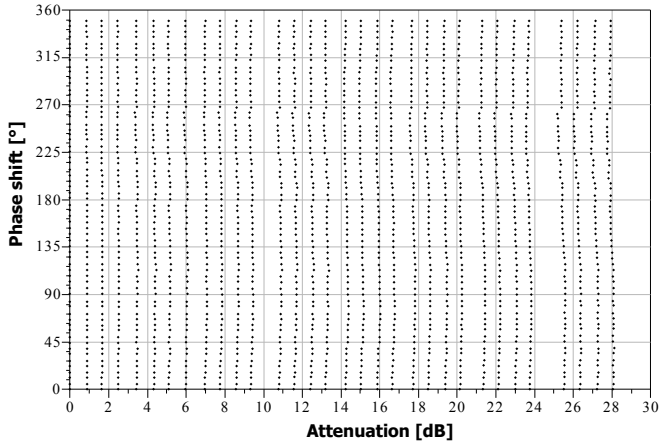


OIP3 versus Temperature in Receive Mode

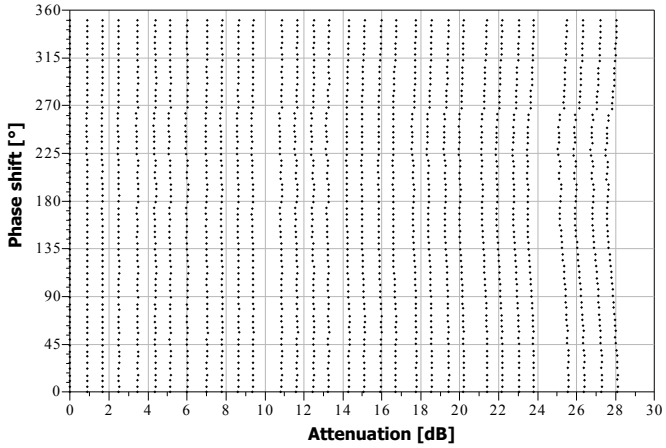


Gain Phase Plots

Measured in RX-mode at f=10 GHz and Ta=35 °C



Measured in TX-mode at f=10 GHz and Ta=35 °C



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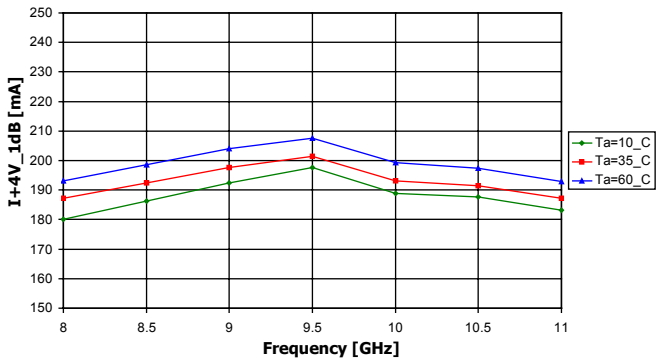
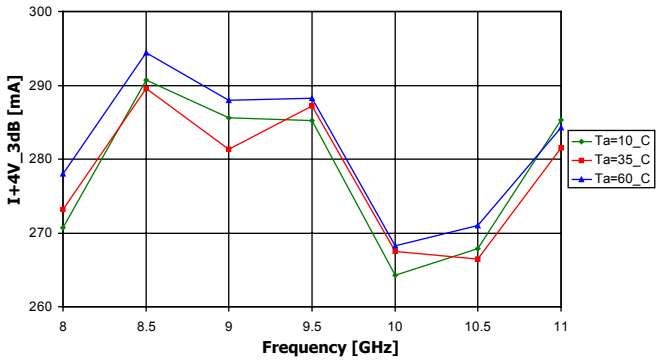
Measurements (cont.)

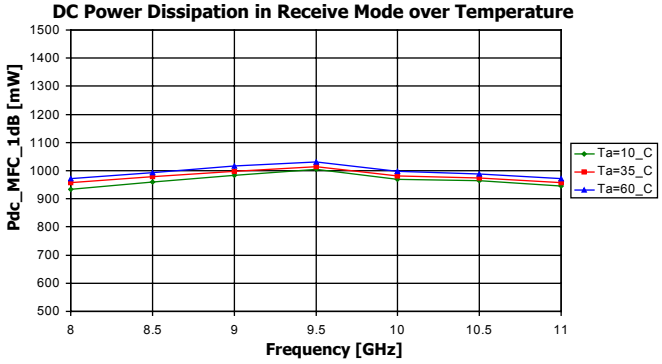
4V Supply Current in Receive Mode over Temperature



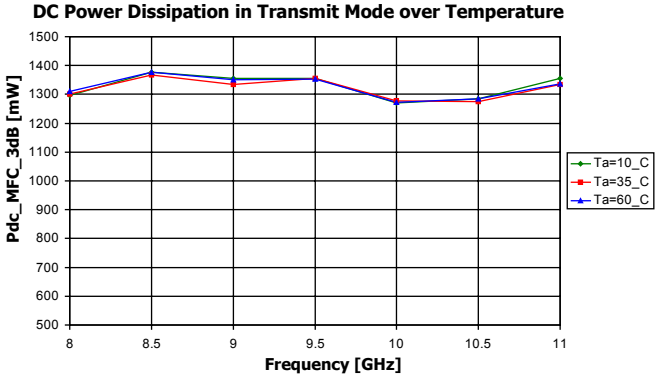
4V Supply Current in Transmit Mode over Temperature



DC Power Dissipation in Receive Mode over Temperature



DC Power Dissipation in Transmit Mode over Temperature



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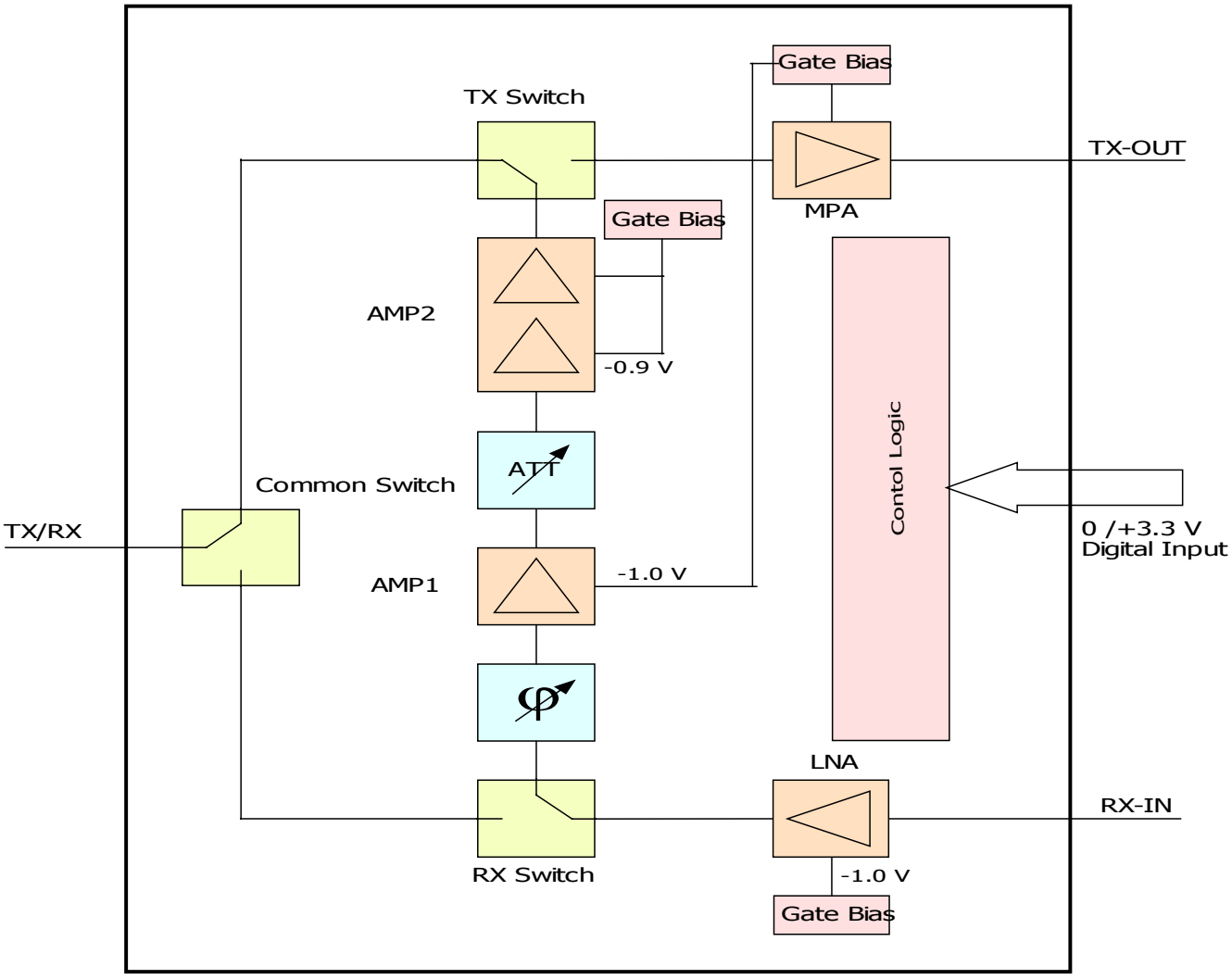
Core Chip Block Diagram



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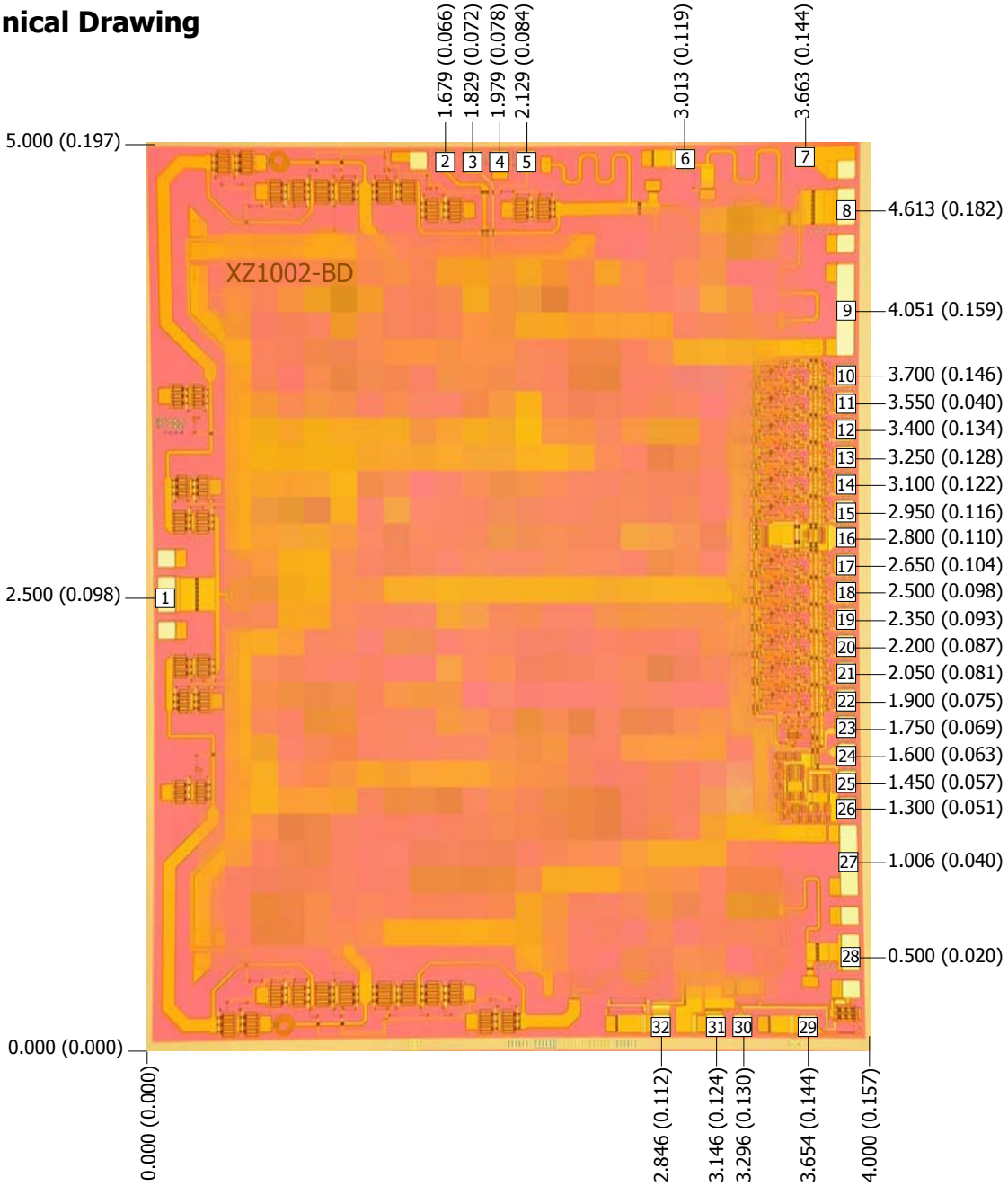
Mechanical Drawing



Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All Bond Pads are 0.100 x 0.100 (0.004 x 0.004).
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 12.4 mg.

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Bond Pad Designations

Pad #	Pad ID	Voltage [VDC]	Description
1	TX/RX	RF	TX input / RX output
2	Vd2	+4.0	Interstage Amp Supply
3	Vs1	-5.0	Gate Bias
4	GND	-	Decoupling Ground
5	RX Qnot	-3.4 (RX Mode)	RF Switch Monitor
6	Vd3	0 / +4.0	Output PA Supply
7	GND	-	Decoupling Ground
8	TXOUT	RF	Transmit [TX] Output
9	GND	-	Decoupling Ground
10	A0	0 / +3.3	0.9 dB Atten Bit
11	A3	0 / +3.3	7.2 dB Atten Bit
12	A4	0 / +3.3	14.4 dB Atten Bit
13	A2	0 / +3.3	3.6 dB Atten Bit
14	A1	0 / +3.3	1.8 dB Atten Bit
15	RX	0 / +3.3	TX/RX Switch
16	GND	-	Digital Ground Cross Talk Suppression

Pad #	Pad ID	Voltage [VDC]	Description
17	P5	0 / +3.3	180° Phase Bit
18	P2	0 / +3.3	22.5° Phase Bit
19	P4	0 / +3.3	90° Phase Bit
20	P3	0 / +3.3	45° Phase Bit
21	P1	0 / +3.3	11.25° Phase Bit
22	P0	0 / +3.3	5.625° Phase Bit
23	Qnot P0	0 (Ref State)	P0 Voltage Monitor
24	Q P0	-3.4 (Ref State)	P0 Voltage Monitor
25	Vs2	-5.0	Gate Bias
26	V3	+3.3	On-Chip Pull-Up
27	GND	-	Decoupling Ground
28	RXIN	RF	Receive [RX] Input
29	Vs3	-5.0	Gate Bias
30	Vd4	+4.0	Gate Bias (Positive)
31	GND	-	Decoupling Ground
32	Vd1	0 / +4.0	LNA Supply

App Note [1] Wire Bonding - Bond wires need to be as short as possible. The device is designed for a total bond wire inductance of 130 pH/RF bond pad. Different bond wire inductance will result in degraded performance.

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App Note [2] Biasing - The core chip can be operated in either Transmit [TX] or Receive [RX] mode. The bias setup is slightly different for each.

TX Mode - The TX mode is activated by setting the TX/RX switch, bond pad 14 (RX), to logic high (+3.3V) Vrx=3.3V. In this mode, bond pad 5 (Vd3) for biasing the output power amplifier (MPA) must be set to Vd3=4V. Additionally, the LNA is not operational in this [TX] mode so Vd1=0V.

RX Mode - To select the RX mode of operation the TX/RX switch, again bond pad 14 (RX), is set to logic low (0V) Vrx=0V. In this mode bond pad 32 (Vd1) for biasing the Low Noise Amplifier stage (LNA) must be set to Vd1=4V. In the RX mode the MPA is not used and must be set to Vd3=0V.

TX/RX Modes - Both the gate bias circuitry (Vs1,2,3) and the interstage amplifiers (Vd2,4) must be biased at Vs(1,2,3)=-5V and Vd(2,4)=4V respectively in both TX and RX operation.

CAUTION! - Also, make sure to properly sequence the applied voltages to ensure negative gate bias (Vs1,2,3) is available before applying the positive drain supply (Vd1,2,3,4).

App Note [3] Attenuator / Phase Shifter Control Bias - Logic buffering is integrated in the device to supply the necessary internal switching voltages. The reference state is enabled with logic "low" on all inputs, and the binary weighted phase(amplitude) states are switched by a logic "high" on the respective control input. Amplitude(phase) variation between phase(amplitude) states is minimized by optimization of internal matching and isolation between bits. Each bit is controlled using a '0' for the reference state and a '1' for the enabled state.

Attenuator/Phase Shifter Logic Truth Tables

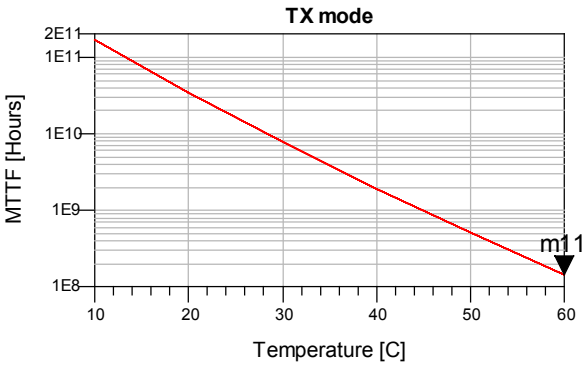
Atten Level (dB)	Va0	Va1	Va2	Va3	Va4
0	0	0	0	0	0
0.9	1	0	0	0	0
1.8	0	1	0	0	0
3.6	0	0	1	0	0
7.2	0	0	0	1	0
14.4	0	0	0	0	1
-	-	-	-	-	-
27.9	1	1	1	1	1

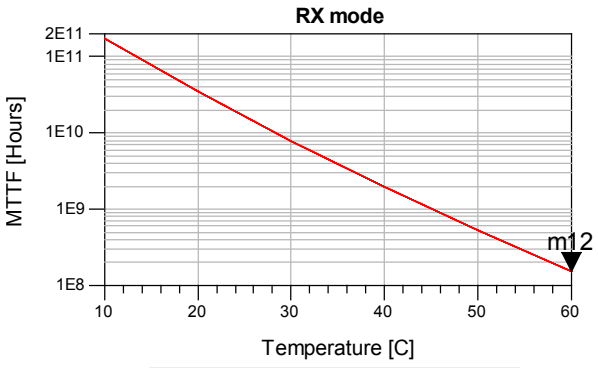
Phase Shift (degrees)	Vp0	Vp1	Vp2	Vp3	Vp4	Vp5
0º	0	0	0	0	0	0
5.625º	1	0	0	0	0	0
11.25º	0	1	0	0	0	0
22.5º	0	0	1	0	0	0
45º	0	0	0	1	0	0
90º	0	0	0	0	1	0
180º	0	0	0	0	0	1
354.375º	1	1	1	1	1	1

App Note [4] Bias Arrangement - Each DC Bias pad (Vd1,2,3) needs to have DC bypass capacitance (~80-120 pF) as close to the device as possible.

MTTF Graphs

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.





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Handling and Assembly Information

CAUTION! - M/A-COM Tech Asia MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- Do not ingest.
- Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.
- Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.

Life Support Policy - M/A-COM Tech Asia's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of M/A-COM Tech Asia. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ESD - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

Die Attachment - GaAs Products from M/A-COM Tech Asia are 0.100 mm (0.004") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the M/A-COM Tech Asia "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001^2 thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280º C (Note: Gold Germanium should be avoided). The work station temperature should be 310ºC +/- 10º C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

Wire Bonding - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Ordering Information

Part Number for Ordering	Description
XZ1002-BD-000V	RoHS compliant die packed in vacuum release gel paks
XZ1002-BD-EV1	XZ1002-BD Evaluation Module

Caution: ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling this device.

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