



STH200N55F3-2

N-channel 55 V, 1.8 mΩ, 160 A, H²PAK
STripFET™ III Power MOSFET

Preliminary data

Features

Type	V _{DSS}	R _{DS(on) max}	I _D (1)
STH200N55F3-2	55 V	< 2.6 mΩ	160 A

1. Current limited by package

- Ultra low on-resistance
- 100% avalanche tested

Application

- Switching applications

Description

This STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

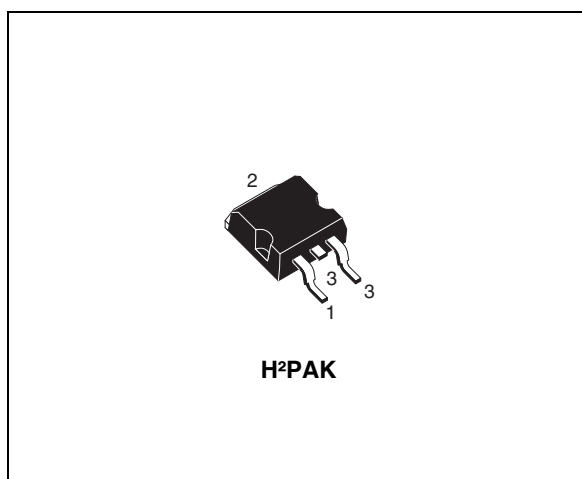
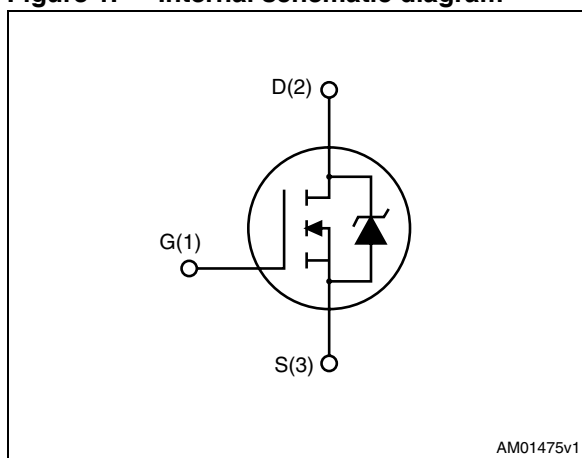


Figure 1. Internal schematic diagram



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Table 1. Device summary

Order code	Marking	Package	Packaging
STH200N55F3-2	200N55F3	H ² PAK	Tape and reel

Contents

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
3	Test circuits	6
4	Package mechanical data	7
5	Revision history	10

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	55	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	160	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	160	A
$I_{DM}^{(2)}$	Drain current (pulsed)	640	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.0	J
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to Rthj-c
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 60\text{ A}$, $V_{DD} = 35\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
Rthj-pcb ⁽¹⁾	Thermal resistance junction-pcb max	35	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4 2 oz Cu

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	55			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 60\text{ A}$		1.8	2.6	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	6800	-	pF
C_{oss}	Output capacitance			1450		pF
C_{rss}	Reverse transfer capacitance			15		pF
Q_g	Total gate charge	$V_{DD} = 44\text{ V}$, $I_D = 120\text{ A}$,	-	100	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$		30		nC
Q_{gd}	Gate-drain charge	Figure 3		26		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 27.5 \text{ V}$, $I_D = 60 \text{ A}$ $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$, Figure 2	-	25 150	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 27.5 \text{ V}$, $I_D = 60 \text{ A}$ $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$, Figure 2	-	110 50	-	ns ns

Table 7. Source drain diode

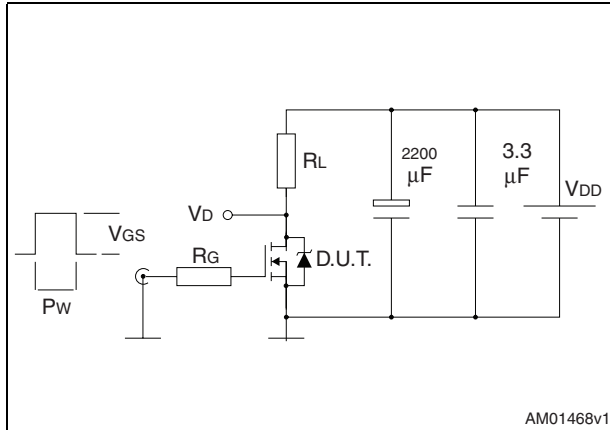
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SD}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		160 640	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 160 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 120 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 35 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ Figure 7	-	60 110 3.5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Test circuits

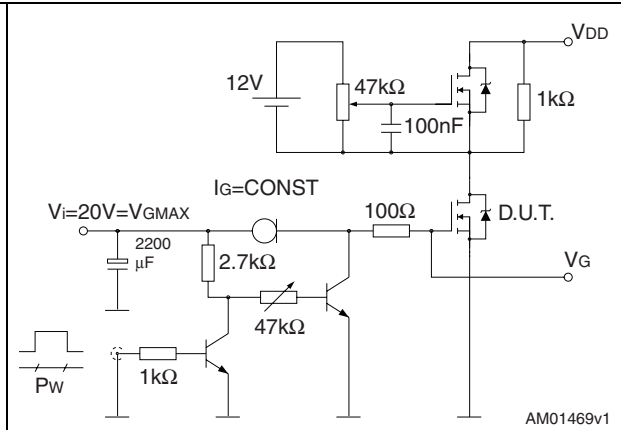
3 Test circuits

Figure 2. Switching times test circuit for resistive load



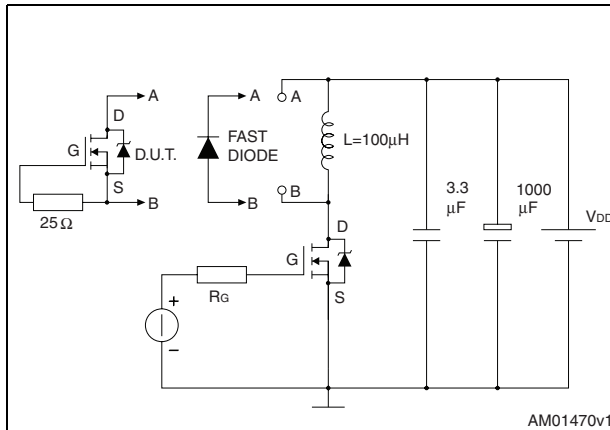
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Figure 3. Gate charge test circuit



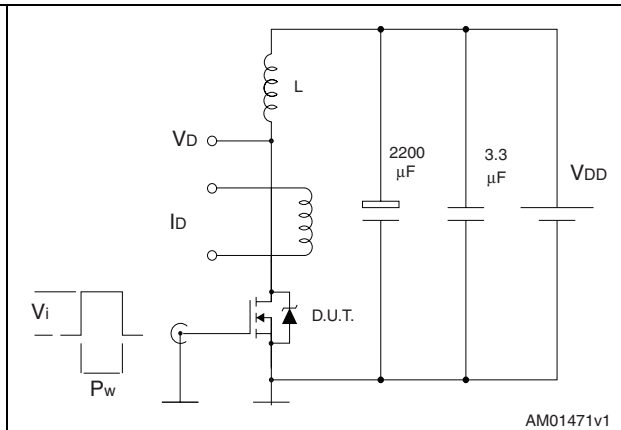
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Figure 4. Test circuit for inductive load switching and diode recovery times



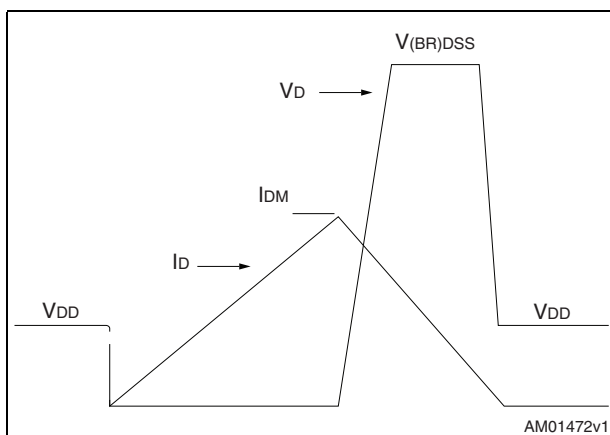
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Figure 5. Unclamped inductive load test circuit



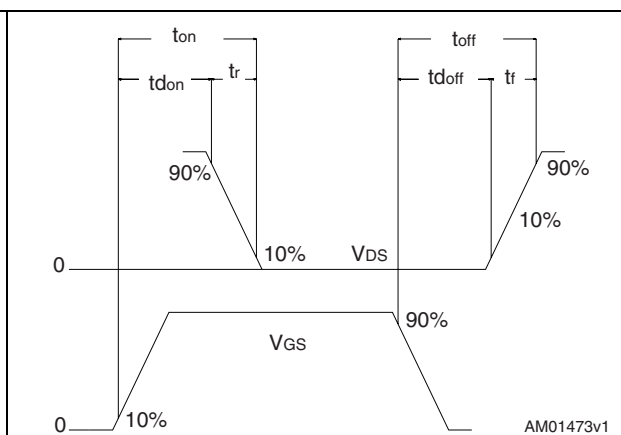
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



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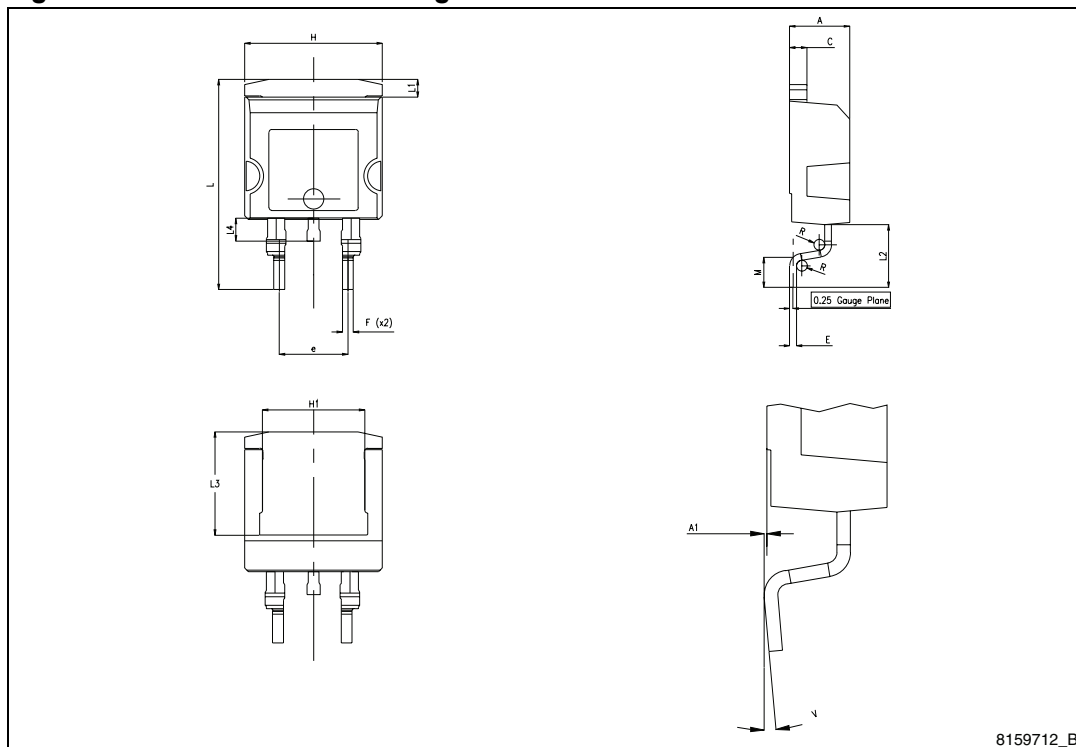
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. H²PAK 2 leads mechanical data

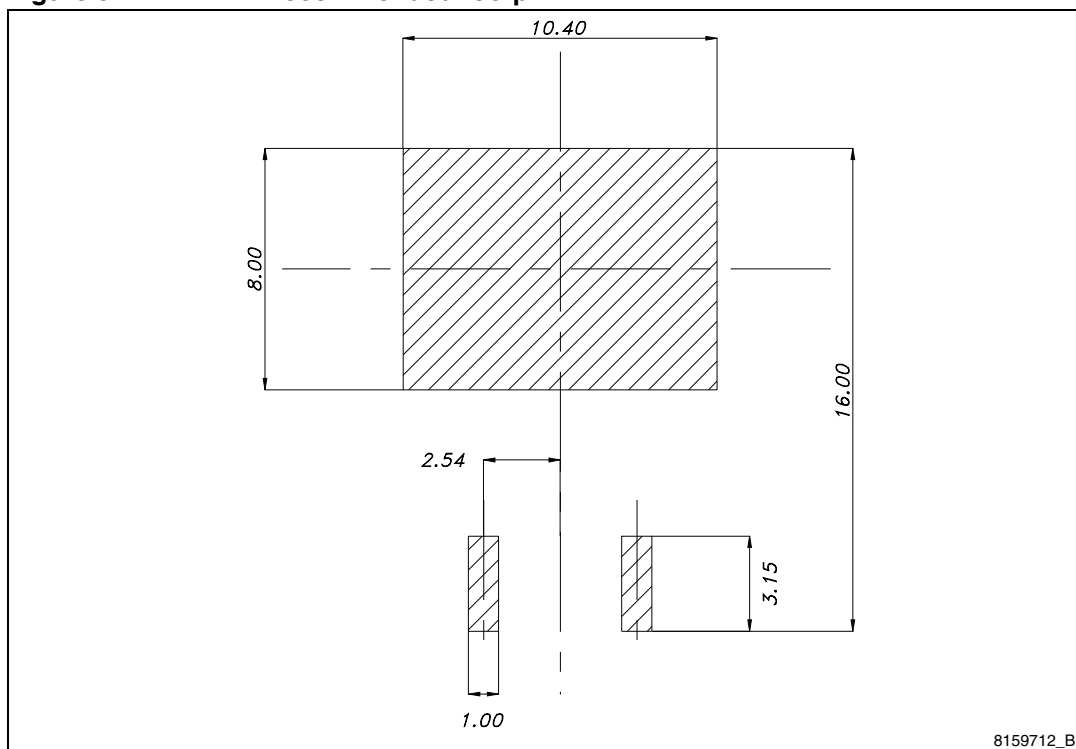
Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 8. H²PAK 2 leads drawing



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Figure 9. H²PAK 2 recommended footprint



8159712_B

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
30-Jul-2009	1	First release.

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