This is an abbreviated datasheet.
Contact a Cypress representative
for complete specifications.

T-52-33-25

CY7C613

CYPRESS SEMICONDUCTOR

MBus Memory Controller

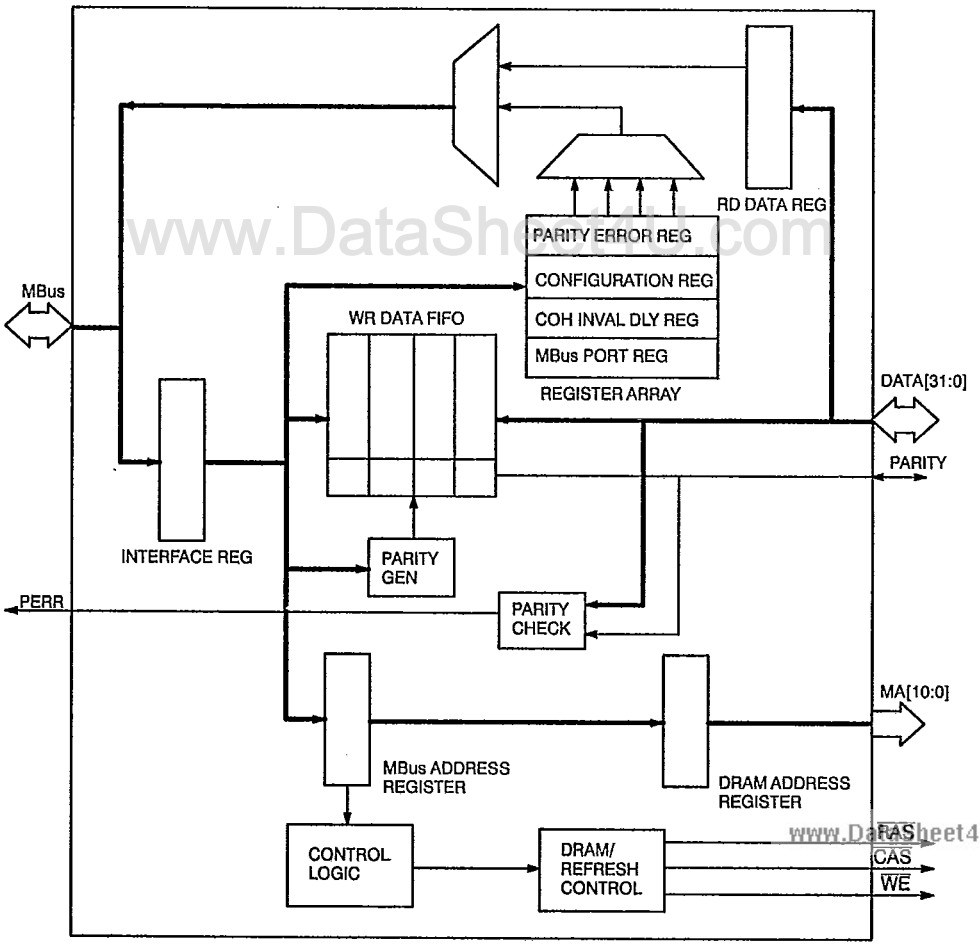
Features

- Level-1 and Level-2 MBus operations
- Four-deep FIFO for optimum writes to DRAMs
- Byte-wide odd/even or no parity
- CAS before RAS refresh scheme
- Supports 1M x 9, 4M x 9, 1M x 36, 4M x 36 DRAM modules
- Memory configurations supported: 8 Mbytes to 128 Mbytes of memory in steps of 8 Mbytes
- Clock speed of 40 MHz
- External buffers needed for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and memory address for 128 Mbytes of DRAM
- Built-in scan chain for 100% fault coverage
- 1- to 128-byte DRAM read or write transaction using fast page mode access

Introduction

The CY7C613 is a high-performance CMOS integrated circuit that provides all the necessary control signals between the DRAM array and the MBus in a SPARC processor–based workstation. The CY7C613 is implemented in 160-pin PQFP. Due to the fact that both the MBus and the memory data path are 64 bits wide, the design of this ASIC is sliced. Hence, a pair of CY7C613 ASICs are required to interface MBus to the DRAM array. The chip that interfaces MAD[63:32] is termed the EVEN slice, while the chip that interfaces MAD[31:0] is termed the ODD slice.

Logic Block Diagram



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